EXPERIMENTAL SETUP AND ELECTRICAL CHARACTERIZATION OF ELECTRONIC MATERIAL AND DEVICES

by

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DEDICATION

I dedicate this work to my parents to be my first teachers, and well-wisher all the time.

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ABSTRACT

Due to our increasing energy demands, access to affordable clean energy resource will be of great importance for a society and economy in the near future. Two separate developments are required to secure stable energy supplies: versatile adoption of revolutionary technologies that can be alternatives to fossil fuel-based energy resources and the introduction of products that consume less energy. One way to fulfil the first goal is to utilize more solar energy, generating electricity and fulfil energy requirement. The second goal can be achieved by developing more efficient electronic, cooling, and lighting systems. It is crucial to study the properties of the semiconductor materials to better understand how to make high performance devices with higher energy efficiencies.

This thesis focusses primarily on the experimental set up and related instrumentation for the electrical characterization of semiconductor materials and devices. This set up was used to characterize a solar cell device (based on copper-indium-gallium-selenium: CIGS) for energy application and a Schottky device based on the high bandgap semiconductor material Ga_2O_3 for power device application. In this exploration, temperature dependent current-voltage, capacitance-voltage, and admittance spectroscopy were used to probe the electronic quality in terms of defect concentration, charge carrier mobility, and other charge transport properties. The results are helpful for further technological advancement of semiconductor devices and materials.

I. INTRODUCTION

1.1 Solar Energy and Solar Cell – A Short History

The energy crisis is a serious and challenging problem in the present world. As our current advanced society, increases in population, and because of technical civilization, the energy requirement has drastically increased and keeps increasing at a very fast rate day by day [1]. To date, for our daily energy need, we are mostly depending on the fossil fuels based energy sources [coal (~15%), gas (~29%), oil (~37%) etc.] and supplemented by non-fossils based energy [hydroelectric (~25%), wind energy (21%) and nuclear energy(~9%)][2]. The fossil fuel based energy resources and nuclear energy are non-renewable. The major challenge is, if the society's energy demand keeps on increasing at this rate, then we will be running out of non-renewable sources soon [3]. In addition, the overconsumption of carbon based energy resources results in an adverse impact on both, the environment/ecosystem (climate change, pollution, and global warming) and hence on our society [3]. Therefore, to solve the increasing global energy demands, a cost effective, reliable, and renewable energy source needs to be established [4].

Fig.1. 1 Solar panel in operation under solar energy.

The sun is a universal source of all sorts of: in a direct form (solar energy – light and heat) as well as indirect form (wind, biomass and hydraulic energy) [5]. In addition, the Sun shines almost every day in every part of the world. The energy from the Sun that showers the Earth is several thousand times greater than our daily energy needs. It's estimated that in 2050 the world energy consumption rate will be 27.6 TW, and 58,300 TW will be the extractable potential of solar energy [6]. Therefore, part of the solar energy can solve the energy requirement. In addition, the solar radiation is a sustainable, clean, and a reliable renewable energy source that could solve our society's energy demand and solve the energy crisis [7].

A solar cell device that can directly convert the solar energy to electricity (as in Fig.1. 1 – the solar panel in operation under solar energy) is often called a photovoltaic device [8].

Photovoltaic history started in 1876 when William Grylls Adams and one of his students, Richard Day, found that when selenium was exposed to light, it produces electricity [9]. Although the selenium cells were not efficient, it was proved that light, without moving parts or heat, could be directly converted into electricity.

In 1953, Calvin Fuller, Gerald Pearson, and Daryl Chapin invented the silicon solar cell [10]. This cell produced was more efficient than Adams selenium cell, and it produced enough electricity to run small electrical devices.

The first solar cells started to be available in the market in 1956, but the price was really high (Around $300 USD for a 1 watt solar cell) [11]. Later that year, the first solar cells started to be used in toys and radios, which were the first items to have solar cells available to consumers.

In the late 1950's and early 1960's space programs in the USA and Russia stimulated the further development of solar cells. In the late 1960's, solar cells became the standard use for powering space bound satellites [11].

Dr. Elliot Berman, with financial help from Exxon Corporation, designed a less costly solar cell in the early 1970's [11]. This was possible by using a poorer grade of silicon and packaging the cells with cheaper materials. This mostly benefited many gas and oil fields that were far away from power lines and needed small amounts of electricity to combat corrosion in well heads and piping.

From the 70's to the 90's, solar cells began to be used in railroad crossings, to power homes in remote places, in microwave towers to expand telecommunication capabilities and even in desert regions to bring water to the soil where line fed power was not an option [11].

Today we see solar cells everywhere. Solar powered homes, gates, cars, and even aircrafts. With the current cost of solar cells coming down, solar power looks really promising for almost any application, and research in this field is growing more and more [12].

1.2 Semiconductor Background

1.2.1 Basic Semiconductor Physics

Each solid has its own characteristics energy band structure. The outer two bands determine its electric properties and are called the valance band (VB) and the conduction band (CB) [13]. The energy difference between the conduction (E_C) and valance (E_V) band is the bandgap (E_g) of materials, i.e., $E_g = E_C - E_V$. To be conductive, the material should have free electrons and empty states. There are three types of materials so called

metals, semiconductors, and insulators. The different energy band diagram are shown in Fig.1. 2. Metals (i.e. Au, Cu, Ag etc.) have free electrons and a partially filled outer band. This band can be a single band that is partially filled or can consist of an overlapping valance and conduction band. Insulators (i.e. glass, diamond etc.) have filled valence bands and empty conduction bands, separated by a large energy gap (typically, $E_g > 4$ eV) and possess high resistivity. The term semiconductor arises from the ability of certain materials to conduct electric currents "part time", i.e., the conductivity of semiconductor material is somewhere in between the conductivity of metals and insulators. Semiconductors (Si, Ge, GaAs etc.) have a similar band structure as insulators but with a much smaller bandgap (i.e. E_g =1.1 eV for Si, 0.67 eV for Ge and 1.43 eV for GaAs). Their conductivity depends strongly on the temperature and increases with higher temperature opposite to the temperature dependence of metals.

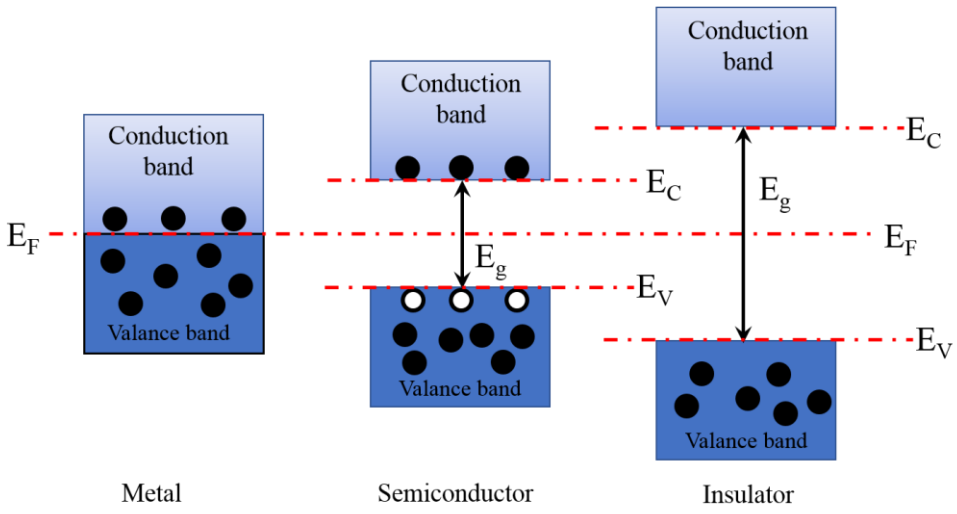

Fig.1. 2 Comparative energy band diagrams of metal, semiconductor, and insulator.

A wide variety of elements and compounds, particularly solids, can function as semiconductors. In semiconducting materials, two types of charge carriers are present: electron (negatively charged particles) and hole (positively charged particles). The number of charge carriers in semiconducting material can be modified by impurities called dopants. One considers intrinsic semiconductor material and extrinsic semiconductor material [14].

In intrinsic semiconductor material, also called un-doped semiconductor, the number of electrons and holes charge carriers are the same. To explain intrinsic semiconductors, we consider the example for silicon. Silicon has four valence electrons. In the crystal or lattice structure, each silicon atom has four neighboring atoms and shares one valence electron with each neighboring atom to make a bond (as shown in Fig.1. 3). These valence electrons are normally kept in place by the silicon atoms and cannot move through the crystal. Light or heat however can make them break free from the silicon atoms so they can move freely through the crystal. In other words, to promote conduction, the electron need to be taken into the conduction band via a thermal or optical or other form of excitation. As a result, an empty state (hole – missing of electron) is created in the valance band. Both the electron in the conduction band and the hole in the valence band are mobile and can move freely through the crystal. The concentration of electrons and hole depend on the temperature and is described by Fermi Dirac statistics. In intrinsic semiconductor the fermi level (E_F) lies at the middle of the bandgap (as shown in Fig.1. 6). Note that the intrinsic carrier concentration in Si is only on the order of 1×10^{10} cm^{-3}. So intrinsic silicon is highly resistive at room temperature.

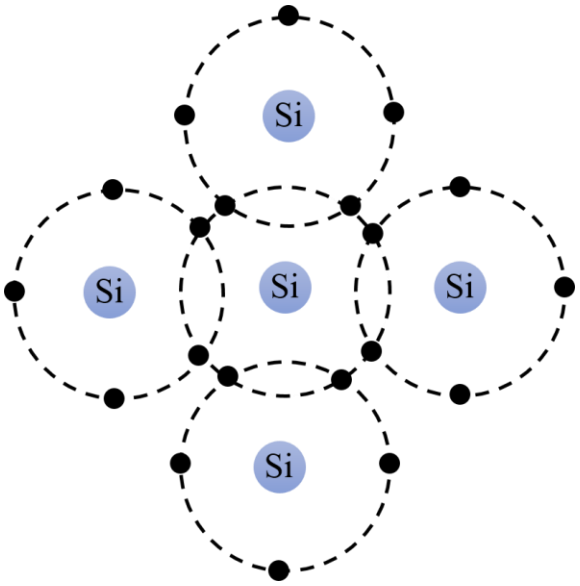

Fig.1. 3 The intrinsic semiconductor silicon and its electron distribution.

An extrinsic semiconductor, also called a doped semiconductor, is the one in which a foreign dopant atom in the crystal lattice provides charge carriers for the conduction process. This phenomenon is known as doping. Depending on the doping type, extrinsic semiconductors can be divided into two types: n-type and p-type semiconductors. When, an atom with five valance electrons is is incorporated in the silicon crystal, one of its valence electrons is only weakly bonded to the atom and it released as a mobile conduction electron into the crystal lattice. An extrinsic semiconductor, doped with atoms which can donate valance electrons, is called an n-type semiconductor. As each donor atom donates a free electron to the crystal, the charge carrier concentration is much higher for n-type silicon than for intrinsic silicon. And because of the electron donation by the donor atoms, most charge carriers in such crystal are negative electrons. To explain this, we consider again the example silicon (valency = 4) doped with pentavalent (valency = 5) atom phosphorous (for example) as shown in

Fig.1. 4. When phosphorous participate in the lattice structure with silicon, the fifth valence electrons become free to move around in the lattice and participate in the conduction process. The strength of doping depends on the amount of P atoms used in this doping. According to the Fermi-Dirac statistics, the fermi level (E_{Fn}) in n-type semiconductor move towards the conduction band as shown in Fig.1. 6.

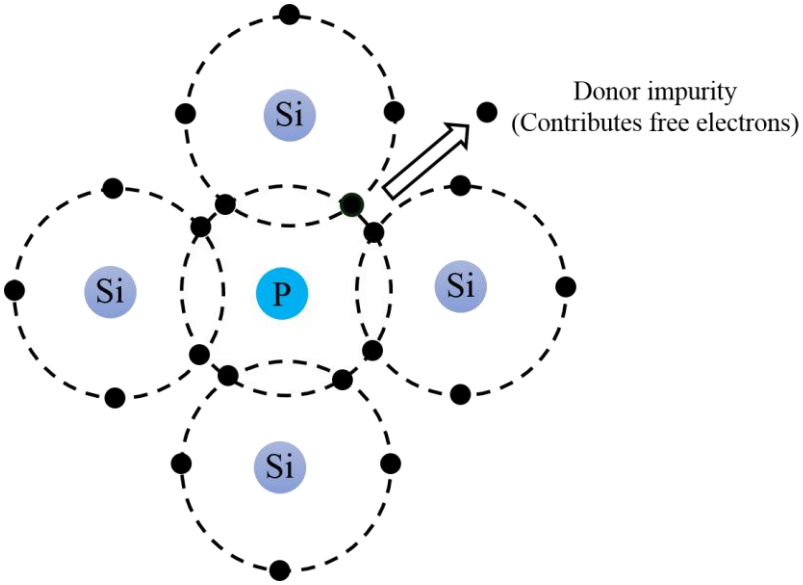

Fig.1. 4 Representation of n-type semiconductor using silicon (Si) which doped with pentavalent phosphorous (P) atom.

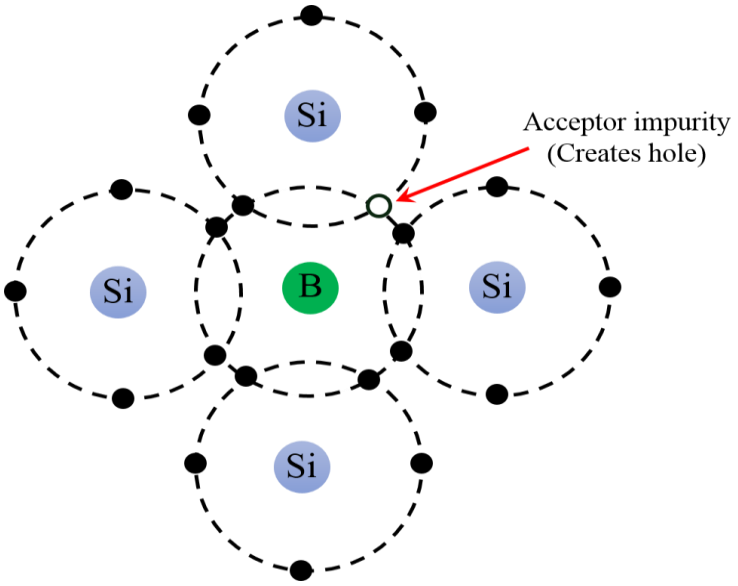

Fig.1. 5 Doping Si with tetravalent Boron (B) to form p-type semiconductor.

P-type silicon is created when the impurities are tri-valent. The impurity is one electron short to create the bonds with its neighboring silicon atoms. This vacancy is normally filled by an electron of a neighboring silicon atom. Such impurity atoms are called acceptors. When, an electron acceptor dopant atom is the one that accepts an electron from the lattice, it creates a vacancy (missing electron), called a hole, which can move through the crystal like a positively charged particle. This extrinsic semiconductor doped with electron acceptor atoms is called a p-type semiconductor and the majority of the charge carriers are holes. For example, in a silicon crystal (valency = 4) doped with an acceptor impurity, like boron (B) (valency = 3), there will be a shortage of valence electrons in the lattice structure (as shown in Fig.1. 5). According to the Fermi-Dirac statistics, the Fermi level of the intrinsic silicon moved towards the valance band (as shown in Fig.1. 6).

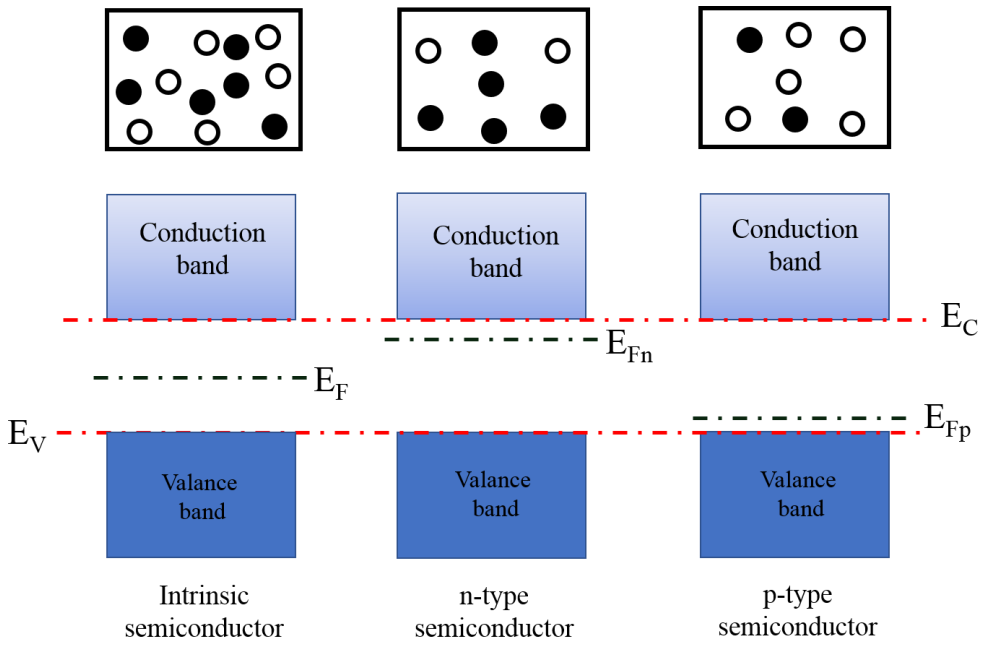

Fig.1. 6 Intrinsic, n-type, and p-type semiconductors and their energy band diagrams.

Doping is the key to the extraordinarily properties of semiconductor devices such as diodes, transistors, semiconductor lasers, light emitting diode devices, solar cells, and in integrated circuits. The level of doping, either with acceptor or with donor in semiconductors, determine the performance of these devices.

1.2.2 p-n Junction

When p-type and n-type semiconductor (i.e. silicon) are placed in contact with one another, a p-n junction is formed [14]. At this junction an interesting phenomenon occurs that it's the foundation of solid state physics devices. A basic p-n junction creates a diode that allows electricity to flow (drift and diffusion - Fig.1. 8) in one direction but not the other. The n-type material has free electrons and the p-type material has free holes, but near the p-n junction the electrons in the n-type material diffuse into the p-type

material and recombine with the vacant holes in the p-type material. So, in that junction area free electrons and holes annihilate each other causing the interface to be depleted of free electrons and free holes. The junction area is called the depletion zone [15]. This depletion zone is highly resistive as very little free electrons or free holes exist. The depletion area carries a charge caused by the ionized dopant atoms. The donor ions are positively charged since they have donated one of their valence electrons to the conduction band. The acceptor on the p-side of the junction are negatively charged since they accepted an electron from a neighboring silicon atom. This leaves a small electrical imbalance inside the diode that creates an internal electric field. When the junction is formed free electrons will diffuse from the n-side to the p-side and free holes will diffuse from the p-side to the n-side. So, the n-side will become positively charged and the p-side will become negatively charged. Fig. 1.7 shows a schematic diagram of the pn-junction under zero bias. It shows the free charge carriers on both sides of the junction and the ionized dopants atoms. The ionized donor and acceptor atoms cannot move. The minority charge carriers are not included in the figure. The depletion area does not contain free charge carriers but has a net charge. Fig. 1.8 shows the band diagram of the unbiased pn-junction.

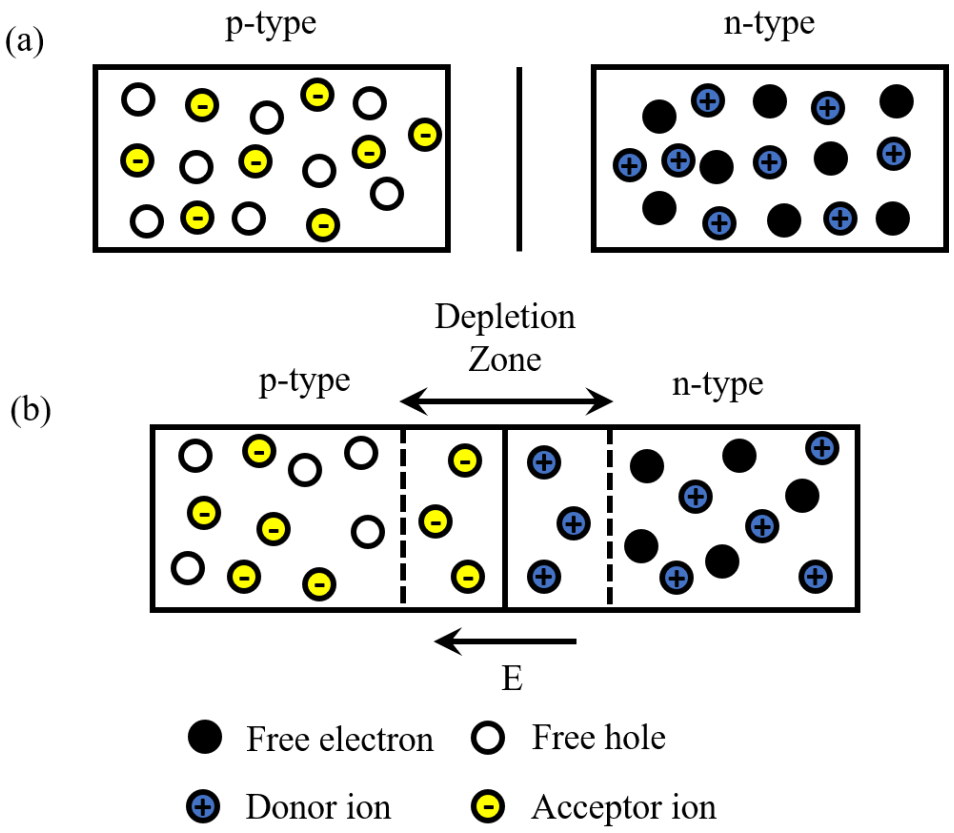

Fig.1. 7 P-N junction at equilibrium (with no applied bias).

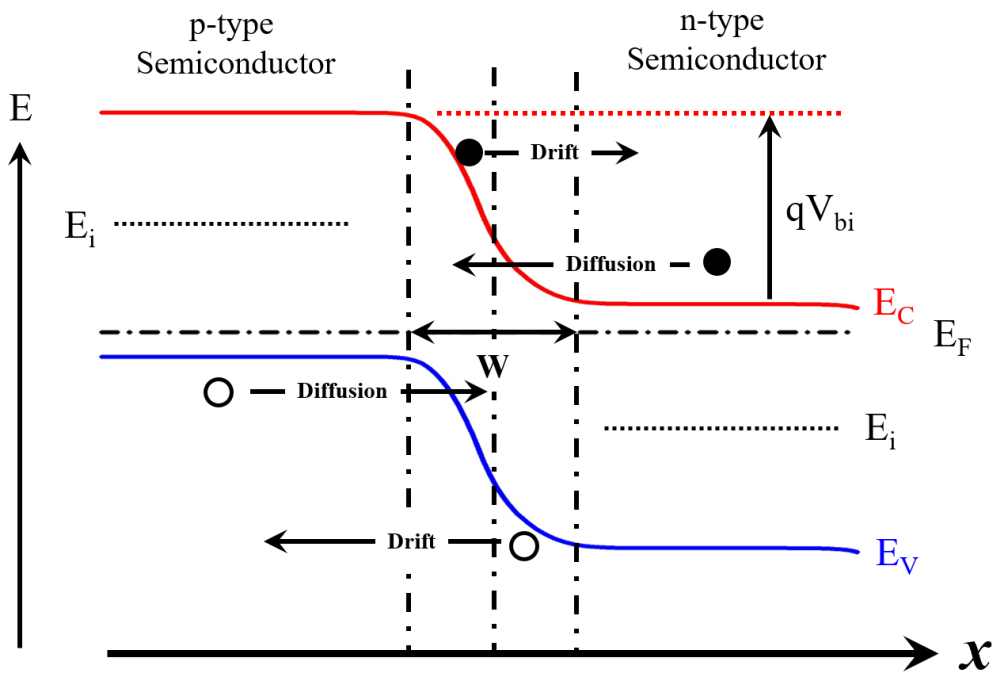

Fig.1. 8 Energy band diagram of the P-N junction at equilibrium (with no applied bias).

1.2.3 p-n Junction Under Forwards Bias

If the positive terminal of a voltage source is attached to the p-type region and n-type region is connected to the negative terminal (Fig.1. 9a) then the p-n junction will be forward biased [15]. The energy band diagram under forward bias is shown in Fig.1. 9(b). In this case, electrons from the n-type region are going to be pushed closer to the junction, and the holes are going to be repelled by the positive terminal towards the junction. This decreases the depletion area and the internal electric field. If the voltage pushing the electrons and holes has enough strength to overcome the depletion zone (usually around 0.7V for silicon), electrons and holes will combine at the junction and current passes through the diode.

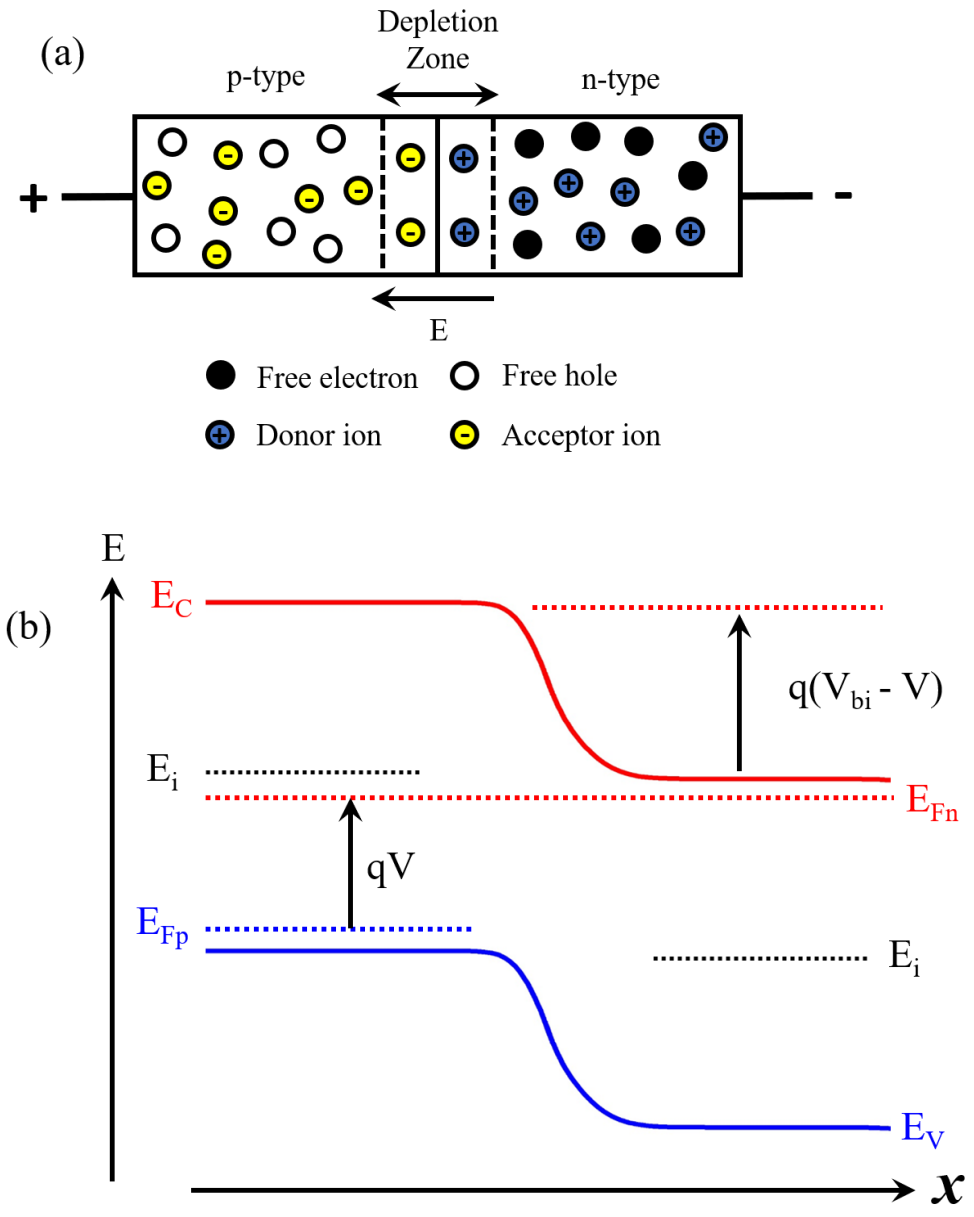

Fig.1. 9 (a) P-N Junction under forward bias (V = V), and (b) energy band diagram under forward bias.

1.2.4 p-n Junction Under Reverse Bias

Now if we connect the positive terminal of the voltage source to the n-type region and the negative terminal to the p-type region (as in Fig.1. 10a), the negative terminal attracts the positive holes in the p-type and the positive terminal attracts the free electrons in the n-type. All the free charge carriers are pulled away from the p-n junction which creates a larger depletion zone (energy band diagram is in Fig.1. 10b) and almost no current flows [15]. The internal electrical field at the junction is now larger.

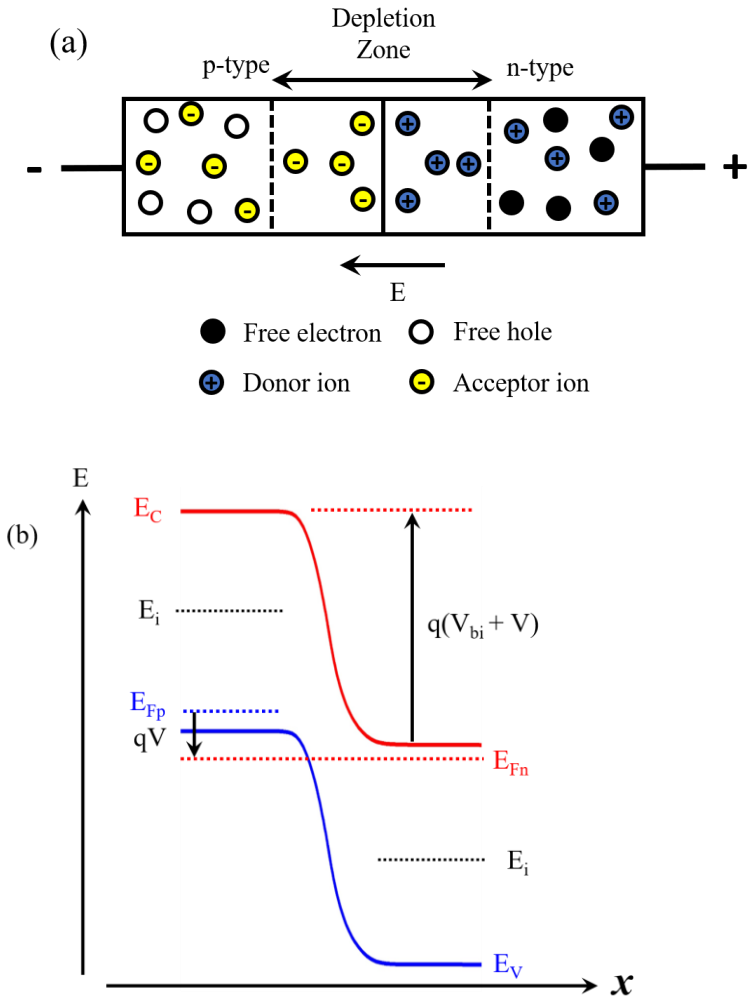

Fig.1. 10 (a) P-N Junction under reverse bias (V = -V), and (b) energy band diagram under reverse bias.

1.2.5 Solar Cells

Some types of diodes can generate DC all by themselves if enough IR, visible light, or UV energy strikes the P-N junctions. We call this property the photovoltaic effect [14]. We can see a solar cell as a p-n junction (a basic solar cell device - although several layer structure possible) with a large surface area. The n-type material is thin to allow light to pass to the p-n junction. Absorption of light [photon energy $\geq E_g$ (absorber bandgap)] in the solar cell absorber layer generates an electric current (this happens inside the depletion zone of the p-n junction as shown in Fig.1. 11). When a photon of light is absorbed by one of the atoms in the semiconductor material, it will dislodge an electron, creating a free electron and a free hole. If this happens in the depletion area, the free electron and the free hole will be separated by the internal electric field in the depletion area. If this happens outside the depletion area two things can happen: (1) there is a chance that the free electron and free hole diffuse into the depletion area. If this happens the hole and electron are separated by the internal electric field present in the depletion area and contribute to the photon current; (2) the free electron and free hole recombine before they are separated from each other. If this happens, they will not contribute to the photon current. If a wire is connected from the cathode n-type material to the anode p-type material, electrons will flow through the wire creating a flow of current. The bias application in solar cell device is like as explained in p-n junction under forward and reverse bias.

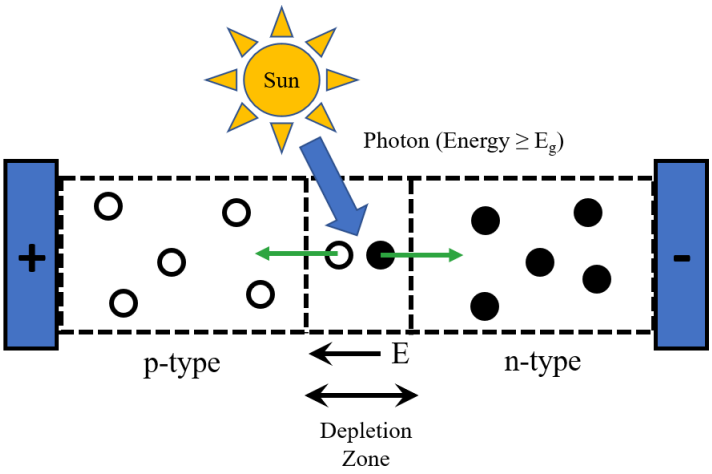

Fig.1. 11 P-N Junction Solar Cell.

1.2.6 Metal Semiconductor Junction

Like p-n junctions, metal-semiconductor junctions are also very important in semiconductor device physics. Contact formed by metal and semiconductor material are two types: Schottky contacts and Ohmic contacts.

1.2.6.1 Schottky Contact

Fig.1. 12(a) and (b) shows the enegy band diagram (at thermal equilibrium) for Schottky contact when a metal is adjucent to a n-type semiconductor and when it makes contact with the n-type semicondcutor respectively. The contact fromed here is the Schottky type contact. A Schottky contact is formed when the metal work function is larger than the semiconductor work function ($\phi_M > \phi_S$). For a Schottky type contact, a barrier exists and electrons can not freely flow from the metal to the n-type semiconductor. One refers to this barrier as the Schottky barrier. If the barrier height $\phi_B > k_B T$, the junction will be rectifying and have different IV characteristics for positive and negative voltages. The potential barrier between the metal and the

semiconductor can be identified on an energy band diagram (electron suffers this barrier to reach the contact to be collected). The barrier height ϕ_B is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carrier resides. From Fig.1. 12(b), one finds that for n-type semiconductor the Schottky barrier height is given by

$$\phi_B = \phi_M - \chi \qquad (1.\ 1)$$

Here, ϕ_B is the barrier height, ϕ_M and χ are the metal's work function and the electron affinity respectively.

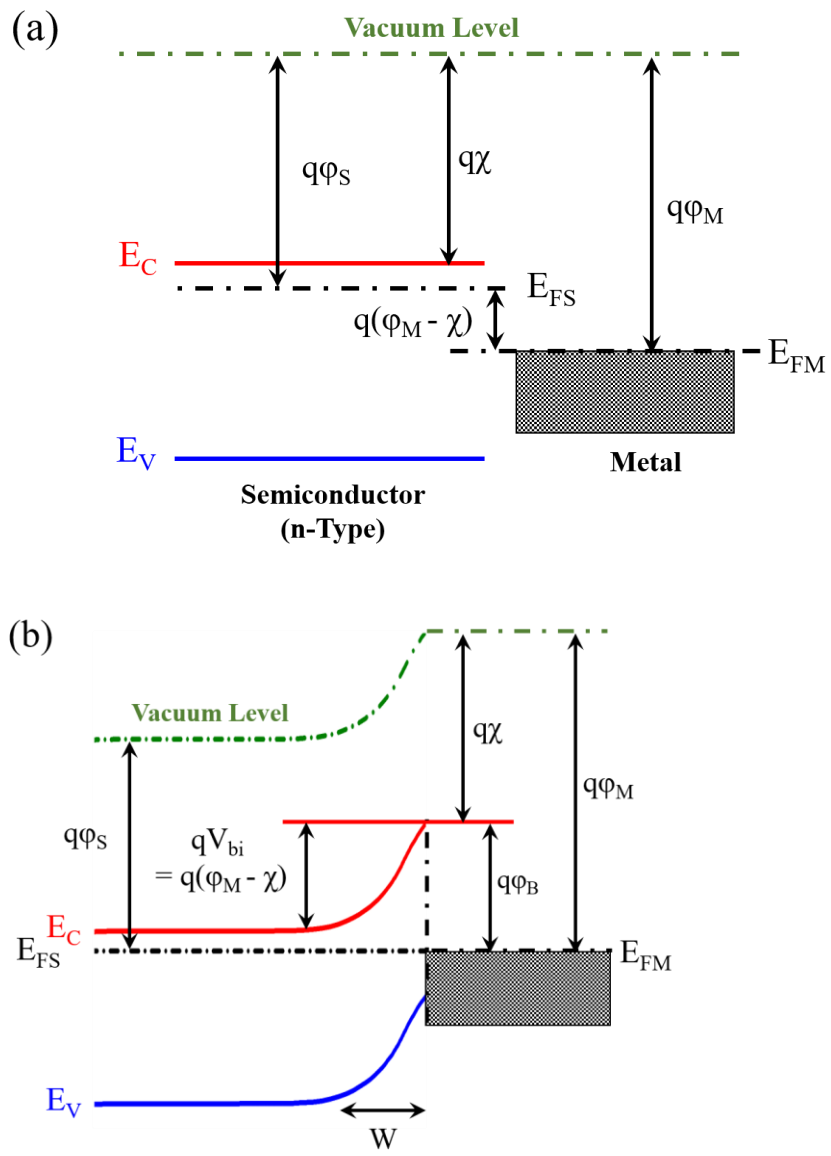

Fig.1. 12 Energy band diagrams for Schottky contact: (a) a metal adjacent to n-type semiconductor under thermal noneqilibrium, and (b) metal semiconductor contact in thermal equilibrium. The symbols are explained in the text.

1.2.6.2 Ohmic Contact

An ohmic contact is defined as a metal-semiconductor contact that has a negligible contact resistance relative to the bulk or series resistance of the semiconductor. Fig.1. 13(a) and (b) shows the enegy band diagram for Ohmic contact (at thermal

equilibrium) when a metal is adjucent to a n-type semiconductor and in contact with the n-type semicondcutor respectively. For an Ohmic to fulfilled that metal work function should be less than the semiconductor work function ($\phi_M < \phi_S$). In case of Ohmic contact an electron does not face any potential barrier when flowing through the contact.

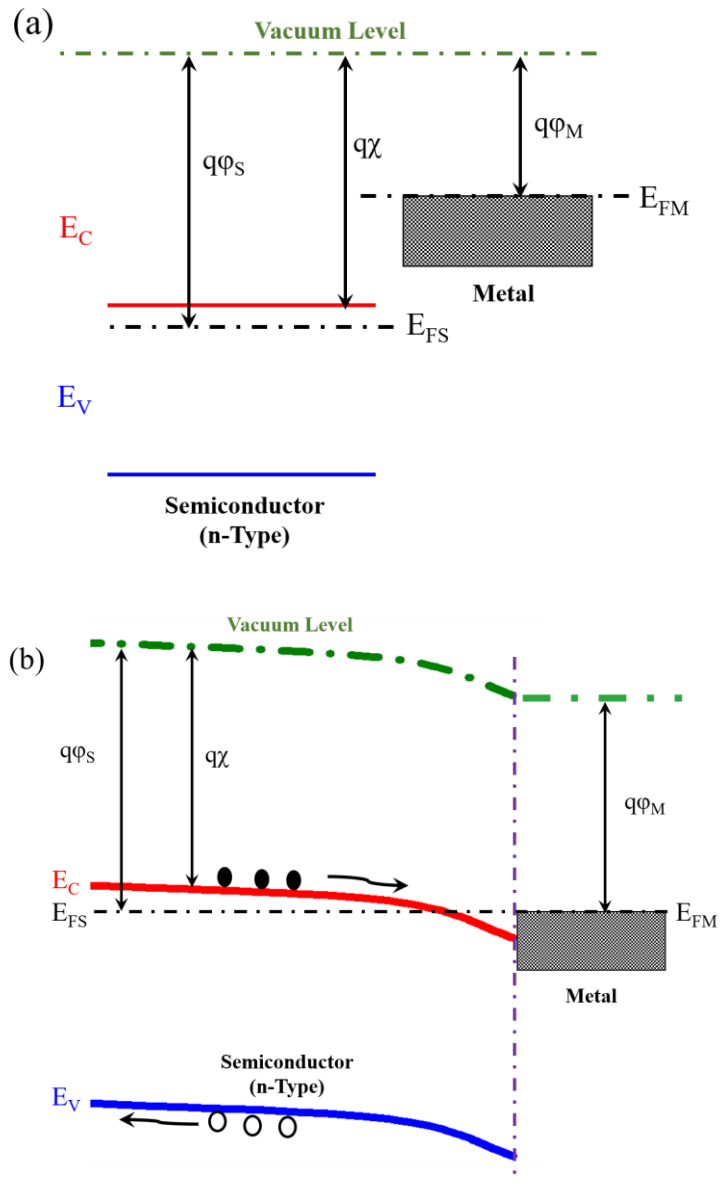

Fig.1. 13 Energy band diagrams for Ohmic contact: (a) a metal adjacent to n-type semiconductor under thermal noneqilibrium, and (b) metal semiconductor contact in thermal equilibrium. The symbols are explained in the text.

1.3 Characterization Methods

Capacitance techniques such as capacitance-voltage measurement, DLTS (Deep-level Transient Spectroscopy) and admittance spectroscopy, monitor the movement of electronic charge within a semiconductor device and provide a measure of free carrier and electrically active defect state properties. Capacitance is the charge storage capacity and is measured across a rectifying junction.

1.3.1 Solar Cell Device Performance Characterization

The commonly used term on the performance of solar cell is the efficiency which is the measure of the ratio of energy output from the solar cell to input energy from the sun. For standard characterization, solar cell performance is tested under AM1.5 (P_{in} = 100 mW/cm^2) conditions and at a temperature of 25°C. The efficiency (η) of a solar cell is given by the formula

$$\eta = \frac{V_{OC} J_{SC} FF}{P_{in}} \times 100\% \qquad (1.\ 2)$$

Here, V_{OC} = Open-circuit voltage (point where the current is zero), J_{SC} = short-circuit current density (current density at V = 0) as pointed in Fig.1. 14 (the dark and light JV characteristics). The fill factor (FF) is defined as

$$FF = \frac{V_m J_m}{V_{OC} J_{SC}} \times 100\% \qquad (1.\ 3)$$

The concept of the FF can be understood from the power curve shown in Fig.1. 14. The curve's minima touches the light JV curves at (V_m, J_m). The FF factor is defined as the ration of the shaded area between x-axis and negative y-axis and V_{OC}×J_{SC}. through point (V_m, J_m) to the same through point (V_{OC}, J_{SC}). In other words, the FF is a measure of the "squareness" of the solar cell's J-V curve under illumination. Note that (V_m,J_m) is the point on J-V curve with maximum power output.

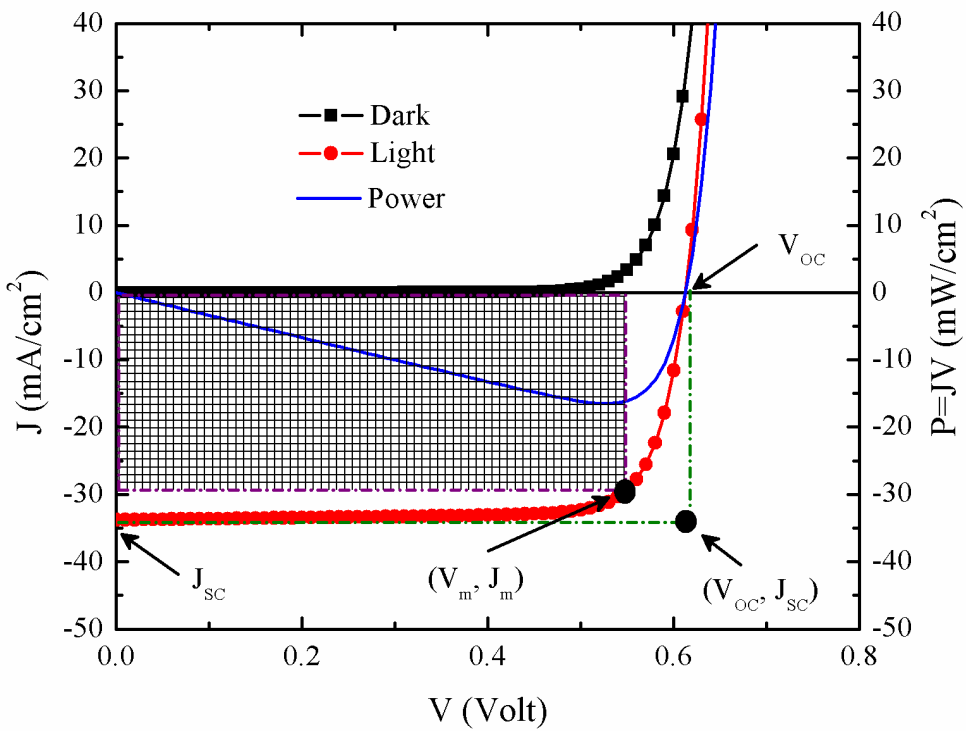

Fig.1. 14 The dark and light JV characteristics (left y-axis) and the power curve (right y-axis) of a solar cell. These curves were generated using SCAPS-1D program [16] with Numos CIGS baseline structure at 300 K and under one sun (100 mW/cm^2) illumination.

1.3.2 Capacitance-voltage Measurement

The capacitance voltage (C-V) measurement technique [14], [15] is usually performed in diode-based devices (for example, Schottky diodes or solar cells), to investigate the semiconductor's properties and the properties of the device. The C-V

measurement determines the concentration of majority carriers in the bulk of the device by applying a bias voltage and measuring current the capacitance. To understand this better we can assume that we connect a capacitor to an alternating (AC) voltage source (Fig. 1.4)

$$V(t) = V_0 Sin(\omega t) \tag{1. 4}$$

Consequently, the current can be calculated from $I = dQ/dt = d(CV)/dt = CdV/dt$ and is given by

$$I(t) = C\frac{dV}{dt} = C\omega V_0 Cos(\omega t) \tag{1. 5}$$

So, the current is 90 degrees out of phase from the voltage

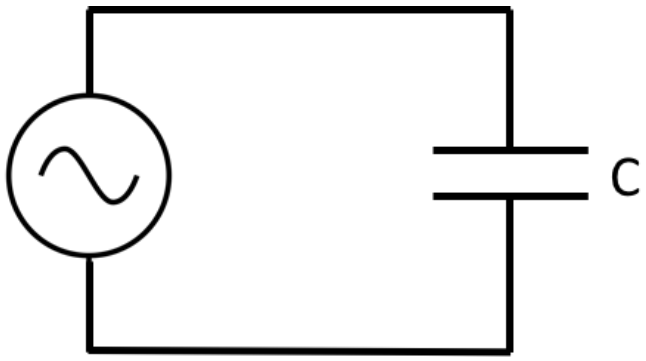

Fig.1. 15 Capacitor connected to an AC voltage source.

For a diode, we have a charge separation due to the depletion region that has a capacitive effect in addition to the reverse bias resistance. So, the model of Fig.1. 15 is too simple. Fig.1. 16 shows how our more advanced diode model would look like.

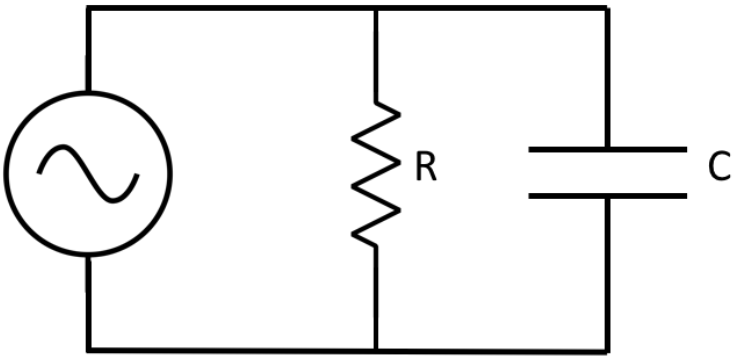

Fig.1. 16 Simple model of diode.

The application of an alternating voltage $V(t) = V_0 \sin(\omega t)$ will now result in current that can be written as

$$I(t) = I_0 Sin(\omega t + \phi) \qquad (1.\ 6)$$

with $\phi -$ the phase angle which is no longer 90 degrees. As we mention before, in a n-p junction the depletion region is fully depleted of free carriers, and the bulk region is neutral. Also, when we apply an ac or dc bias, the only change in charge occurs at the edge of the depletion zone (Fig.1. 17).

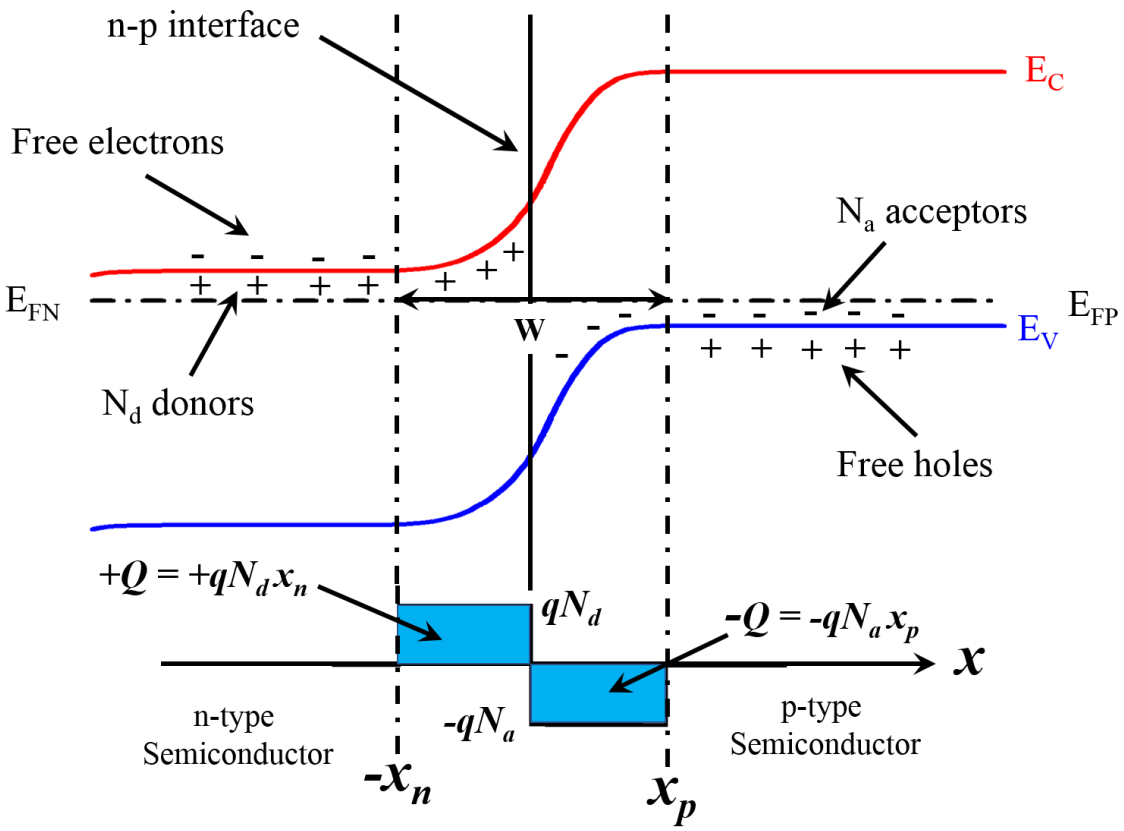

Fig.1. 17 n-p junction band diagram and charge distribution.

So, we can assume a n-p junction, where the depletion region extends a distance x_p into the p-region, and x_n into the n-region as shown in Fig.1. 17. The donor concentration in the n-type material is given by N_d, and the acceptor concentration in the p-type materials is given by N_a. Because the charge on one side of the depletion region must be equal in magnitude but opposite to the sign on the other side of junction, we can write

$$x_p N_a = x_n N_d \qquad (1.7)$$

Now, according to the Gauss' Law,

$$\vec{\nabla} \cdot \vec{D} = \rho \tag{1. 8}$$

where, D is the electric displacement (D = εE, E is the electric field and ε the permittivity of the material). So, in one dimension, Gauss's law reduces to

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon} \tag{1. 9}$$

Now, we know that $E = -\frac{dV}{dx}$ and that inside the depletion region $\rho = qN_a$ for the p-region and $\rho = qN_d$ for the n-region, where q is the elementary charge. The maximum value of the electric field across the depletion region is found to be at x = 0, the position of the junction:

$$E_{\max} = -\frac{qN_a x_p}{\varepsilon} = -\frac{qN_d x_n}{\varepsilon} \tag{1. 10}$$

The voltage between x = 0 and x = x_p is given by

$$V_1 = -\int_{-x_p}^{0} E dx = \frac{qN_a {x_p}^2}{2\varepsilon} \tag{1. 11}$$

Similarly, the voltage between the point x = 0 and x = x_n is given by

$$V_2 = -\int_{0}^{x_n} E dx = \frac{qN_d {x_n}^2}{2\varepsilon} \tag{1. 12}$$

So, we can write in terms of built-in potential (V_{bi}) and externally applied voltage (V)

$$V_{bi} - V = V_1 + V_2 = \frac{q}{2\varepsilon(N_a {x_p}^2 + N_d {x_n}^2)} \tag{1. 13}$$

Now, using the condition as in equation (1. 7)

$$V_{bi} - V = \frac{q x_n^{\,2} N_d^{\,2}}{2\varepsilon\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{1. 14}$$

If $N_d >> N_a$, and the condition $x_p N_a = x_n N_d$, equation (1. 14) reduces to

$$V_{bi} - V = \frac{q x_p^{\,2} N_a}{2\varepsilon} \tag{1. 15}$$

Then:

$$x_p = \sqrt{\frac{2\varepsilon(V_{bi} - V)}{q N_a}} \tag{1. 16}$$

Now, since $x_p \approx W$ (the width of the p side region), then we can write

$$W \approx \sqrt{\frac{2\varepsilon(V_{bi} - V)}{q N_a}} \tag{1. 17}$$

This is in agreement with Fig.1. 7, Fig.1. 9, and Fig.1. 10: in reverse bias (negative V) the width of the depletion zone is larger than in forward bias. Now, as we discussed before, with $C = \frac{dQ}{dV} = \frac{\epsilon A}{W}$, we can write

$$\frac{1}{C^2} = \frac{2}{q N_a \varepsilon A^2}(V_{bi} - V) \tag{1. 18}$$

The above equation is known as the Mott-Schottky equation. Using experimental CV data and a Mott-Schottky plot ($\frac{1}{C^2}\ vs.V$), we can estimate the values of N_a and V_{bi} from the slope $\left(= -\frac{2}{q\epsilon N_a A^2}\right)$ and intercept $\left(= -\frac{2}{q\epsilon N_a A^2}V_{bi}\right)$ respectively. One of the most conventional way to estimate the value of N_a is to consider the differential capacitance spectra and in this case the estimated value of $N_a = N_{CV}$ (N_{CV} here stands for the value of N_a estimated via CV method) is

$$N_{CV} = -\frac{2}{q\varepsilon A^2}\left(\frac{d(1/C^2)}{dV}\right)^{-1} \qquad (1.\ 19)$$

1.3.3 Admittance Spectroscopy Measurement

The admittance spectroscopy technique is a well-known technique used to study defects or traps in semiconductor materials (with either semiconducting device such as Schottky diode or p-n junction or solar cells). In defect studies using admittance spectroscopy, we can determine the energetic location of the traps (defects), their capture cross-section, and their concertations. The series resistance in the material underlying the Schottky or p-n junction is also detected when the free carriers are freezing out. Also, utilizing the carrier freeze-out phenomena we can estimate the semiconductor layer thickness in Schottky devices or the thickness of absorber in solar cell devices. In addition, utilizing the bias dependent depletion width, the temperature dependent admittance spectroscopy is a great tool to study resistivity/conductivity, charge carrier mobility, and hence charge transport properties.

Admittance spectroscopy [17] involves the measurement of complex admittance (Y) which is the combination of capacitance and conductance in terms of temperature (T) and frequency (ω), i.e.,

$$Y(T,\omega) = i\omega C(T,\omega) + G(T,\omega) \qquad (1.\ 20)$$

In admittance spectroscopic measurements, we apply an ac signal (V_{ac}) superimposed with the applied dc bias ($V = V_{dc}$) on the devices (pictorial representation is in Fig.1. 18) and measured admittance as function of temperature and applied bias Conventionally, we use the ac signal (peak-to-peak) value to $\frac{k_B T}{q}$ ~ 30 mV.

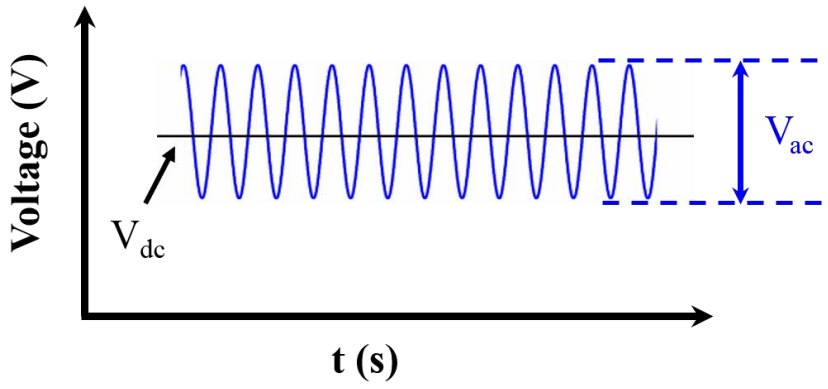

Fig.1. 18 Schematic representation of the ac signal (V_{ac}) used in admittance spectroscopy which is superimposed on the applied dc bias (V_{dc}).

For a p-n junction (containing shallow donors and acceptors only), the space charge region (SCR) width will determine the capacitance in the device while the majority carriers can respond to the ac frequency $\omega = 2\pi f$ (f is the linear frequency) and the temperature T. The characteristic frequency of the carrier response is related to the

dielectric relaxation frequency (ω_D) or time (τ_D) as (also to the conductivity of the materials σ):

$$\omega_D = \frac{2\pi}{\tau_D} = \frac{\sigma}{\varepsilon} \tag{1. 21}$$

A trap charge can respond to low frequencies, but it cannot respond to high frequencies, where high and low frequencies are determined by the trap's relaxation time. Because of this, traps contribute to the low frequency capacitance (but not to the high frequency) and trap distributions can be extracted from measurements of capacitance versus frequency. The admittance spectroscopy measurement characterizes defect levels by measuring capacitance while varying frequency and temperature. The utilization of the admittance spectroscopy in studying defects and charge transport properties will be discussed in chapter 3 and 4 respectively.

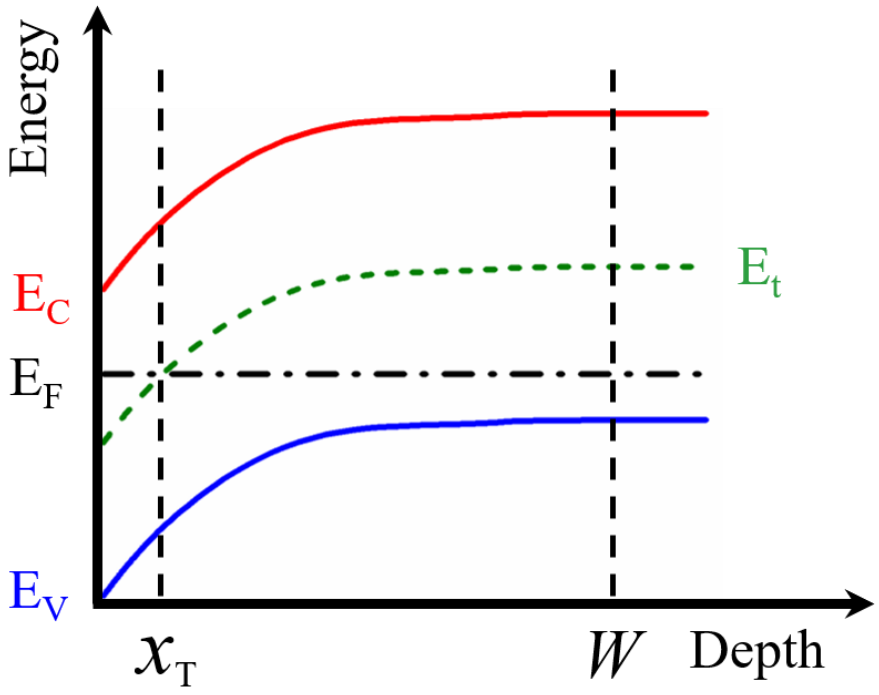

Fig.1. 19 Energy band diagram present in admittance spectroscopy in semiconductor materials and devices.

Depending on the temperature and frequency, capacitance steps commonly observed (capacitance response in function of frequency and temperature will be discussed in detail in chapter 3 and 4) due to the charging and discharging of defect at a location where the trap energy level E_t of electron (hole) traps crosses fermi level (as shown in Fig.1. 19). The characteristic frequency for this capacitance response is related to the thermal emission depth Ea of the defect and can be expressed by the following equation

$$\omega_0 = 2N_{CV}v_{th}\sigma_t \exp\left(-\frac{E_a}{k_B T}\right) \qquad (1.\ 22)$$

Here, $N_{C,V}$ is the effective density of states of the valance band, v_{th} is the average thermal velocity, σ_t is the capture cross section of the defect, and E_t is the energetic location of defect level. The expression of effective density of states and the thermal velocity are $N_{C,V} = 2\left(\frac{2\pi m^* k_B T}{h^2}\right)^{3/2}$ and $v_{th} = \left(\frac{3k_B T}{m^*}\right)^{1/2}$. Where, m^* is the effective mass of majority carrier (i.e., hole). So the temperature dependent of $N_{C,V}$ and v_{th} can be factored out to leave T^2 dependent and hence the peak frequency expression results in $\omega_0 = \xi_0 T^2 \exp\left(-\frac{E_a}{k_B T}\right)$. The trap capture cross-section, σ_t, can be estimated from the temperature independent pre-factor: $\xi_0 = \frac{4m^* \pi \sqrt{6\pi}}{h^3}\sigma_t$.

II. RESEARCH INSTRUMENTATION AND EXPERIMENT SETUP

2.1 Introduction

The development of the experimental set up is the part of this thesis work. The experimental set up is for the temperature dependent electrical characterization of electronic materials and devices. The temperature dependent electrical measurement set up allows for current-voltage (IV), capacitance-voltage (CV), and the admittance spectroscopy (AS) measurements. The setup includes data acquisition software written in LABVIEW [18]. Below a description of the different components used to build the complete set up is given.

2.2 Instrumentation

2.2.1 ARS Cryogenic Probe Station [18]

This probe station (Fig.2. 1) has 4 probe manipulators capable to displace 2 inches on X, Y and Z directions. Two of the probes have been customized with a small ball on the tip to create a soft contact while working between low temperature and room temperature. An electronic microscope is used to contact the device.

The chamber is capable to support a wide range of temperatures (this chamber has been tested between 6 K to 800 K). To heat the chamber, the system has 2 heaters inside which can work either simultaneously or independent.

To cool down a cryogenic system consisting of a compressor, a cryogenic pump and helium lines is used. The compressed helium flows from the compressor into the motor driven multistage piston assembly located inside the cryogenic pump, and as it moves, the helium expands and gets colder. As the piston returns, the helium is pushed

out of the cryogenic pump and is returned to the compressor. Here it is re-compressed and heat is disposed into the lab. After this, the cycle repeats. Heat is removed during every cycle until the minimum temperature, 6K, is reached.

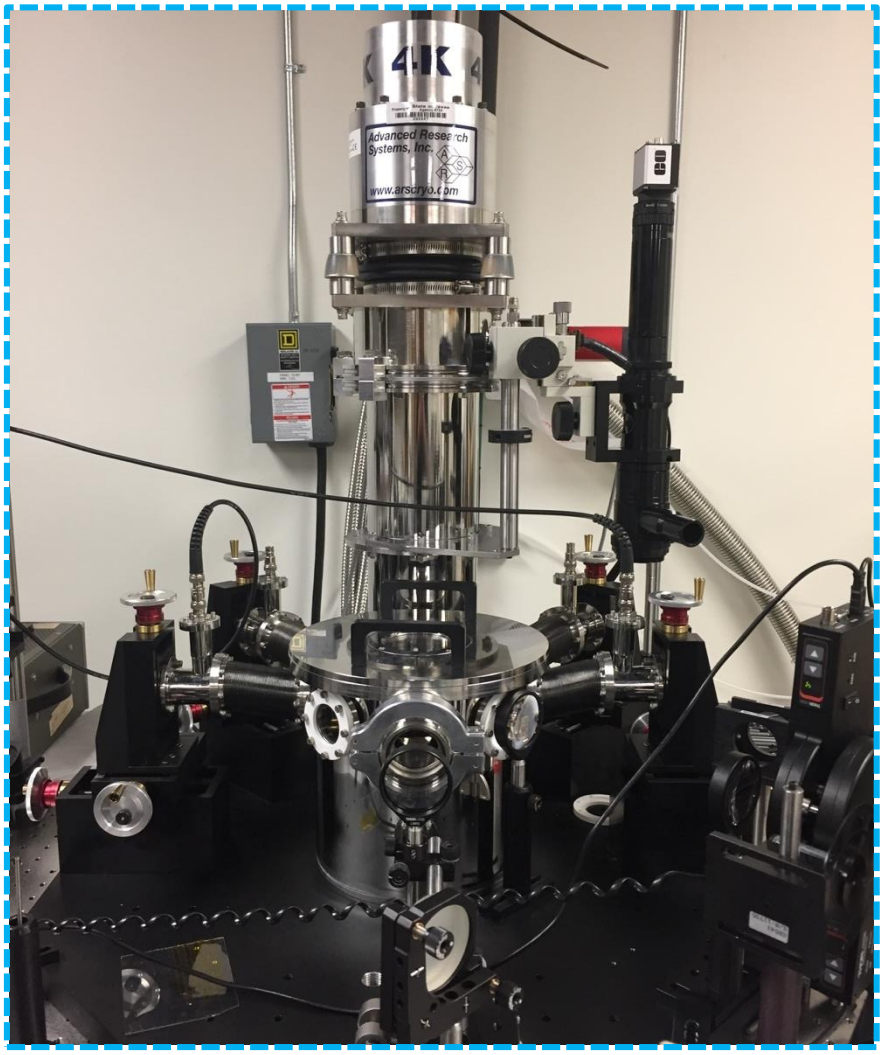

Fig.2. 1 ARS Cryogenic Probe Station used in this research for temperature dependent electrical characterization.

2.2.2 Keysight E4990A Impedance Analyzer

This impedance analyzer (Fig.2. 2) possesses 4 channels with the possibility to use up to 4 traces per channel (each one of them represent a different measurement in the same sweep). With 10 independent markers per trace, to the capability to collect 1601 data points, a tunable measurement speed option, 17 measurement parameters, a frequency operation range between 20 Hz and 20 MHz, a basic impedance accuracy of 0.045%, a four terminal pair measurement type, a built-in DC bias source of +/- 40 V with a 1 mV resolution and the capability to get data while sweeping frequency, signal voltage/current or DC bias voltage/current this device makes a perfect addition to our system. The system contains with GPIB, USB and Ethernet communication interfaces as well as a very useful I/O port.

In this thesis work, this impedance analyzer was used to sweep frequency and DC bias while keeping a constant AC voltage to measure capacitance, conductance, and or admittance. This process will be explained with more detail in this chapter in the Data Acquisition section.

Fig.2. 2 Keysight E4990A Impedance Analyzer (Used to sweep Frequency and DC Bias to collect Capacitance and Conductance).

2.2.3 Keysight B2912A Precision Source/Measure Unit (SMU)

This unit (as shown in Fig.2. 3) supports a two channel configuration and it is capable to source and measure both, voltage and current. Current and voltage resolution are respectively 10 fA and 100 nV. It has a maximum output capability of 210 V, 3 A DC, and 10.5 A in pulse mode. It comes with GPIB and USB interface.

In this work, the source measurement unit (SMU) will be used to measure the IV (current vs voltage) characteristics of the samples.

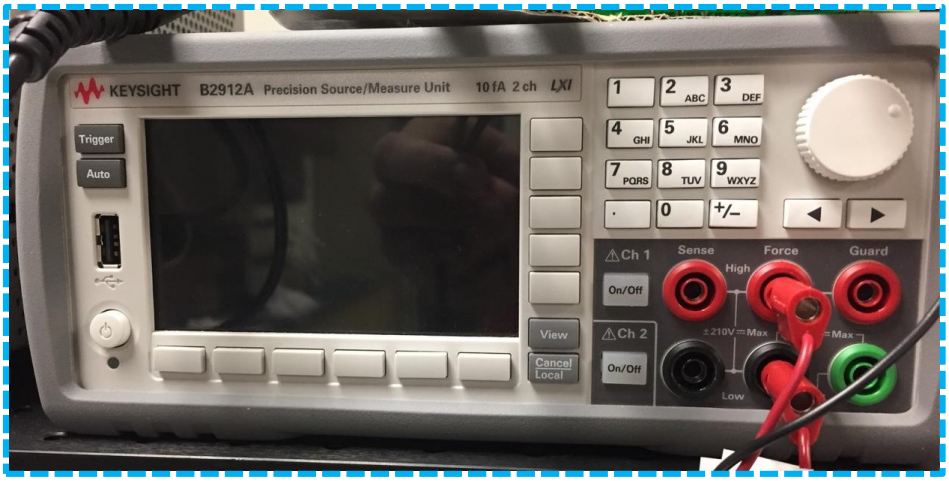

Fig.2. 3 Keysight B2912A Precision Source/Measure Unit (Used to measure the IV characteristics of the photovoltaic devices).

2.2.4 Lakeshore 336 Temperature Controller

This temperature controller model (as in Fig.2. 4) has four sensor inputs, four control outputs and 150 W of low noise heater power. It is capable to control two heaters independently providing up to 100 W and 50 W through two outputs which can be associated with any of the four sensor inputs and programmed for closed loop temperature control in PID (proportional-integral-derivative) mode. It supports the most advance cryogenic temperature sensors used by industry, such as diodes, RTDs (resistance temperature detectors) and thermocouples. It is capable to control and measure temperatures from 300 mK to 1500 K and it can switch automatically between temperature sensor inputs when one of them goes beyond its range. It also counts with alarms, relays and a +/- 10 V analog voltage output to help automate if secondary control functions are needed. It comes with Ethernet, USB and GPIB interfaces.

In this work, this temperature controller will be measuring and controlling the temperature inside the chamber to allow us to characterize the sample at different temperatures.

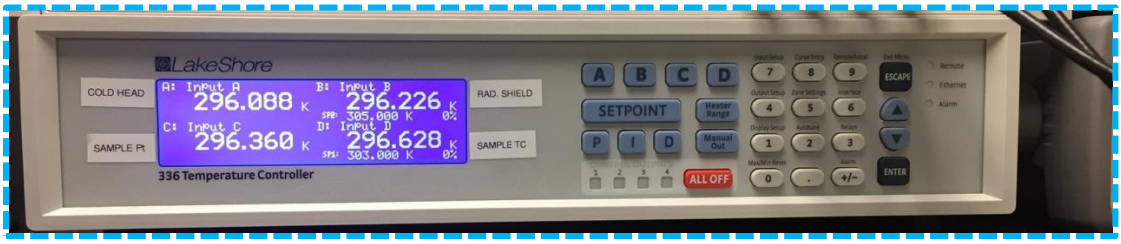

Fig.2. 4 Lakeshore 336 Temperature Controller. Used to set up the temperature at which the measurements are taking place.

2.3 Automation Design

2.3.1 Hardware

We have two characterization instruments that are going to be performing measurements on the device. The ideal scenario would be to make these measurements simultaneously without interfering one to another (this would guaranty both measurements are done at exactly the same conditions). While we know this is not possible, we know that the only condition changing inside of the chamber is the temperature. So, if we are fast enough to perform the experiment in after each other, the temperature should not change a lot between both measurements. So, electrons needed to be designed that would allow one to connect two measurement setups using two connectors to one device. To solve this issue, we created a switch matrix: a device capable of switching between multiple inputs and outputs (Fig.2. 5).

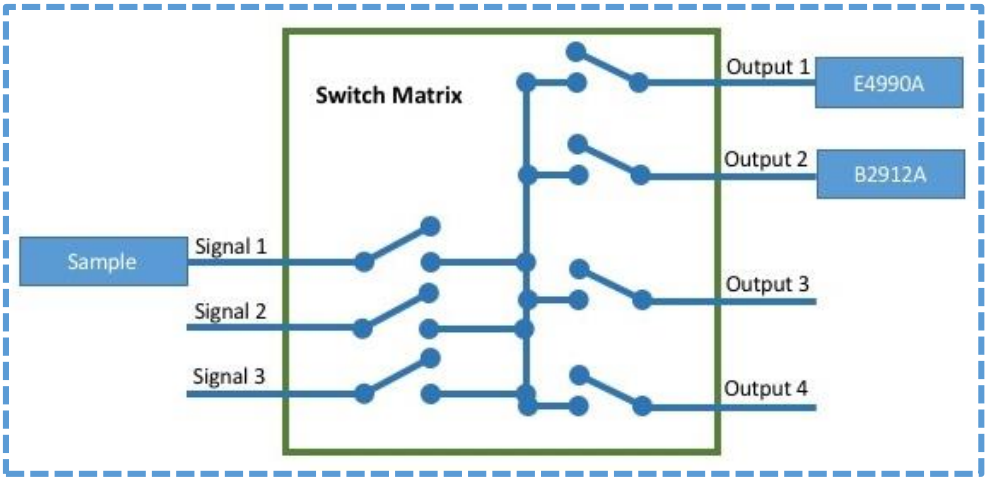

Fig.2. 5 The Switch Matrix. This circuit is able to connect different inputs to different outputs and thus modify the measurement setup.

In order to not to have to switch manually the circuit, we use as our input the same port that the impedance analyzer is using, that way we can make a program to control it through the impedance analyzer and we would not need to use another port from the computer. Since the impedance analyzer has port a, b, c and d, and all of them are communicated through the same connector, we added the I/O connector to our circuit design in order to not to eliminate these ports from the E4990A for future use.

This impedance analyzer also has the peculiarity of being on low input mode, which means that when the bit is high, the pin will measure 0V, and when the bit is low, it will measure 5V. We made sure the design would not require the person who is programing the instrument to know this and made the circuit to be low input too (to take 0V as high and 5V as low).

Using ExpressSCH, we created a schematic of the circuit (Fig.2. 6). We choose to use this program because it is free and created by the company that we chose to fabricate the PCB. Express PCB provided by the same company was used to create the PCB (see

Fig.2. 7). After receiving the circuit from ExpressPCB, we soldered the components and tested the circuit. The realized board is displayed in Fig.2. 8.

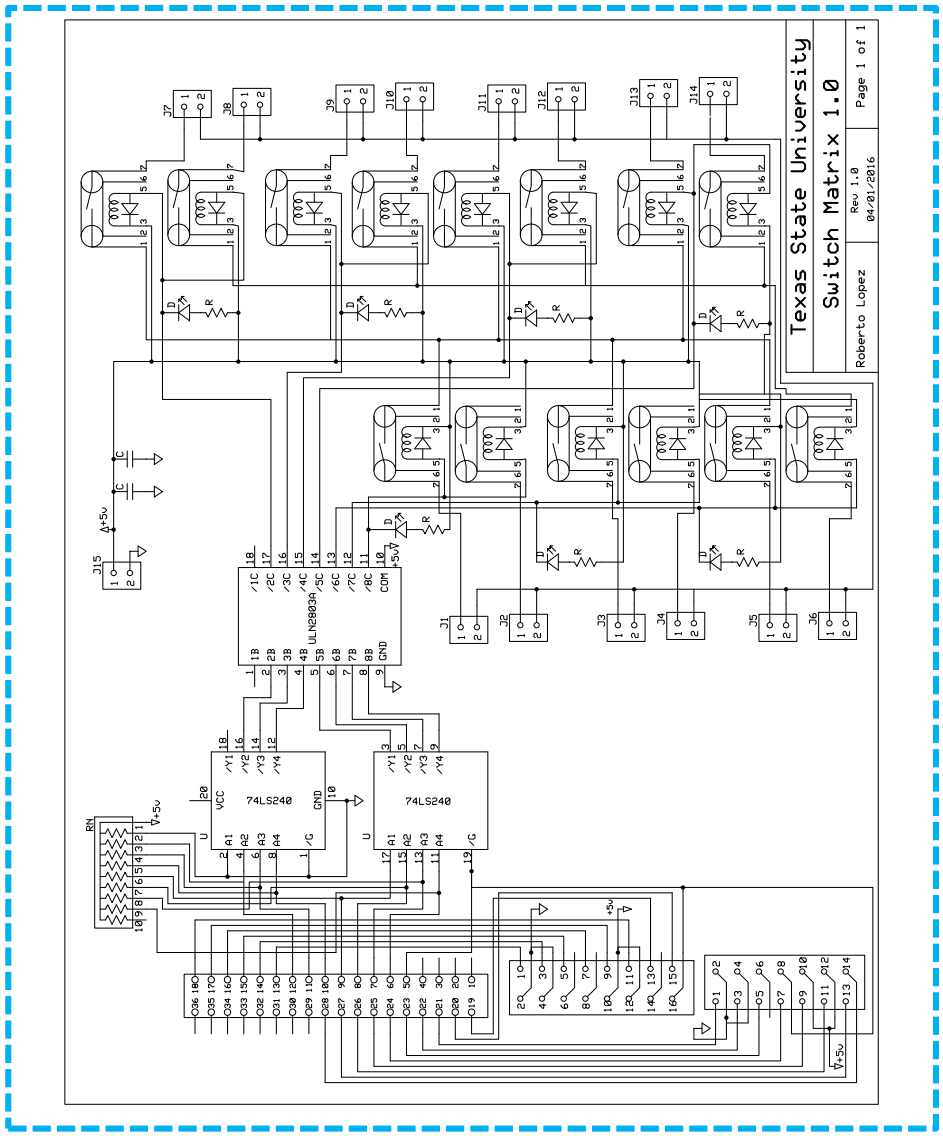

Fig.2. 6 Schematic of Switch Matric created in ExpressSCH.

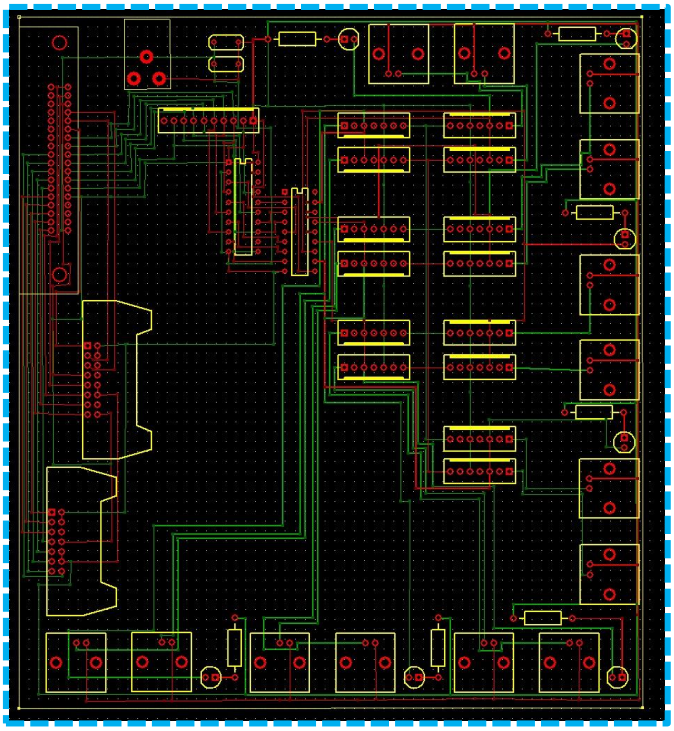

Fig.2. 7 Switch Matrix PCB in ExpressPCB.

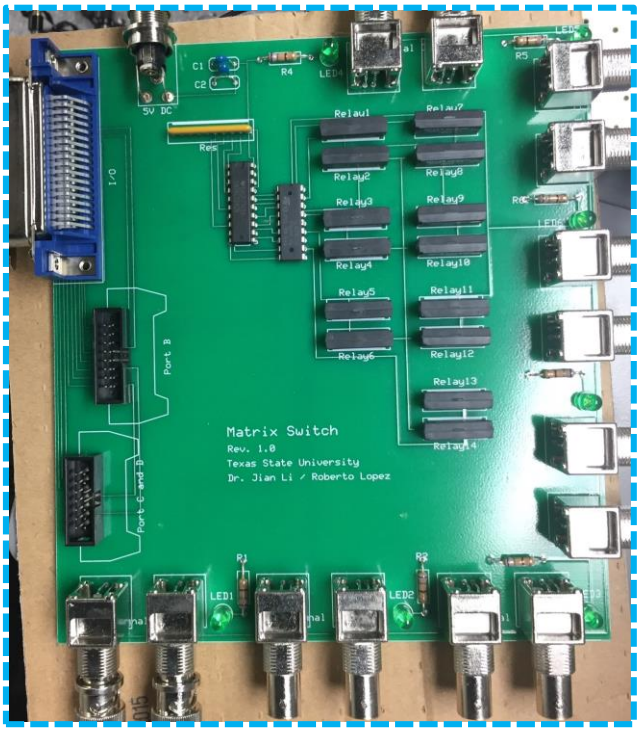

Fig.2. 8 Actual Switch Matrix (developed).

2.3.2 Software

A program was created in LABVIEW to control the developing switching matrix and switch between instruments. Other tasked performed by the Labview program included to set the parameters for the measurements (measurement conditions) and acquire and store the data it in a standardized format for analysis. The developed program is capable to switch between instruments according to the requested measurements. It sweeps frequency, DC bias and temperature while collecting capacitance and conductance data for an admittance spectroscopy measurement, and it sweep voltage and collect capacitance for a C-V measurement. To see details of this program, please refer to Appendix A in this document.

III. ELECTRICAL CHARACTERIZATION AND CHARGE TRANSPORT STUDIES IN CIGS SOLAR CELL

3.1 Introduction

Coper-Indium-Gallium-Selenide (CIGS) [19]–[21] is one of the high efficiency solar cell absorber materials and currently being considered for application in novel thin film photovoltaic devices. Other materials being considered for absorber in thin film PV devices are CdTe [22], and CZTSe [23] [24], [25]. The efficiency of the CIGS solar cell reported to date is 22.6% [26]. When combined in proper ratios, Copper, Indium, Gallium and Selenium form a semiconductor material that can be used as an absorber in the manufacturing of thin film solar cells [27]. The crystal structure of CIGS is a I-III-VI tetragonal chalcopyrite (Fig.3. 1), derived from zinc blende structure. This is a diamond like structure like sphalerite (ZnS) but with an ordered substitution of group I (Cu) and group III (In, Ga) elements on Zn sites. CIGS was developed from $CuInSe_2$ (CIS), a p-type multi-crystalline semiconductor with high absorption coefficient. By adding gallium to CIS and replacing some indium atoms with gallium, the band gap of the material increases and the material will have better optoelectronic properties [27]. This means that by adding gallium atoms, we can tune the band gap of CIGS (1.0-1.4 eV). Fine tuning the bandgap will result in a material that capable to absorb a significant portion of light in the solar spectrum, achieving a very high efficiency and allowing the possibility of tandem CIGS devices [28]. Another benefit of using CIGS the moderate surface recombination velocity at the material's interfaces.

The CIGS solar cell is usually fabricated in substrate configuration. The cells are grown starting with the substrate to then deposit each layer by different commercially

methods. So the sun light falls directly on the absorber layer and does not have to pass through the substrate. Currently used CIGS solar cells consist of five layers. Fig.3. 2 shows the typical layer structure [with layer stack: soda-line glass/Mo back-contact/CIGS absorber/CdS buffer layer/TCO (ZnO or ITO)] of a CIGS solar cell. Several techniques are available for deposition of thin-film CIGS solar cells. Co-evaporation, reactive sputtering, hybrid sputtering, closed-space sublimation, chemical bath deposition and laser evaporation are some of the commonly used deposition techniques. The substrate is the starting point to manufacture a CIGS solar cell. This part is what determines if the cell is going to be rigid or flexible. Due to its low cost and the ability to resist corrosion, glass is one of the most common substrates used in solar cells. However, using any glass substrate negates the ability for a CIGS solar cell to be lightweight and flexible. The use of a metal such as aluminum or stainless steel, offers the capability for a solar cell to keep its lightweight and flexible properties. It is also possible to use thin plastics and polymers as a substrate for a CIGS cell. This would allow to decrease the thickness of the substrate considerably.

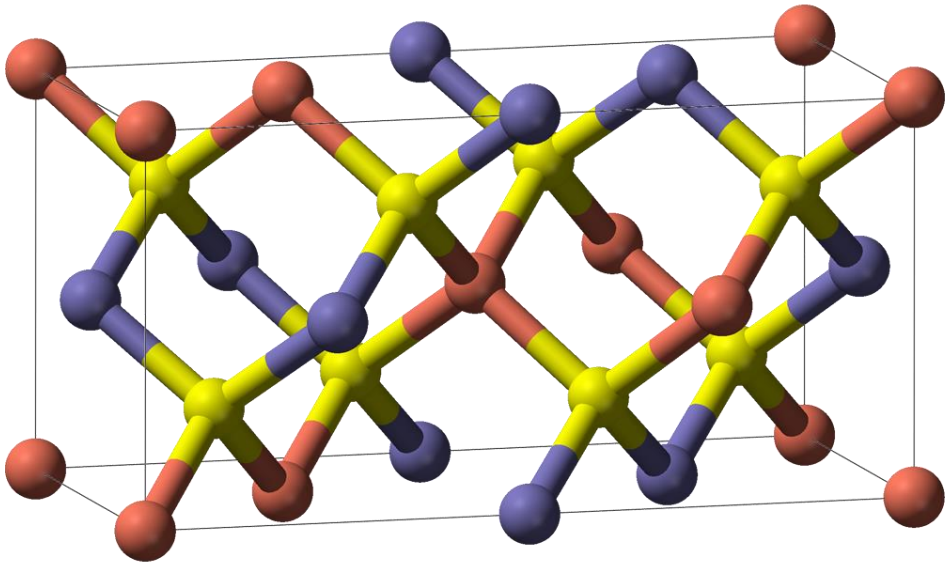

Fig.3. 1 CIGS crystal structure. Cu is on red, In/Ga are on blue and Se is on yellow [29].

The back contact of a CIGS solar cell is located between the top of the substrate and the bottom of the absorber layer (CIGS). The function of the back contact is to collect the carriers as they are produced in the absorber layer. A metal with low resistivity is commonly used as back contact and is the positive lead or anode of the cell. Due to its compatibility in the manufacturing process, molybdenum (Mo) is generally used in CIGS solar cells. The buffer layer is very important to the operation of a CIGS cell. It provides the n-type junction layer in the solar cell hetero-junction. Conventionally an n-type CdS layer is used for the buffer layer. The final layer of the CIGS solar cell is the transparent conducting oxide (TCO) layer and most common used TCOs are either ZnO or ITO.

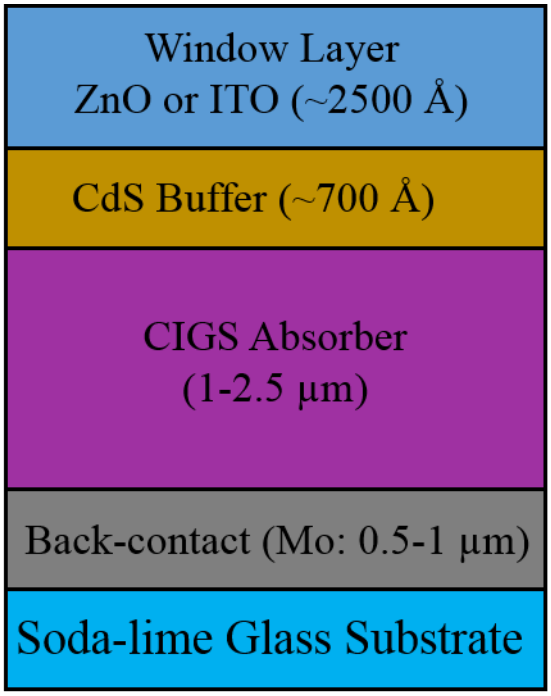

Fig.3. 2 Schematic illustration of a typical CIGS substrate thin-film photovoltaic device.

In developing high-quality CIGS materials and hence high-performance devices, understanding the critical parameters such as charge carrier density, resistivity/conductivity, mobility, and their temperature dependency is important both from scientific and technological perspectives. In particular, the charge carrier mobility in the CIGS materials is a key parameter to both contact resistance and carrier collection efficiency yet less understood than that in the single-crystal PV materials such as Si.

There are several characterization methods to extract the charge carrier mobility and study transport phenomena in semiconductors including the Hall [30], the pulsed laser time-of-flight [31], and the admittance spectroscopy approach [32], [33]. The Hall mobility measurement technique is well established [34], but it applies only to the absorber level (i.e. in the early stage of device fabrication)[35]–[38] and requires the

exclusion of conductive sublayers such as the molybdenum. The pulsed-laser time-of-flight drift mobility measurement is particularly suitable for materials possessing high resistivity and low carrier motility hence applied successfully to a range of insulating solids and liquids [39], [40]. Due to the short duration of the laser pulse and its penetration depth, the time-of-flight technique requires thick films in order to have well defined flight distances [41], [42]. Also, the built-in electric field in the solar cell device makes it complicated to use the time-of-flight photo-transient method and requires specially designed time-of-flight technique and analysis method [43]. Admittance spectroscopy, on the other hand, is an effective and proven method in extracting carrier concentration, resistivity, and mobility [32], [33]. The biggest advantage of the admittance spectroscopic technique is that it can be applied to finished solar cells [44], [45].

The mobility in CIGS solar cells has been investigated using both admittance measurements [46] and the time-of-flight method [47]. However, there are few reports on the temperature dependency of hole mobility and resistivity. This study demonstrates and elaborates the use of coordinated capacitance-voltage and simplified admittance spectroscopy measurements to estimate the resistivity and mobility, and their dependency on temperature for a lightly doped $Cu(In,Ga)Se_2$ solar cell. The temperature dependence of the mobility may reveal the dominant mechanism governing carrier scattering and charge transport. In our specific case of CIGS thin-film materials, the mechanism of interest here is potential fluctuation or the grain boundary barrier height, which is to be measured from the thermal behavior of mobility.

3.2 Experimental

The thin-film $Cu(In,Ga)Se_2$ (CIGS) solar cell studied in this thesis work was fabricated at the National Renewable Energy Laboratory (NREL). The cell structure is as follows: soda-lime glass substrate, sputtered Mo back contact, p-CIGS deposited *via* the co-evaporation method by utilizing the standard three-stage recipe (with substrate temperature of 435 °C) [48], chemical-bath deposited n-type CdS, sputtered ZnO (TCO), and e-beam evaporated Ni/Al grids for front-contact.

To perform the Capacitance-Voltage (C-V) measurement and the Admittance Spectroscopy, an Agilent 4294 Impedance Analyzer was used to collect the data. For the capacitance-voltage measurement, the DC bias voltage was varied from -1.5 to 0.6 V while keeping an AC modulation amplitude of 50 mV_{p-p} at 10 kHz. For admittance spectroscopy, the DC bias was varied from -1.5 to 0.6 V, the temperature from 14 to 350 K with a step size of 7 K, and the frequency from 10^3 to 10^8 Hz. After the measurement, we analyzed and processed all acquired data using a specially designed program developed in Igor-Pro software by Dr. Jian V. Li.

3.3 Results and Discussions

3.3.1 Solar Cell Current Density - Voltage Characteristics

Fig.3. 3 show the dark and light (one sun: 100 mW/cm^2) characteristics of the solar cell used in this study. The cell parameters are: V_{OC} = 0.566 V, J_{SC} = 29.12 mA/cm^2, FF = 52.91%, and η = 8.728%. Note that the acceptor density for this device 4×10^{14} cm^{-3} is lower than that of a typical high-efficiency device ($N_a \sim 10^{16}$ cm^{-3}). The low doping results in a poor device performance, i.e., low V_{OC}. The V_{OC} = 0.566 V is consistent with our acceptor density [49], [50].

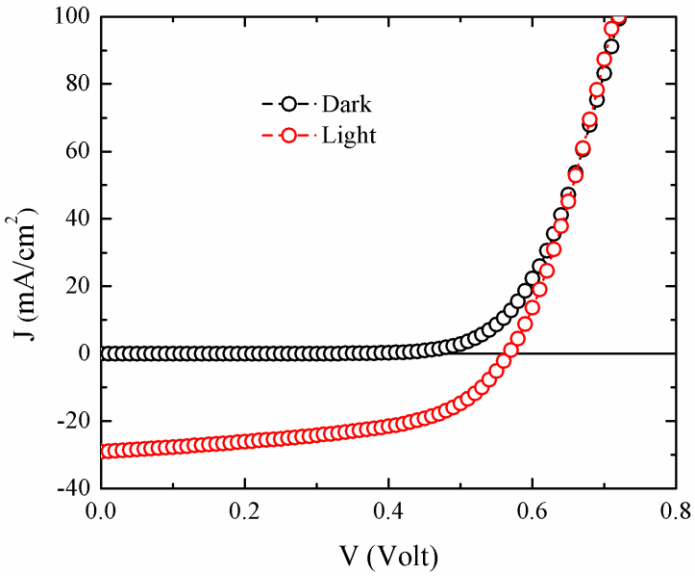

Fig.3. 3 Dark and light current-voltage characteristics of CIGS the CIGS solar cell. In the light JV characteristics, intensity of the illumination light (equivalent to AM1.5) is one sun (100 mW/cm^2).

3.3.2 Charge Transport Study via Admittance Spectroscopy

In exploring the charge transport study in this CIGS solar cell, we need to introduce some basic theory of admittance spectroscopy. Fig.3. 4(a) shows the energy band diagram of the CIGS solar cell with clear representation of the depletion and quasi-neutral (bulk of CIGS absorber) region. The solar cell can be modeled by the equivalent circuit shown in Fig.3. 4(b). The depletion region is modeled as a depletion capacitance C_d. The quasi-neutral region is modeled as the parallel connection of a capacitor (C_g') and a conductor (G_g'). We will refer to those as the geometrical capacitance and conductance of the quasi-neutral region.

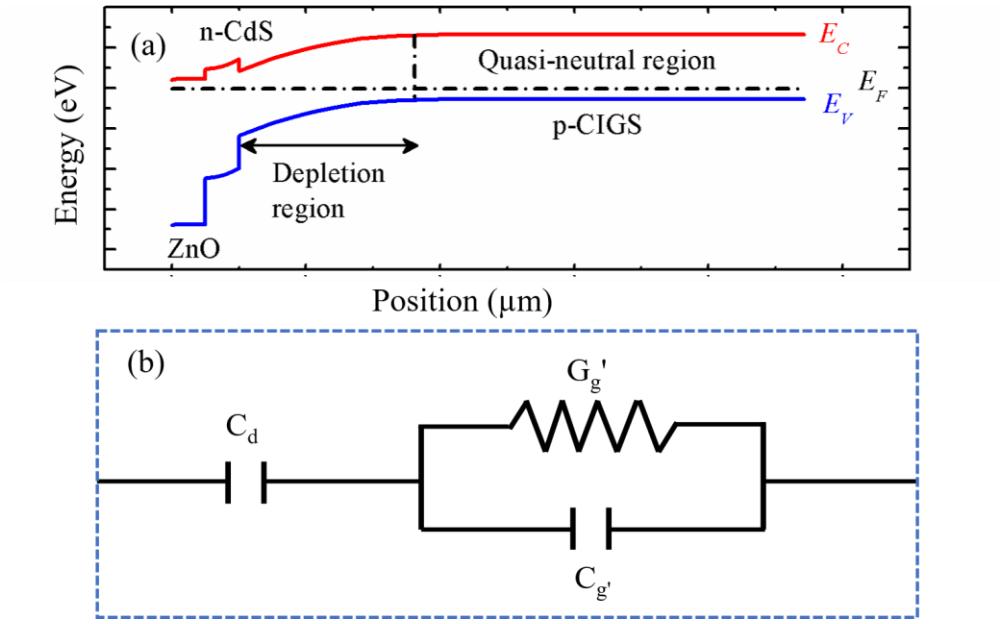

Fig.3. 4 (a) Energy band diagram of CIGS solar cell, and (b) the equivalent circuit corresponding to the energy band diagram in (a). The depletion region is modeled as a depletion capacitance C_d. The quasi-neutral region is modeled as the parallel connection of geometrical capacitance (C_g') and the conductance (G_g').

The response of the majority carrier particularly at a frequency (ω) of the ac signal is limited by the dielectric relaxation time τ_D $\left(\tau_D = \frac{2\pi}{\omega_D};\ \omega_D = {}^{\sigma}/_{\varepsilon}\right)$, where, σ is the conductivity (=1/ρ; ρ = resistivity) of the material and ε is the dielectric permittivity. For frequency $\omega < \omega_D$, the absorber in the quasi-neutral region behaves as a conductor with bulk conductance $G_g' = {}^{A}/_{\rho(t-W)}$, where A is the cell area, W the depletion width, and t the absorber thickness. Whereas, for high frequencies ($\omega > \omega_D$), the quasi-neutral absorber behaves like a capacitor with bulk capacitance $C_g' = {}^{\varepsilon A}/_{(t-W)}$. The admittance analysis of the equivalent circuit of the CIGS solar cell using a small AC signal model, leads to the following equation

$$C = C_d \frac{1+\left(C_d/C_g\right)\left(\rho\varepsilon\omega\right)^2}{1+\left(C_d/C_g\right)^2\left(\rho\varepsilon\omega\right)^2}$$
$$\frac{G}{\omega} = C_d \frac{\left(C_d/C_g - 1\right)\left(\rho\varepsilon\omega\right)}{1+\left(C_d/C_g\right)^2\left(\rho\varepsilon\omega\right)^2} \qquad (3.\ 1)$$

Experimentally, the capacitance *vs.* frequency plot, as shown in Fig.3. 5 shows step transition with an inflection frequency (ω_p) below which C approaches C_d and above which C approaches C_g, which is the series connection of C_d and C_g'. Using simple calculus and algebra, ω_p can be estimated *via* minimizing [see $\omega\frac{dC}{d\omega}\ vs.\ \omega$ plot in Fig.3. 5] the expression in equation (3. 1) and its expression is

$$\omega_p = \frac{W}{t}\left(\frac{1}{\rho\varepsilon}\right) \qquad (3.\ 2)$$

Because of the dependency of depletion width (W) with applied dc bias (V), $W \approx \sqrt{\frac{2\varepsilon\,(V_{bi}-V)}{qN_a}}$, ω_P depends on V. Where, N_a is the acceptor density, q is the elementary charge, and V_{bi} is the built-in potential. The bias dependent inflection frequency (ω_p) in the n^+-p junction is given by the relation

$$\omega_p{}^2 = \frac{W^2}{t^2}\left(\frac{1}{\rho\varepsilon}\right)^2 = \frac{2}{q\varepsilon N_a \rho^2 t^2}\left(V_{bi} - V\right) \qquad (3.\ 3)$$

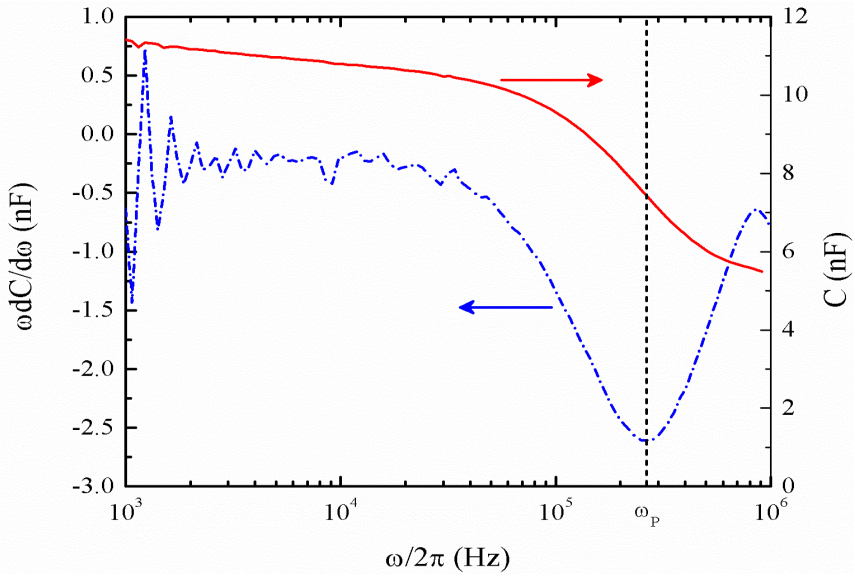

Fig.3. 5 The frequency (ω) dependent capacitance (C) and differential capacitance (ωdC/dω) spectra used to extract the inflection frequency (ω_P).

Now, using equation (3. 2) and from experimental data (ω_p^2 vs. V plot), the slope can be used to extract the resistivity (ρ) and hence the mobility (μ) as

$$\rho = \sqrt{\frac{2}{q\varepsilon N_a t^2 \times Slope}} \tag{3. 4}$$

and

$$\mu = \frac{1}{qN_a\rho} = \sqrt{\frac{\varepsilon t^2 \times Slope}{2qN_a}} \tag{3. 5}$$

Using standard procedures at high temperature and low frequency, we calculate the hole density N_a from the local slope of the Mott-Schottky plot of C^2 vs bias N_a=-2/slope/qεA^2 and depletion region W=εA/C. N_a is determined to be 2.2x10^{14} cm^{-3} at 150 K. At lower temperatures, the entire CIGS absorber becomes depleted and the thickness of the absorber is determined to be 3.3 μm using a dielectric constant value of 13.6 (Fig.3. 6).

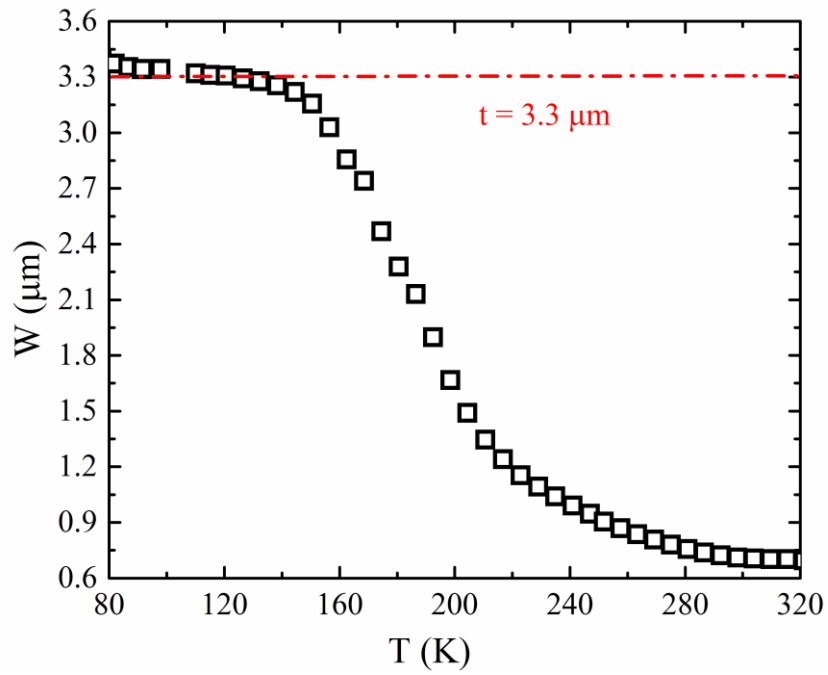

Fig.3. 6 Variation of depletion width with temperature. At lower temperatures (< 150 K), the entire CIGS absorber becomes depleted and the thickness of the absorber is determined to be 3.3 μm using a dielectric constant value of 13.6.

The frequency dependent capacitance (C) and differential capacitance ($\omega \, {dC}/{d\omega}$) spectra of the CIGS solar cell for different applied bias voltage (-0.4 – 0.1 Volt, ΔV = 0.1 Volt) are shown in Fig.3. 7. The temperature in this case is 203K. We present this as an example. Similar behavior was observed at other temperatures. In all cases, the depletion

capacitance shows a step (Fig.3. 7a) at inflection frequency (ω_P) which was determined from the peak seen in the differential capacitance spectrum (Fig.3. 7b). The transition frequency, ω_p, shifted towards higher frequency with bias is key to extracting the resistivity and carrier mobility.

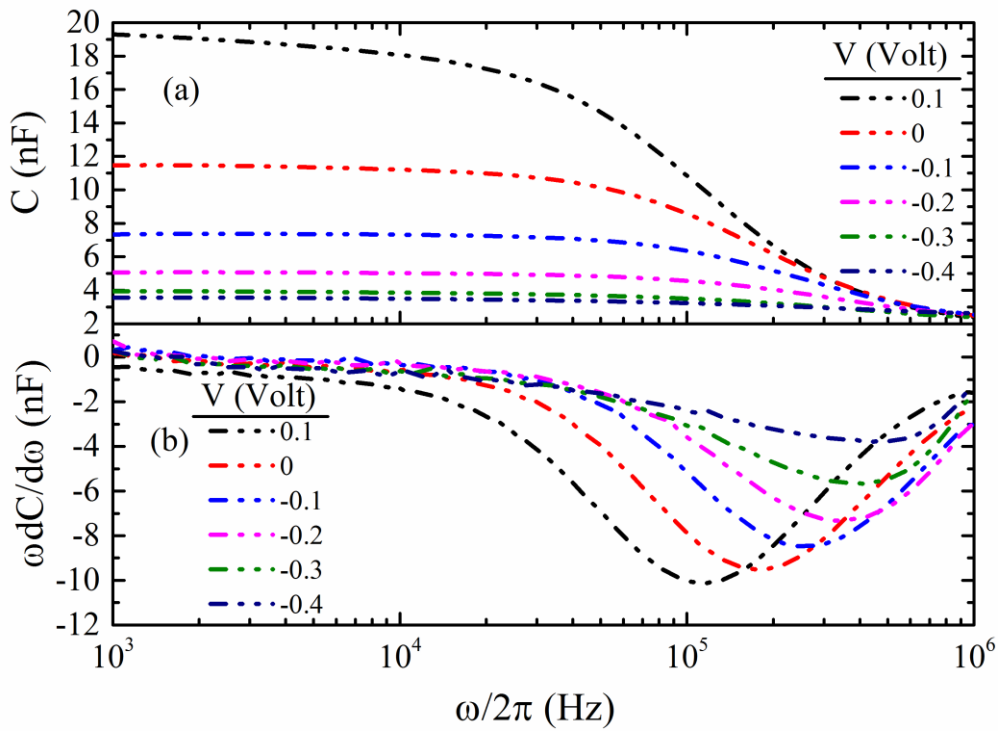

Fig.3. 7 The bias (V) dependence of capacitance and differential capacitance spectra plotted against frequency of the CIGS solar cell at T = 203K. The voltage change is from -0.4 Volt to 0.1 Volt with voltage step ΔV = 0.1 Volt.

The inflection frequencies (ω_p's) from the $\omega\left({}^{dC}/_{d\omega}\right)$ *vs.* ${}^{\omega}/_{2\pi}$ plot (as shown in Fig.3. 7b) were used to extract the resistivity (ρ) and mobility (μ) of CIGS. As expected from equation (3. 3), the square of the inflection frequency, ω_p^2, depends linearly on the bias voltage (V) as shown in Fig.3. 8. The measurement temperature for this data set was at 203K. The linear fitting leads to $\rho = 1.86 \times 10^4$ Ωcm and $\mu = 0.19$ cm^2/Vs using

equation (3. 4) and (3. 5). The acceptor concentration (extracted from the CV measurement) at 203 K was 1.76×10^{14} cm^{-3}.

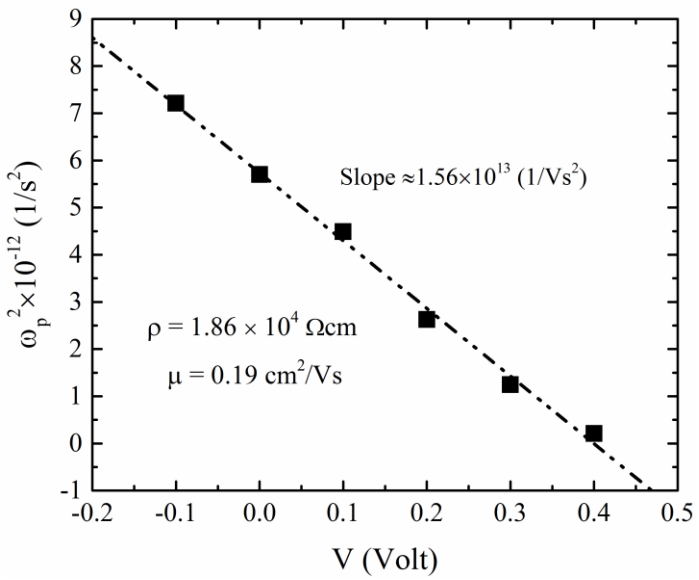

Fig.3. 8 The square of ω_P^2 exhibit a linear dependence on the bias voltage (V) at T = 203K as described in equation (3. 3), from which a slope (1.56×10^{13} $V^{-1}s^{-2}$) is determined. This leads to extraction of resistivity ($\rho = 1.86 \times 10^4$ Ωcm) and hole mobility ($\mu = 0.19$ cm^2/Vs) respectively.

The extracted hole mobility is lower than that measured by Lee et al. *via* high frequency admittance measurement in polycrystalline $Cu(In,Ga)Se_2$ [46]. With various $Cu(In,Ga)Se_2$ cells with Ga content in the range of 0 – 34%, the hole mobility μ_h in that report varies from 2.9 ± 0.3 to 22 ± 4.2 cm^2/Vs. The reported temperature in their measurement is 150K. Temperature independent hole mobility was reported by this group. Extracted mobility in our measurement at this temperature is $\approx 3.24 \times 10^{-2}$ cm^2/Vs. On the other hand, our extracted hole mobility (4.08 cm^2/Vs) at 300K is larger than the reported value (0.6 cm^2/Vs) by S. A. Dinca et al.[47]. The measurement method they used was a specially arranged pulsed laser time-of-flight technique. This technique has lots of limitations. When extracting mobility *via* time-of-flight photo-transient

measurement, it is challenging to estimate the transit time of photogenerated charge carriers particularly with very thin films. In addition, trapping and multiple trapping phenomena during the charge carrier's journey influenced the transient signal and hence the measured hole mobility. It is noteworthy that, the drift mobilities ranged from 0.02 - 0.7 cm^2/Vs at room temperature with several CIGS cells fabricated different laboratories.[47] The presence of trap signature was observed in estimating electron mobility (0.02 - 0.05 cm^2/Vs). S. A. Dinca et al. also reported weakly temperature dependent hole mobility (measured using time-of-flight method) in polycrystalline $CuIn_{1-x}Ga_xSe_2$ in the temperature range of 100–300 K [47]. Our experimental observation shows strong temperature dependence of the hole mobility as shown in Fig.3. 9(a). It is also important to mention here that in the temperature dependent mobility estimation, we have used the temperature dependent carrier concentration as shown in the inset of Fig.3. 9.

The temperature dependent mobility behavior is Arrhenius type (as shown in Fig.3. 9b), i.e. thermally activated, and follows the Arrhenius equation ($\mu = \mu_0 e^{\frac{-E_{a,\mu}}{k_B T}}$, where μ_0 is the mobility pre-factor, k_B is the Boltzmann's constant, $E_{a,\mu}$ is the activation energy of the mobility, and T is the absolute temperature). Fitting the mobility and resistivity data with the Arrhenius equation leads to the following activation energy $E_{a,\mu}$ = 116.1±5.7 meV. The mobility pre-factor is found to be $\mu_0 = 2.13 \times 10^2 \pm 1.46$ cm^2/Vs.

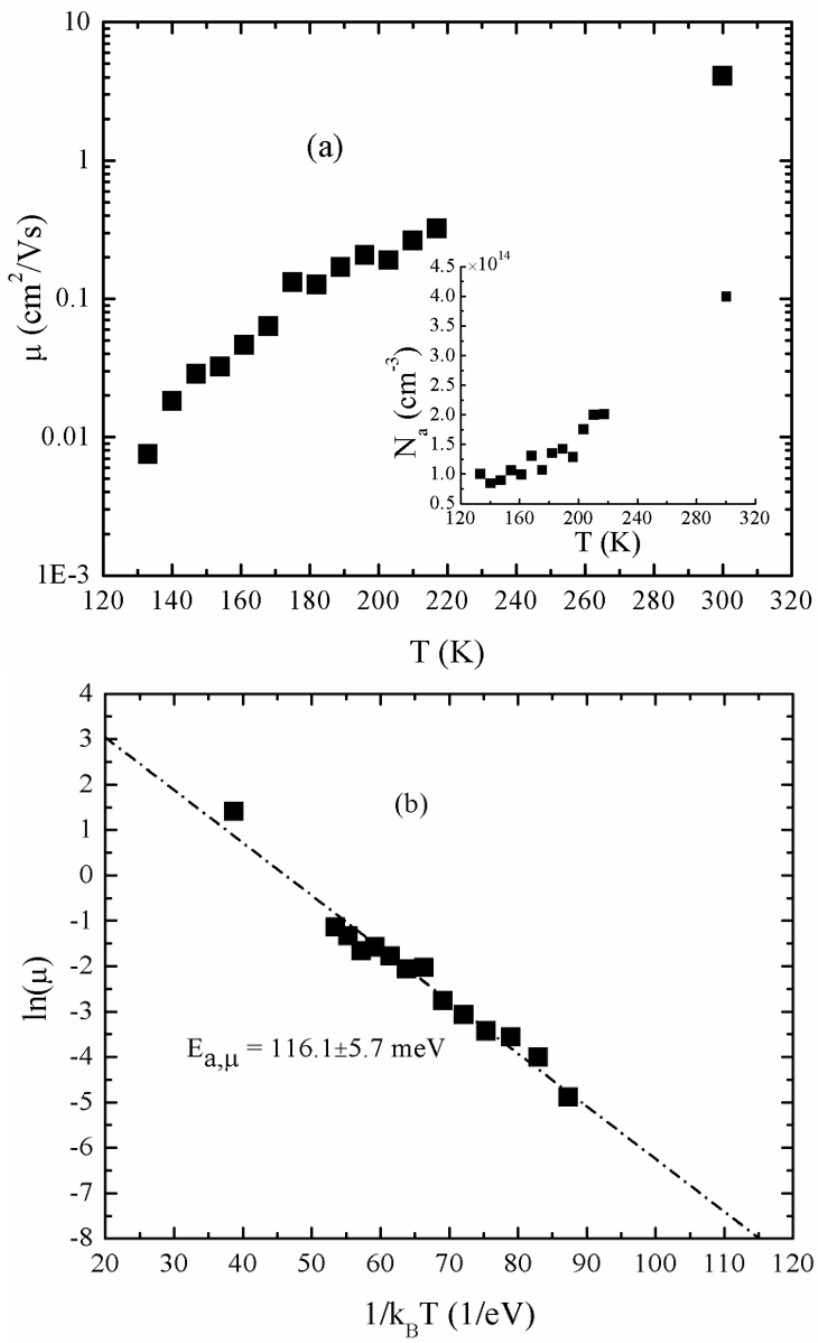

Fig.3. 9 (a) Variation of mobility (in logarithmic scale) with temperature (inset shows temperature dependency on N_a), and (b) the temperature (range: 133 – 300K) dependent Arrhenius plots (i.e. logarithmic of mobility or resistivity vs. $1/k_BT$) for mobility with activation energy 116.1±5.7 meV.

The estimated activation energy of mobility is possibly due to band fluctuations originating from compositional variations and/or grain boundary barrier height variations in the polycrystalline semiconductors material [32]. The temperature dependent mobility behavior in polycrystalline silicon have been modeled by J. Y. W. Seto [51]. The polycrystalline semiconducting materials consist of variable sized grain and grain boundary. The crystallographic structure of grain boundaries is not perfect, and they are highly defective. Our CIGS absorber material is polycrystalline in nature. Due to carrier trapping in p-type CIGS, downward band bending occurs, and the height of the band bending is a measure of the grain boundary barrier height [51]. While there are few reports on the temperature dependence of the mobility in $Cu(In,Ga)Se_2$, there have been several reports on the temperature dependent conductivity in this material. Yan et al. reported the temperature dependent conductivity data (via Hall measurement) in one-stage RF sputtered deposited CIGS and reported two different slopes in the resistivity curve [37]. In the high- temperature regime (>120K) the dominant transport mechanism is indicated as the thermionic emission transport with an activation energy (increases with substrate temperature) of 90.6 meV which corresponds to samples grown at substrate temperature of 380 °C. Similar activation energy (98.1 meV) in the temperature dependent conductivity data was reported by Mesa et al. in which CIGS was deposited via three stage process.[35] In our case the substrate temperature is 435 °C and the observed activation energy 116.1±5.7 meV is reasonable if substrate temperature plays an important role in the transport process. The second possibility of the 116.1±5.7 meV activation energy is due to the bandgap fluctuation which is due to the compositional variation in Cu(In,Ga)Se2 [52], [53].

3.4 Conclusions and Future Works

We describe the electrical characterization of a CIGS solar cell (with PV parameters: V_{OC} = 0.566 V, J_{SC} = 29.12 mA/cm^2, FF = 52.91%, and η = 8.738%) fabricated at National Renewable Energy Laboratory (NREL). Further, we use a classic and straightforward method based on coordinated capacitance-voltage techniques and bias dependent admittance spectroscopy to measure the resistivity, hole mobility, and their temperature dependence in this solar cell. In the temperature range of 133 – 300K, the hole carrier mobility varies between 7.55×10^{-3} cm^2/Vs - 4.08 cm^2/Vs respectively. The temperature dependent mobility and resistivity shows thermally activated behavior with an activation energy of 116.1±5.7 meV, which is speculated to be directly tied to the potential fluctuations due to grain boundaries. These potential fluctuations agree well with the values estimated by using optical and microscopy technique. This method and the observed results on the charge transport are useful for further optimization of material processing and device fabrication. The future work may include the verification of temperature dependent hole mobility in CIGS thin film using Hall measurements.

IV. ELECTRICAL AND DEFECT CHARACTERIZATION IN β-Ga2O3

4.1. Introduction

In power electronics, to date, silicon (either crystalline or amorphous form) is the major material [54]. However, the high cost of purifying silicon (Si) is a major burden for cheap electronics. More and more electronics require high power electronic devices easily realized in silicon [55]. The use of wide bandgap semiconductors allows for devices with higher current densities and higher power ratings than possible in silicon. Wide bandgap semiconductors have superior materials properties, including higher breakdown voltages and much lower switching losses [56]. Up to the present, the two most promising, highly developed wide bandgap materials for power electronics are gallium nitride (GaN) [57] and silicon carbide (SiC) [58]. However, both have massive weaknesses including high cost, low mobility, and substrate choice challenges when it comes to mass production.

A promising wide bandgap alternative that has been overlooked up until now is gallium oxide (Ga_2O_3). Its high bandgap (4.5 – 4.9 eV) [59] and high breakdown voltage [60] make it an attractive semiconductor material for high power electronics devices. In addition, Ga_2O_3 power device manufacturing could be possibly low cost at high volume, because it is possible to produce single-crystal native substrates from a melt using the same method employed for manufacturing sapphire substrates [27]. In addition, in employing Ga_2O_3 in power devices, Ga_2O_3 use in other applications such as its use as transparent conducting oxide layer in solar cells, ultra-violet (UV) photodetectors, and sensors [61].

A better understanding of the materials properties of Ga_2O_3 including its electronic quality and defect properties is required for the successful application in devices [62]. There are five available variants [63], [64] of Ga_2O_3: α–Ga_2O_3, β–Ga_2O_3, γ–Ga_2O_3, δ–Ga_2O_3, and ε–Ga_2O_3. The β–Ga_2O_3 phase (Fig.4. 1) is the more stable structure which is mostly studied by academic and the semiconductor.

In this thesis, the electrical properties including defect characterization of β–Ga_2O_3 material from Tamura Corporation (Japan) is being reported on [65]. This chapter focusses on the electrical characterization of ITO/β-Ga_2O_3 Schottky diodes. Schottky devices were used to extract electronic quality and defect properties of β-Ga_2O_3. Others have used the Hall effect and deep level transient spectroscopy (DLTS) to characterize β-Ga_2O_3,Here we report on the characterization of β-Ga2O3 using capacitance and admittance spectroscopy [66].

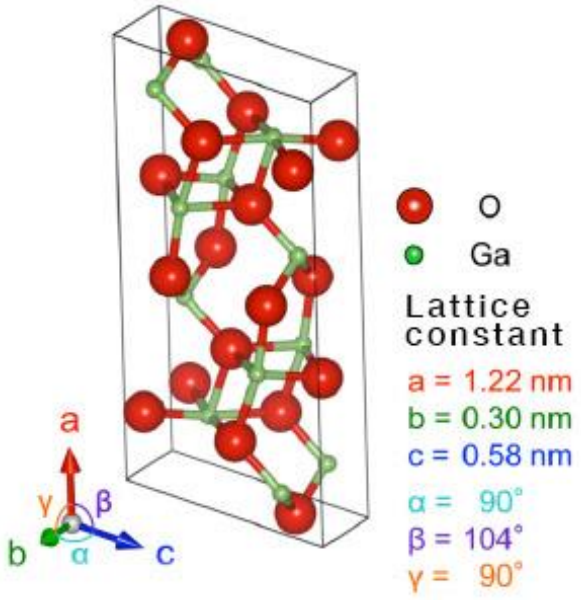

Fig.4. 1 Lattice structure of Ga_2O_3 (with permission from Tamura Corporation) [65].

4.2. Experimental

We used commercially available unintentionally doped (201) β–Ga_2O_3 wafers from Tamura Corporation. These wafers were grown via the EFG method. Schottky and Ohmic contacts (the layer structure and top view of the sample is shown in Fig.4. 2) were made to the material by Dr. Shin Mou's research group at Air Force Research Laboratory. Initially, the wafer was diced into 1 cm × 1 cm square sample. Following dicing, the material was solvent cleaned and 50nm/1μm Ti/Au contacts were sputtered on the sample corners. These electrodes act as Ohmic contacts. Schottky contacts were made to the β–Ga_2O_3, by depositing a thin layer of indium tin oxide (ITO) on the other side of β–Ga_2O_3 substrate. To improve contact resistance, the sample was annealed in a tube furnace with argon gas flow at a temperature of 450 C with a 15 min ramp.

We performed admittance spectroscopy measurements using the Agilent 4990A Impedance Analyzer to collect the data. The AC modulation amplitude used was nominally 50 mVrms. Measurements were done over a wide frequency range stretching from 10^2 to 10^6 Hz. The DC bias was varied from -0.6 to 0.6 V. The temperature was varied from 20 – 320K with a step size of 10K using an ARS cryogenic probe station controlled by a Lakeshore 336 temperature controller. After the measurement, we analyzed and processed all acquired data using a specially designed program developed in Igor-Pro software by Dr. Jian V. Li.

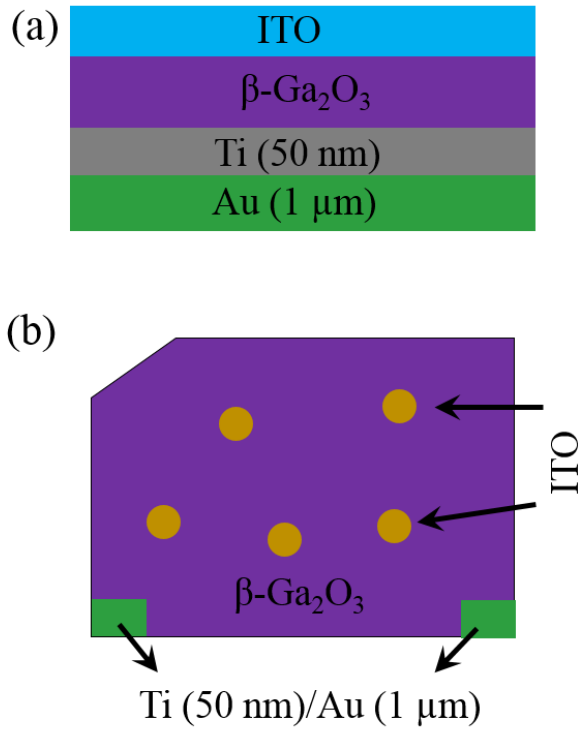

Fig.4. 2 The device stacks - (a), and the sample top-view - (b) of the Schottky diode using ITO/β-Ga2O3.

4.3 Results and Discussions

Fig.4. 3 shows the current-voltage characteristic of an ITO/ β–Ga_2O_3 Schottky diode (as in the inset) at T = 300K. In the reverse bias, at around -0.9V the breakdown happens. In the forward bias the current grows rapidly above V = 0.5V.

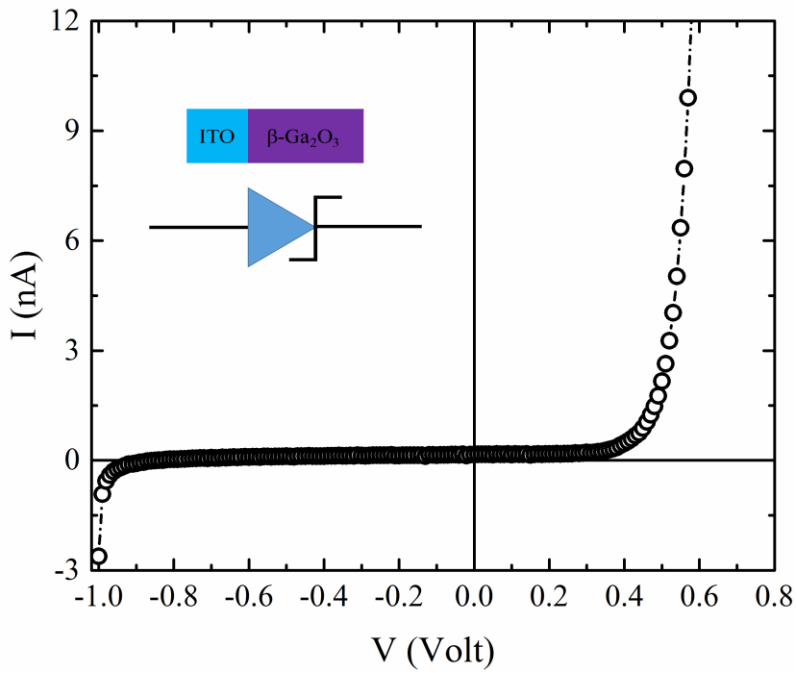

Fig.4. 3 Current-voltage characteristic of ITO/ β–Ga_2O_3 Schottky diode at T = 300K.

Fig.4. 4 shows the capacitance-voltage (CV) and the Mott-Schottky plots for the ITO/β–Ga_2O_3 Schottky diode at T = 300K. The CV characteristics is typical for a Schottky diode. To estimate, the built-in potential in the ITO/β–Ga_2O_3 Schottky diode, we use the Mott-Schottky equation, which is given by

$$\frac{1}{C^2} = \frac{2}{qA^2\kappa\varepsilon_0 N_d}\left(V_{bi} - V\right)$$

Here, q is the electronic charge (= 1.602×10^{-19} C), A the device area (0.02 cm^2), κ the dielectric constant (here 10 for β–Ga_2O_3), ε_0 the free space permittivity (= 8.85×10^{-12} F/m), N_d is the donor concentration, and V_{bi} is the built-in voltage to be estimated.

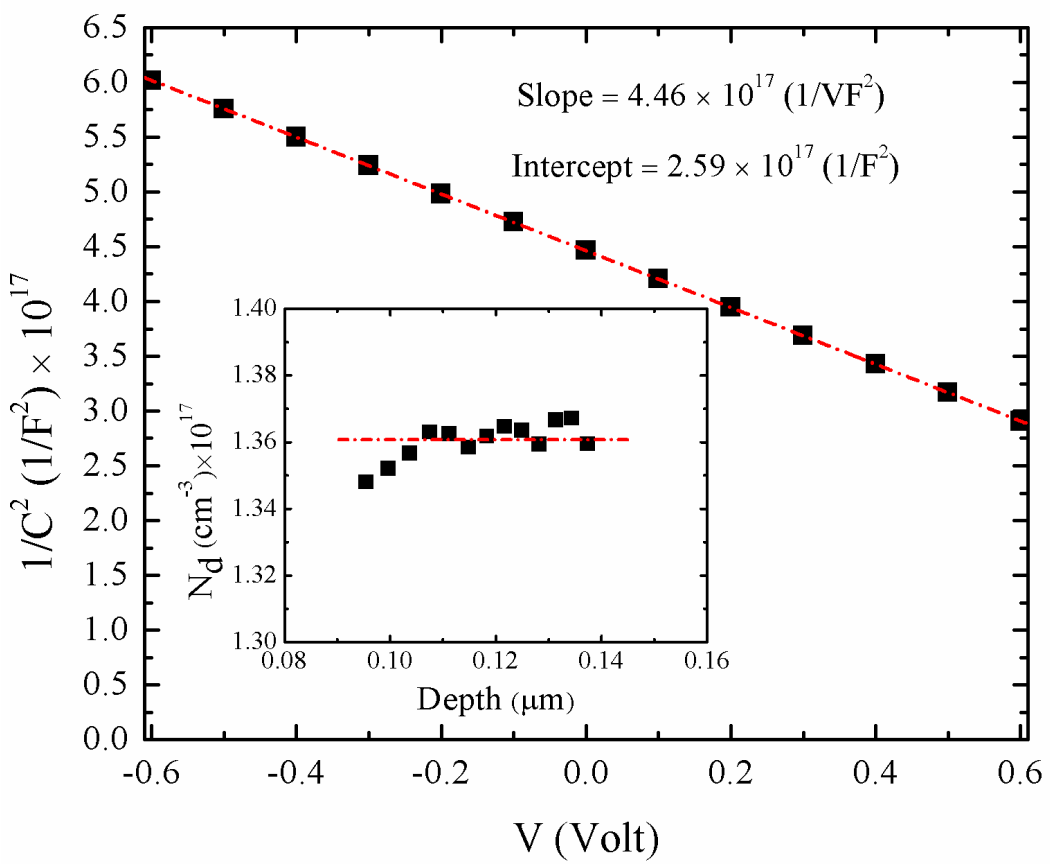

Fig.4. 4 Capacitance-voltage (CV) and Mott-Schottky ($1/C^2$ vs. V) plots for the ITO/ β–Ga_2O_3 Schottky diode at T = 300K.

The Mott-Schottky analysis gives for the value of negative slope ($\frac{2}{qA^2\kappa\varepsilon_0 N_d}$) and the intercept ($\frac{2}{qA^2\kappa\varepsilon_0 N_d} V_{bi}$) 4.46 × 10^{17} $1/VF^2$ and 2.59 × 10^{17} $1/F^2$ respectively. The built-in potential is the ratio of to the intercept and the slope and its value is 1.72 Volt. We extract the electron density (N_d in cm^{-3}) from the differential capacitance technique (give the free electron density as function of depth) using equation $N_d = \frac{2}{qA^2\kappa\varepsilon_0}\left(\frac{d\left(1/C^2\right)}{dV}\right)^{-1}$ and the estimated value is ~ 1.36 × 10^{17} cm^{-3} at 300K.

Fig.4. 5 shows the frequency ($\frac{\omega}{2\pi}$ in Hz) dependent capacitance (C is nF) and differential capacitance (ωdC/dω in nF) spectra at a temperature of T = 250K. The frequency dependent capacitance shows a step transition which shows up as a minimum in the differential capacitance spectra. It has an extreme at a peak frequency $\frac{\omega_P}{2\pi}$ = 2.9 × 10^4 Hz. In the defect characterization, this peak frequency is important. Its position changes with temperature.

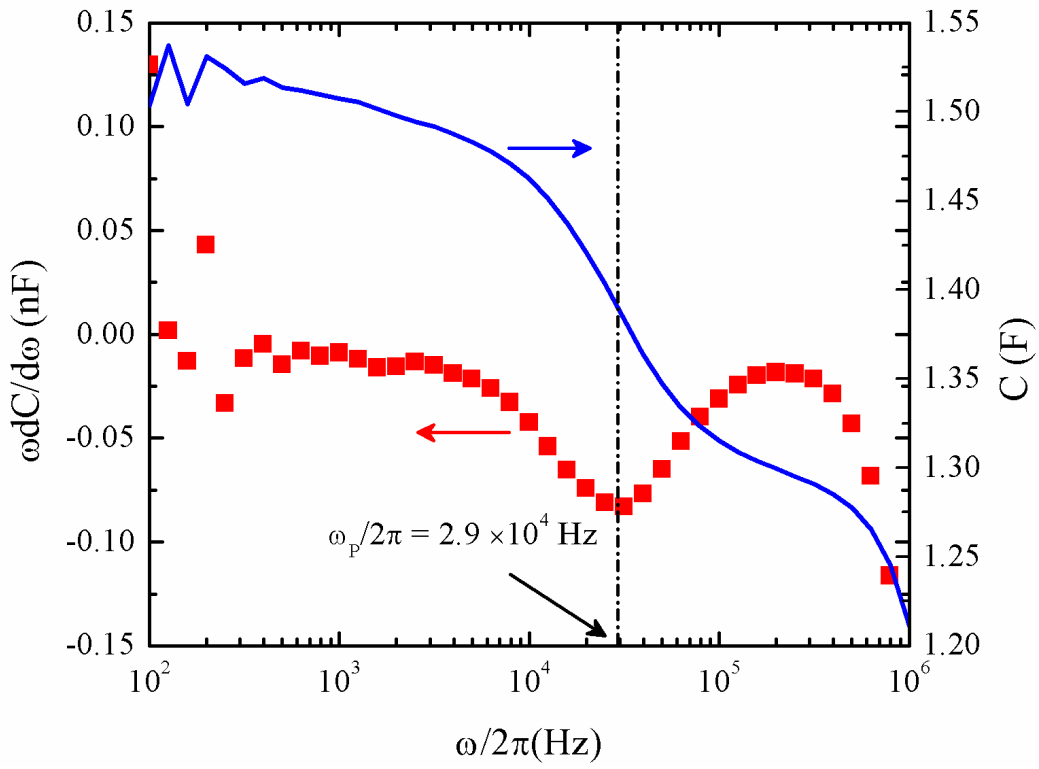

Fig.4. 5 Frequency dependent capacitance (a) and differential capacitance (b) spectra of the ITO/β-Ga_2O_3 Shhottky device at T = 250K.

Fig.4. 6 shows the differential capacitance spectra as a function of temperature (T: 40 – 320K). The single minima in this spectrum indicates to the presence of a single defect which will be discussed later in this chapter.

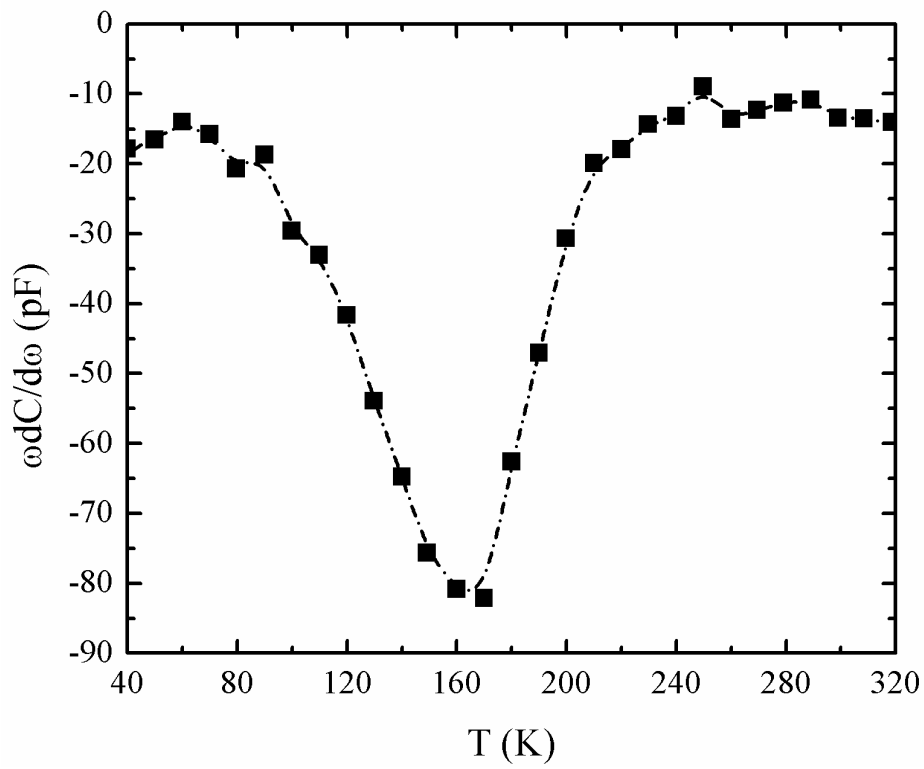

Fig.4. 6 Differential capacitance spectra as function of temperature.

To explore the defect properties and the energetic location of the defect present in the β-Ga_2O_3, we plot the frequency dependent capacitance and differntial capacitance spectra in the temperature range of 180 – 280K as shown in Fig.4. 7(a) and (b) respectively. Each graph (Fig.4. 7a) shows a capacitance indicated by minimas in the corresponding differential capacitance spectra (Fig.4. 7b).

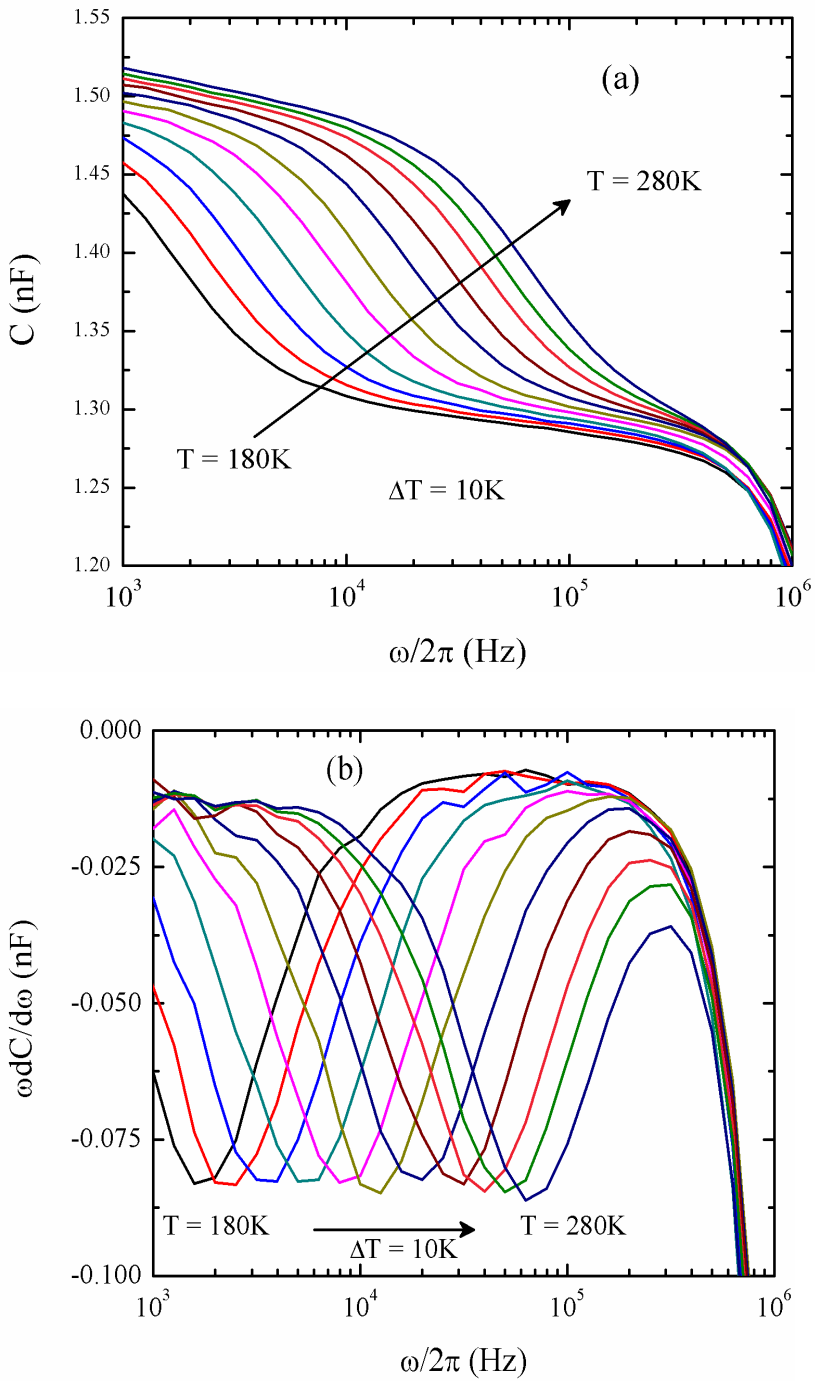

Fig.4. 7 Frequency dependent capacitance (a) and differential capacitance spectra (b) of the ITO/β-Ga_2O_3 in the temperature range of 180 – 280K.

The temperature dependent peak frequencies $\omega_P = (2\pi f_P)$ follows an Arrhenius equation and allows for the determination of the energy level and capture cross section of the defect. Fig.4. 8 shows a plot of $\ln\left({\omega_P}/{T^2}\right)$ $vs.$ ${1}/{k_B T}$. Slope and intercept can be used to determine the defect level (E_t) in the bandgap and the defect's capture cross-section (σ_t). The data of Fig.4. 8 suggest that the defect activation energy is E_t = 131.2 ± 5.4 meV.

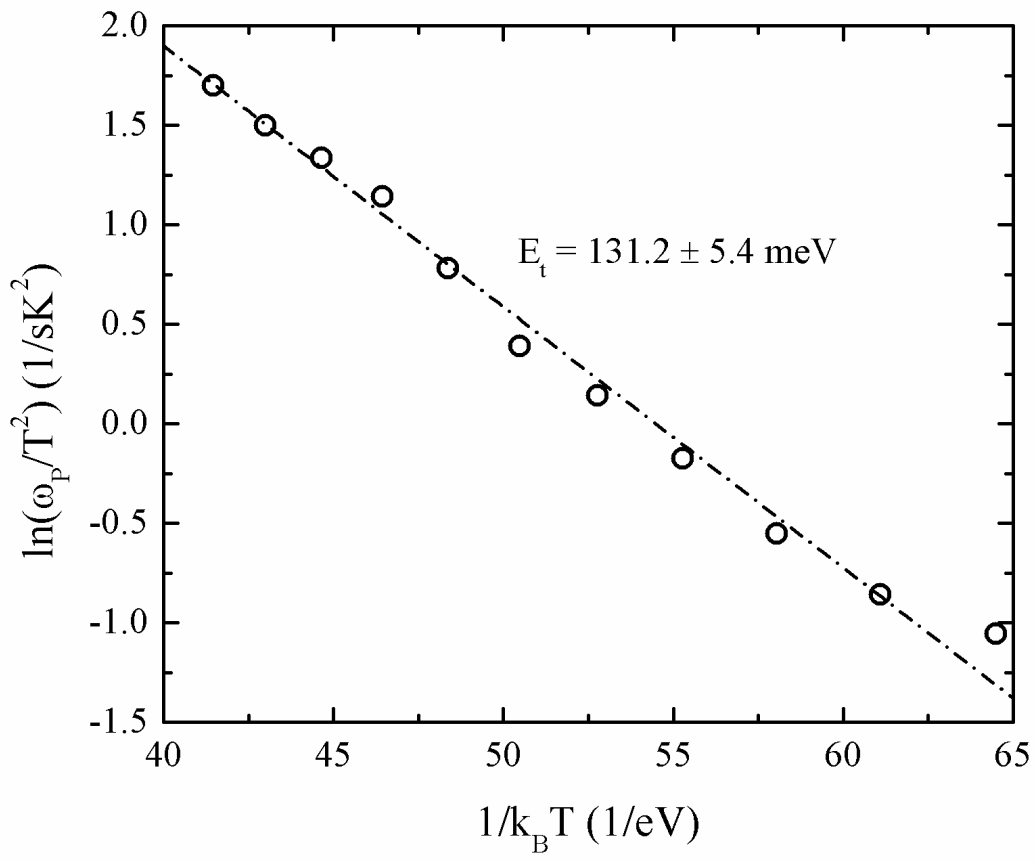

Fig.4. 8 The Arrhenius plot for the defect activation energy in the temperature range of 180 – 280K.

We further calculated the trap density from $N_t = N_d \left(\frac{\Delta C}{C_0}\right)$, where ΔC is the step size of the capacitance transition and C_o the capacitance value at the lower plateau (as shown in Fig.4. 7a). The trap density is N_t = 3.7×10^{16} cm^{-3}.

4.4 Conclusions and Future Works

We have studied the defect structure of β-Ga_2O_3 material by fabricating an ITO/β-Ga_2O_3 Schottky diode. Capacitance and admittance spectroscopy were performed as a function of temperature on the Schottky device to extract electronic properties of β-Ga_2O_3 defects. In the temperature range of 180 – 280K, we observed a single defect located at 131.2 ± 5.4 meV. The estimated trap density estimated is N_t = 3.7×10^{16} cm^{-3}. This device possesses 1.17 V built-in potential whereas the donor density was observed 7.9 × 10^{16} cm^{-3}. Future work may include verifying the defect level and trapping density using other correlated methods like deep level transient spectroscopy (DLTS).

APPENDIX SECTION

A.1 Switch Program

As the switch is being controlled through the impedance analyzer I/O port, we created a program that communicates to the E4990A and select the input and output desired for the required measurement (Fig.A. 1).

The front panel of the VI (Virtual instrument) shows an image of the physical circuit. This avoids confusion as the user can see what is happening. This VI gets the information (VISA resource name, the error in, the Input number desired to use and the output number desired) from the user directly using the controllers on the front panel (if the program is running independently) or gets the information from another program (if used as a VI by another code).

The program first set the output from the impedance analyzer to the switch matrix to be 0 (this restarts any condition stablished before). Then it reads the number entered in the fields “Input” and “Output” and select the binary number to be used according to the selected values. Since the first pin is the one that activates the usage of the port, we needed to make sure to add 1 to the binary number to activate the port. Then we simply just send the binary number to the impedance analyzer in order to activate the correct inputs and outputs of our circuit board. The block diagram is shown in Fig.A. 2.

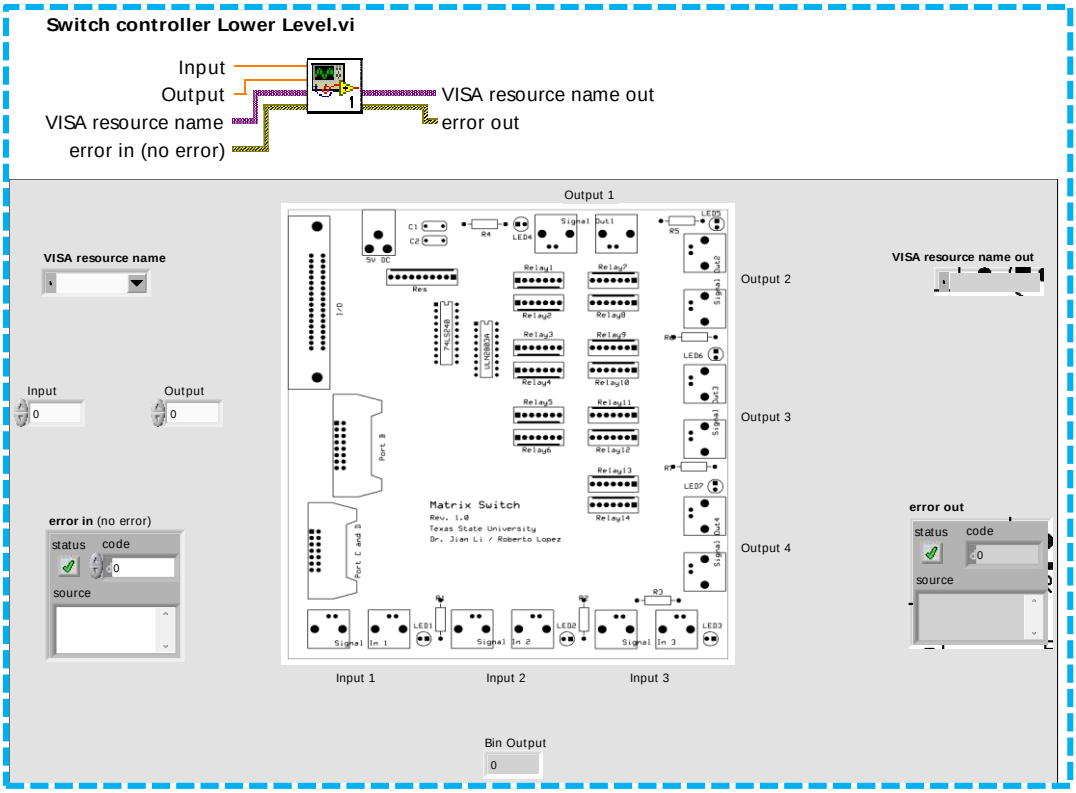

Fig.A. 1 Front panel of switch program VI.

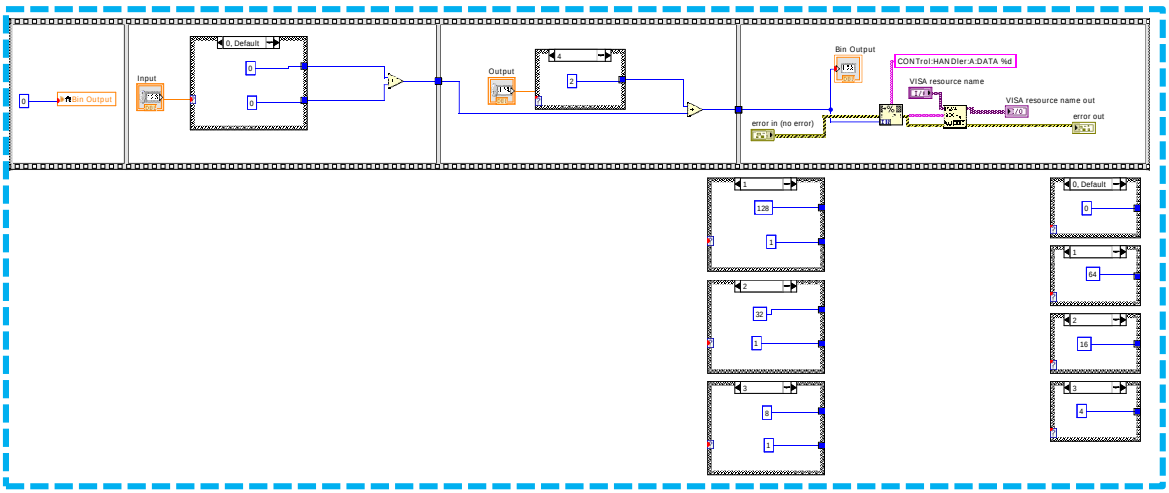

Fig.A. 2 Block diagram of switch program.

A.2 Frequency Sweep Program

As one of the main characterization techniques that we have been using is admittance spectroscopy, we needed a system capable to collect the measurement data. The variables used for this measurement are temperature, DC Bias Voltage, and frequency. The best option for this VI was to sweep through a specified frequency range at a specific temperature and bias voltage. The main program uses this VI on multiple occasions to measure the frequency dependence at different DC Bias and at different temperatures, creating a matrix. In order to simplify the understanding of the program, we will only show how the sweep program works.

This VI receives the set points for the measurement (AC peak, DC Bias, Speed required to perform the experiment, frequency start point, frequency stop point, number of data points collected, VISA resource name and error in), then it performs a frequency sweep with those values and gives back the data with capacitance, conductance, frequency points and measured DC Bias during the sweep (Fig.A. 3).

The VI first sets the impedance analyzer to its default values. Then it sets the experimental conditions, such as sweep ranges and bias voltage and other parameters, it then triggers the sweep (separate VI), wait for the measurement to finish (separate VI), and collect the data from the instrument (Fig.A. 4 and Fig.A. 5).

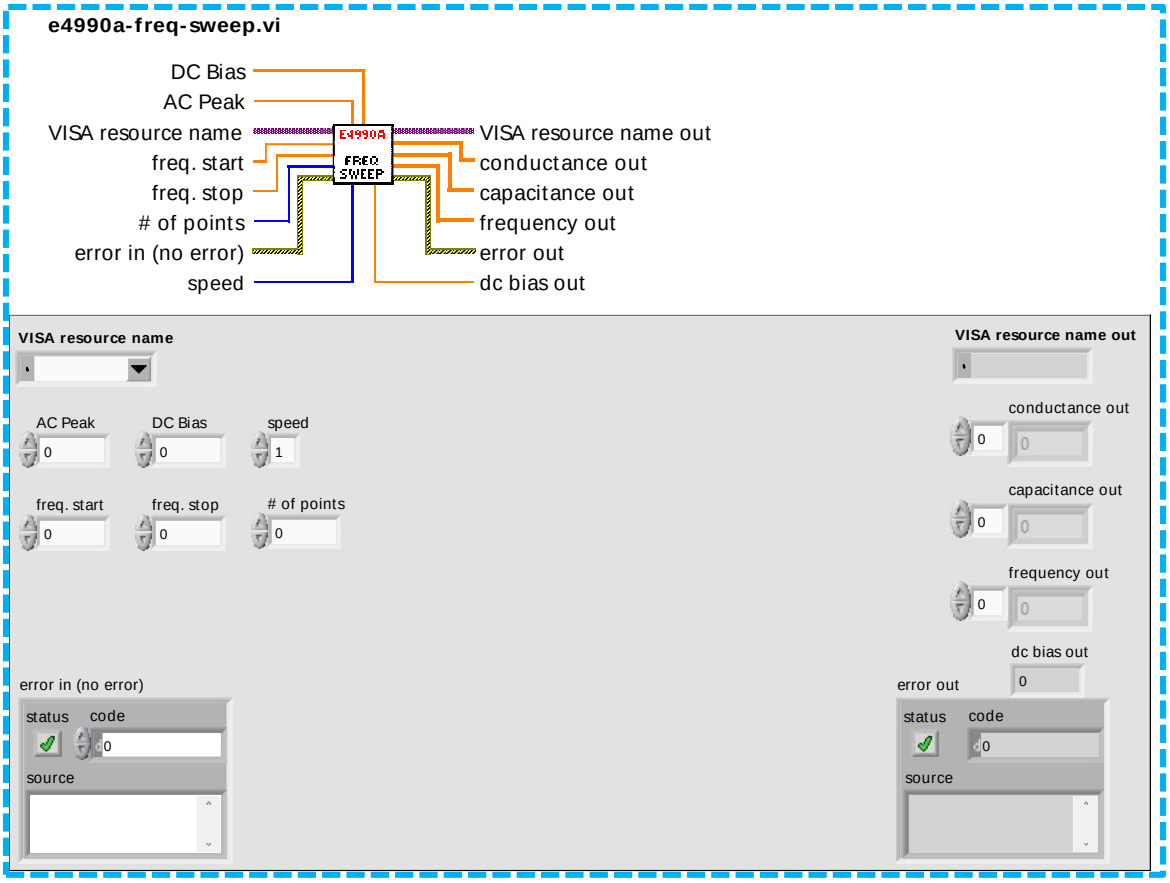

Fig.A. 3 Front panel of frequency sweep.

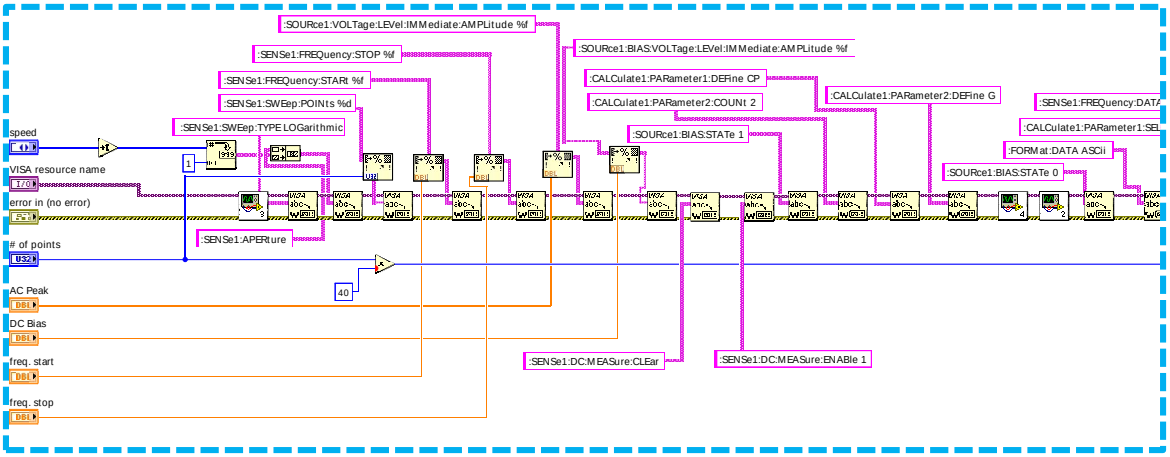

Fig.A. 4 Block diagram of switch program part 1.

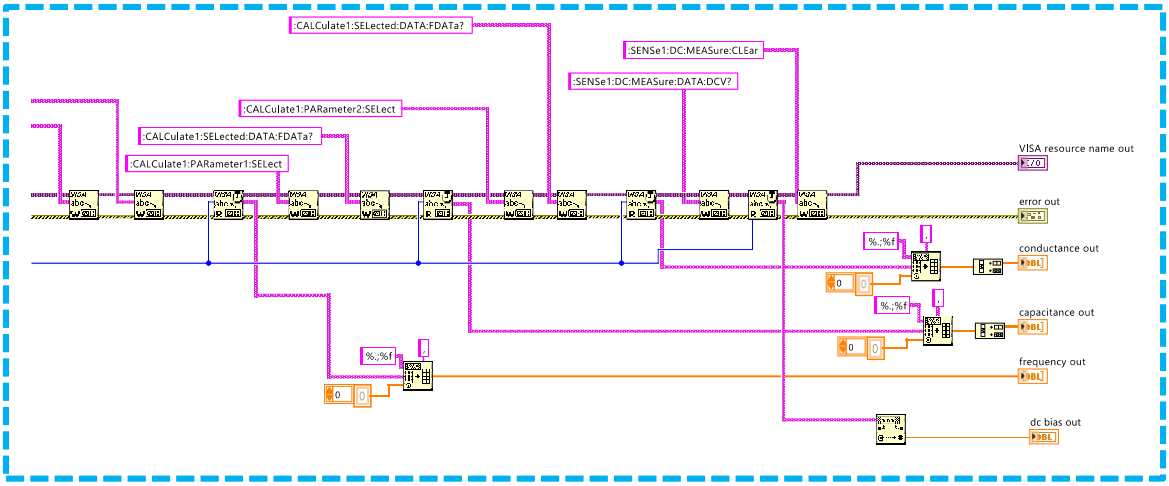

Fig.A. 5 Block diagram of switch program part 2.

A.3 Default Values Program

This VI is being used inside the code of the frequency sweep program and the DC Bias sweep program. It only uses the basic Inputs and Outputs (VISA resource name, error in /out) (Fig.A. 6).

Its function is very simple, it only clears the memory and recalls functions to reset values to the impedance analyzer (Fig.A. 7).

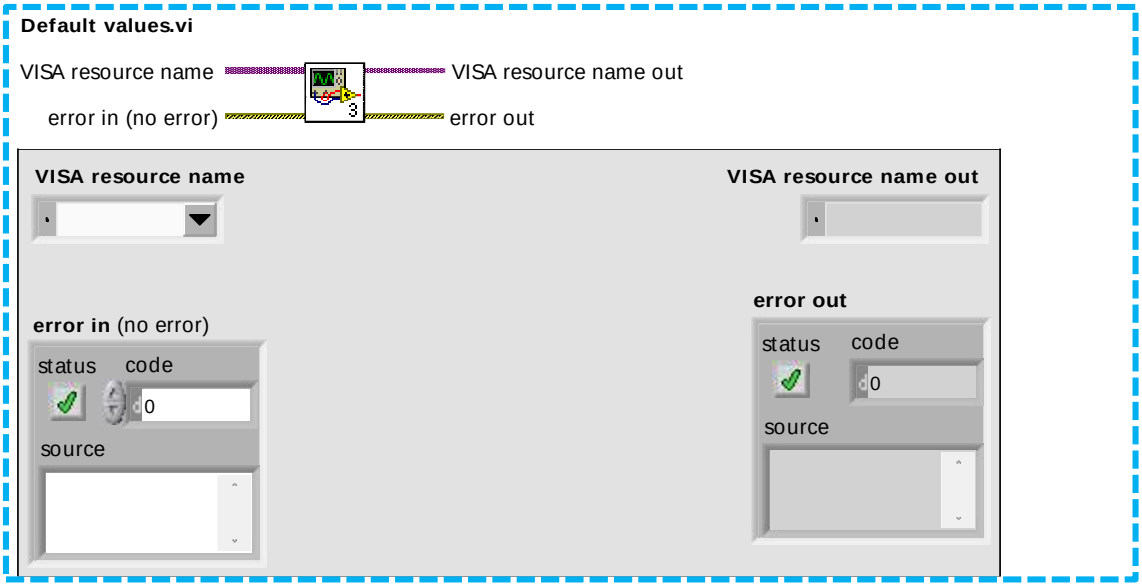

Fig.A. 6 Front panel of Default values.

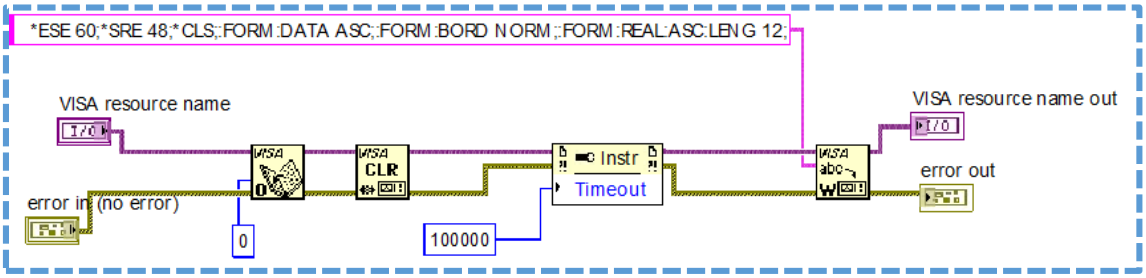

Fig.A. 7 Block diagram of default values.

A.4 Trigger Program

This VI is being used inside of the code of the frequency sweep and the DC Bias sweep program. It only uses the basic Inputs and Outputs (VISA resource name, error in/out) (Fig.A. 8).

This program stops the default continuous trigger mode, sets the parameter for a single trigger mode and execute it (Fig.A. 9).

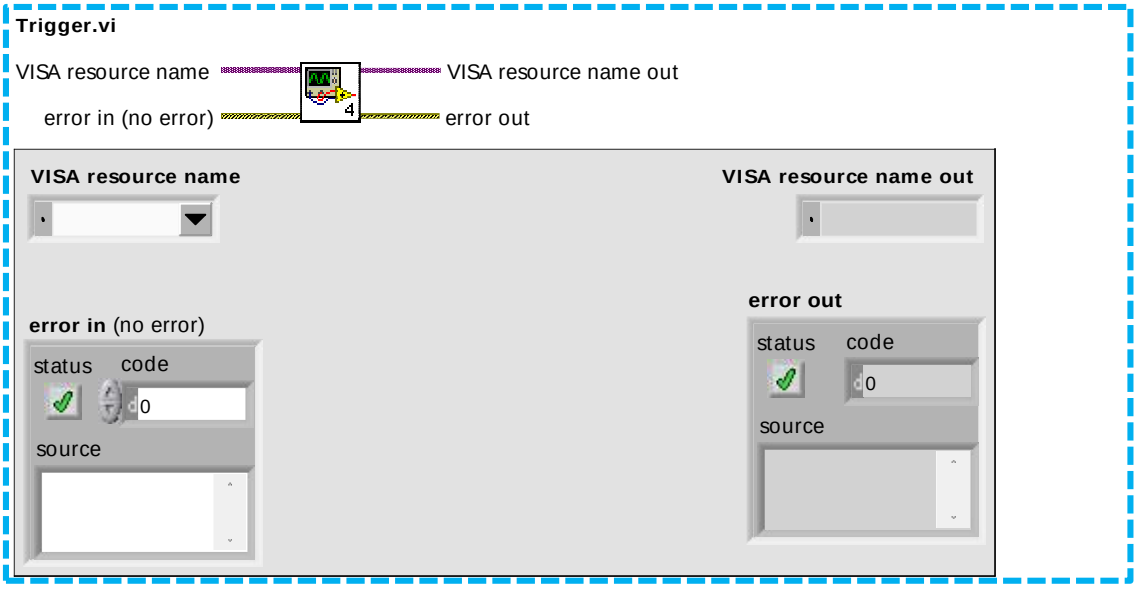

Fig.A. 8 Front panel of Trigger.

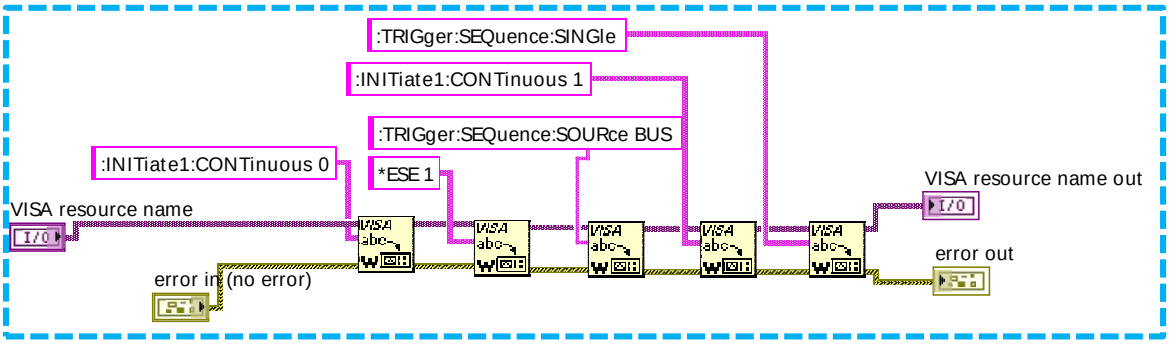

Fig.A. 9 Block diagram of trigger.

A.5 Wait for Response Program

This VI is being used inside of the code for the frequency sweep and the DC Bias sweep program. It only uses the basic Inputs and Outputs (VISA resource name, error in/out) (Fig.A. 10).

This program asks the impedance analyzer for the measurement status every second (Fig.A. 11). As soon as the impedance analyzer finishes the measurement, this VI

will end and the program that controls it will continue with the next step. This is made with the intention to ask for the data as soon as the measurement is done in order to make sure that we are getting the correct amount of data and also in order to not to lose time.

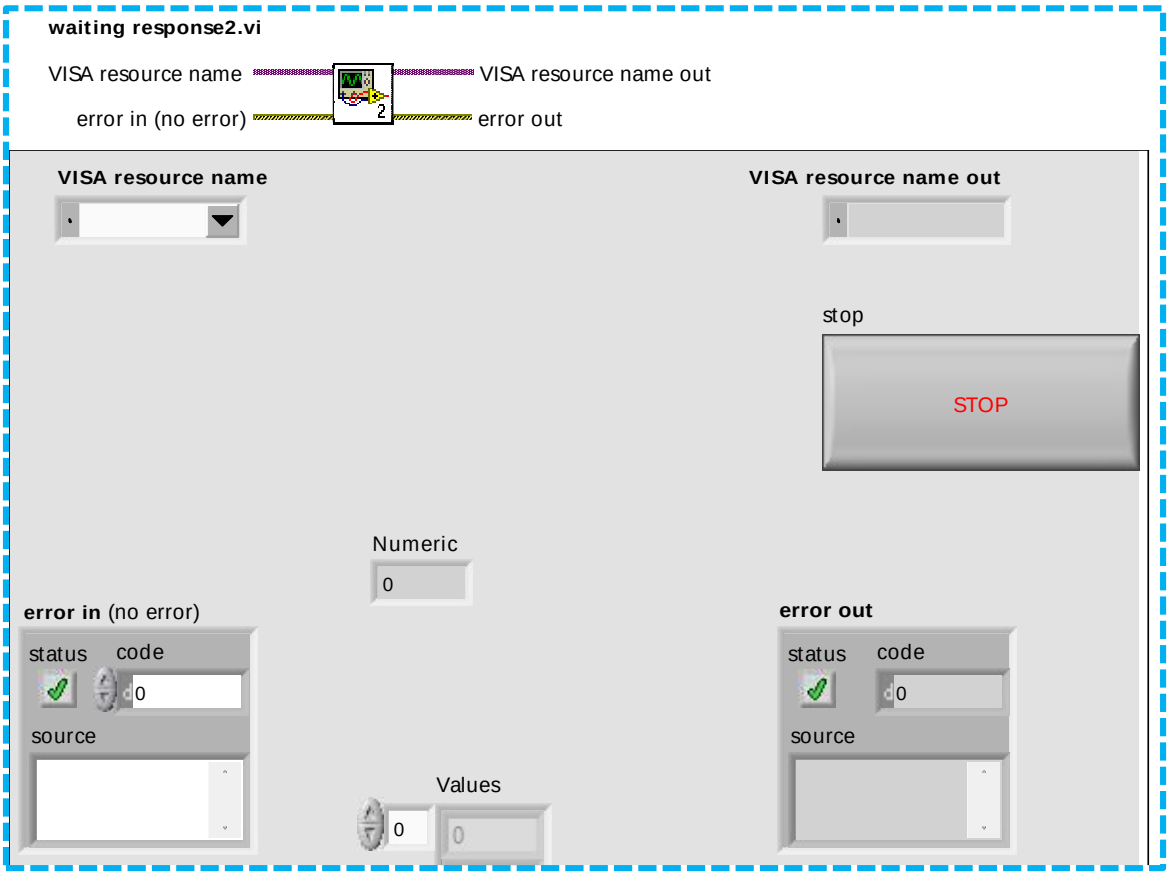

Fig.A. 10 Front panel of waiting for response.

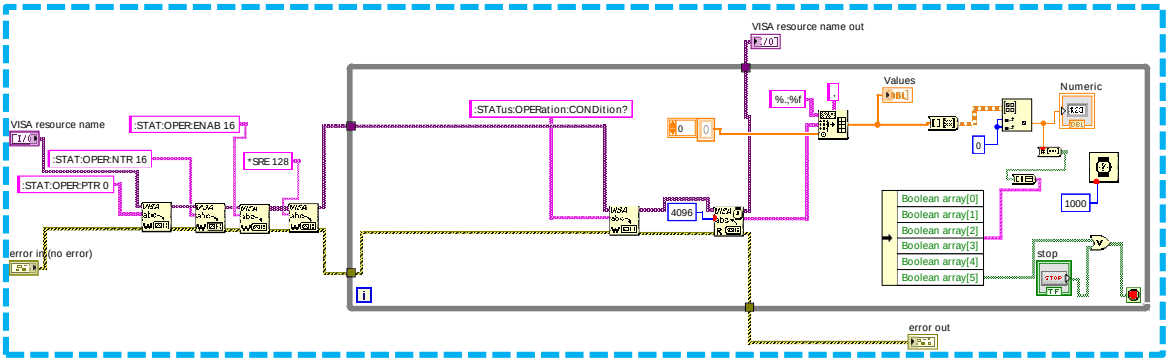

Fig.A. 11 Block diagram of waiting for response.

A.6 DC Bias Sweep Program

This program was created to measure the C-V (Capacitance-Voltage) characteristics of a sample. This VI receives the set points for the measurement (AC peak, frequency, Speed required to perform the experiment, DC Bias start point, DC Bias stop point, number of data points collected, VISA resource name and error in), then it performs a DC Bias sweep with those values and gives back the data with capacitance, conductance and DC Voltage out (Fig.A. 12).

The VI first sets the impedance analyzer to default measurement values. Then it sets the experimental conditions (such as sweep ranges and variables to measure), it then triggers the sweep (separate VI), wait for the measurement to finish (separate VI), and collects the data from the instrument (Fig.A. 13)

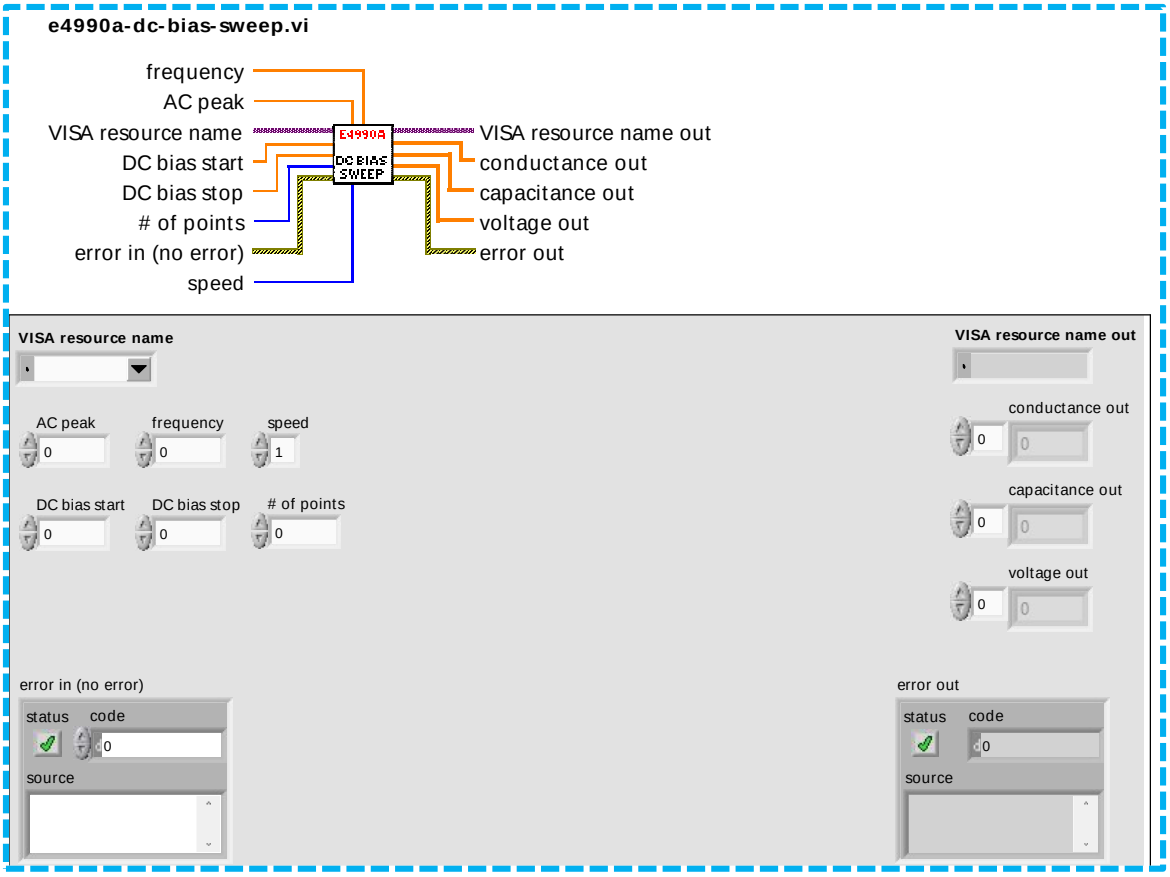

Fig.A. 12 Front panel of DC bias sweep.

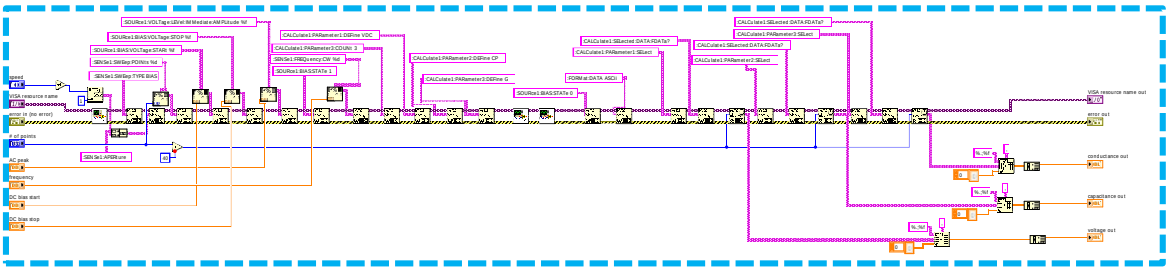

Fig.A. 13 Block diagram of DC bias sweep.

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