INVESTIGATION OF III-V SEMICONDUCTOR HETEROSTRUCTURES FOR POST-Si-CMOS APPLICATIONS

by

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ABSTRACT

Silicon complementary metal-oxide-semiconductor (CMOS) technology in the past few decades has been driven by aggressive device scaling to increase performance, reduce cost and lower power consumption. However, as devices are scaled below the 100 nm region, performance gain has become increasingly difficult to obtain by traditional scaling. As we move towards advanced technology nodes, materials innovation and physical architecture are becoming the primary enabler for performance enhancement in CMOS technology rather than scaling. One class of materials that can potentially result in improved electrical performance are III-V semiconductors, which are ideal candidates for replacing the channel in Si CMOS owing to their high electron mobilities and capabilities for band-engineering. This work is aimed towards the growth and characterization of III-V semiconductor heterostructures and their application in post-Si-CMOS devices. The two main components of this study include the integration of III-V compound semiconductors on silicon for tunnel-junction Esaki diodes, and the investigation of carrier transport properties in low-power III-V *n*-channel FETs under uniaxial strain for advanced III-V CMOS solutions. The integration of III-V compound semiconductors with Si can combine the cost advantage and maturity of the Si technology with the superior performance of III-V materials. We have demonstrated high quality epitaxial growth of GaAs and GaSb on Si (001) wafers through the use of various buffer layers including AlSb and crystalline $SrTiO_3$. These GaSb/Si virtual substrates were used for the fabrication and characterization of InAs/GaSb broken-gap Esaki-tunnel diodes as a possible solution for heterojunction Tunnel-FETs. In addition, the carrier transport properties of InAs <110> channels were evaluated under uniaxial strain for the potential use of strain solutions in III-V CMOS.

CHAPTER 1

Introduction

Continuous scaling of silicon CMOS to keep up with Moore's law presents many challenges as we draw close to the fundamental operational limit of the silicon MOSFET. The cost effectiveness of silicon combined with the extremely mature processing technology have made it one of the most important materials of the 20th century. Even with its cadre of undeniable advantages, the silicon technology still suffers from low optical efficiency and has degraded electrical properties in scaled CMOS devices. On the other hand, III-V semiconductors are ideal for optoelectronic and photonic applications and their high carrier mobilities are ideal for the channel material in future Si based MOSFETs [1]. For the first time, the International Technology Roadmap for Semiconductors (ITRS) roadmap has included the use of compound semiconductors for future implementation in Si CMOS devices. Such implementation would require the deposition of various III-V materials on silicon with low enough surface defects to fabricate surface channel transistors. The integration of III-V compound semiconductors with Si could also combine the cost advantage and maturity of the Si technology with the superior performance of III-V materials.

The replacement of the Si channel in future CMOS with III-V channels showing superior device performance has also driven the development and evolution of a fundamentally different device: the Tunnel Field Effect transistor (TFET) [2, 3]. Most TFET designs involve a *p-i-n* Esaki diode structure where current is modulated by applying a gate bias across an intrinsic region so as to cause an accumulation of carriers, which causes an overlap of the Fermi levels, thereby enabling tunneling across the band gap of

the device [4]. Researchers seem to focus on the device as a whole and not a sum of parts with problems to solve. The first part of this work will focus on successful integration of III-V materials on Si substrates using MBE as the primary growth technique as well as the device performance of III-V heterojunction Esaki diodes to assess the III-V heterojunction as a potential TFET candidate.

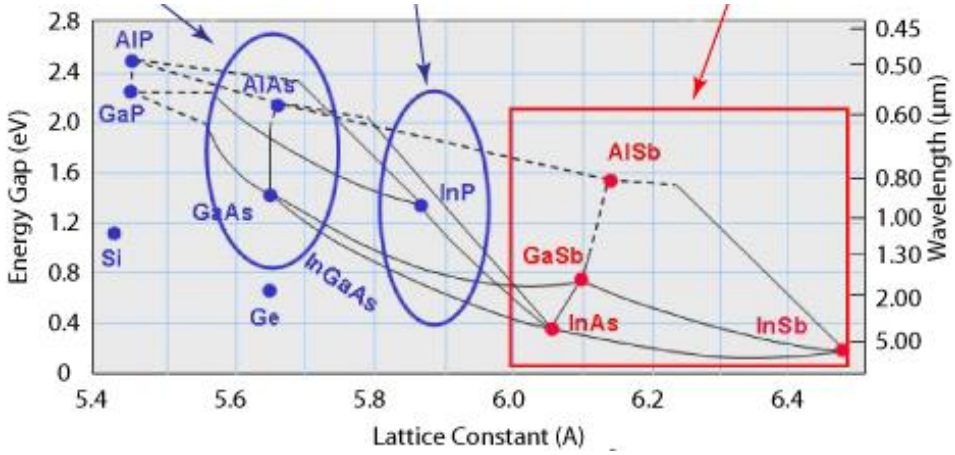

Fig. 1 The energy band gap and lattice constant map for different III-V compounds and the significance of the 6.1 Å family for post-Si CMOS applications. (*Courtesy: Naval Research Laboratory*)

Additionally, III-V semiconductors based around the 6.1 Å lattice constant consist of the group III and group V elements including In/Ga/Al and As/Sb, respectively. These compounds possess small band gaps (e.g., bulk InAs E_g = 0.354 eV) and are ideal for channel materials in next-generation CMOS. The electronic properties of these semiconductors can be strongly influenced by the application of stress via the splitting of the conduction band valleys. In the case of a 2D electron system for semiconductor channels, the occupation and energies of the conduction band valleys can be modified to effect the carrier concentration and mobility by the application of stress [5]. Mainstream Si logic applications employ the use of intentional strain in the Si channels to increase carrier mobility [6]. Up to two times enhancement in hole mobility and drive current is obtained in state-of-the-art *p*-channel silicon transistors using uniaxial strain [7]. Therefore, the

second part of work is geared towards the growth of InAs-based heterostructures for III-V *n*-channel FETs, and Hall transport measurements of InAs channels under uniaxial strain.

In this chapter, a basic review of the epitaxial growth of III-V semiconductors such as GaAs and GaSb on Si substrates using solid-source molecular beam epitaxy (MBE) will be presented. The physical principles behind the MBE technique will also be discussed in detail. Next, various III-V heterojunction band-alignments will be discussed along with the importance of the InAs/GaSb broken-gap tunnel junction for Esaki tunnel diodes and TFETs. A review for the use of strain technology to improve performance in III-V high electron mobility transistors will also be discussed. Finally, a review of each chapter and the overview for this dissertation is presented.

1.1 MBE Growth of III-V Semiconductors on Si

1.1.1 Fundamentals of Molecular Beam Epitaxy

Since its inception in the 1970s by Alfred Cho, molecular beam epitaxy (MBE) has been the primary growth technique for the epitaxial growth of III-V semiconductors [8]. MBE is essentially a growth technique that involves the surface reaction of thermal beams of atoms or molecules on a crystalline surface under ultra-high vacuum conditions. One of the most important and mature technologies developed using MBE is the homoepitaxy of compound semiconductor GaAs. Epitaxial GaAs is usually grown using the evaporation of atomic Ga, and the sublimation of arsenic, which can be both in the dimeric (As_2) or tetrameric form (As_4). The adsorbed As_2 migrates on the GaAs (001) surface in a physisorbed state and the dimers dissociate to get incorporated into the solid phase by binding with Ga atoms on the surface. The others get desorbed in the form of As_2 or As_4 tetramers [9]. The sticking (incorporation) coefficient of group III atoms is usually unity

under normal growth conditions and since Ga adatoms have a surface lifetime of more than 10s, the Ga atoms impinging on the surface undergo surface migration and dissociative chemisorption after interacting with the surface Arsenic species. Under As-rich conditions, the growth of GaAs is kinetically driven by the adsorption of the group V element and the growth rate is controlled is directly influenced by the group III species. The sticking coefficient of group V atoms is usually less than unity as it depends on the group III surface population and arrival rate. The sticking coefficient for As_2 is 1 only when there is complete Ga coverage, and since this is not always the case, usually an excess As_2 flux is required for stoichiometric III-V epilayer growth [10] .

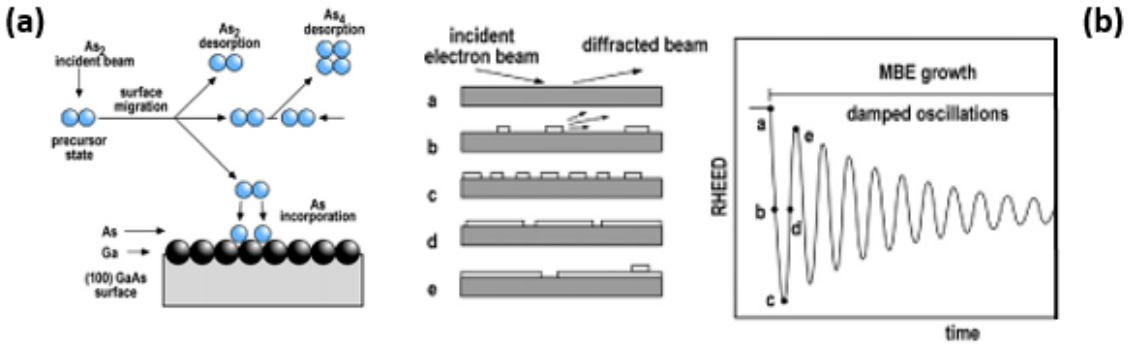

Fig. 2 (a) Incorporation of As atoms on a (100) GaAs surface from incoming As_2 dimers in the following steps: (i) surface migration of the adsorbed molecules (ii) dissociative chemisorption (iii) incorporation into energetically favorable lattice sites (iv) desorption in the form of dimers or tetramers. (b) Different stages of layer-by-layer 2D growth and the corresponding RHEED intensity oscillations. (*Courtesy: Molecular Beam Epitaxy, 1st Ed., M. Henini*)

The ideal growth mechanism for thin epitaxial films is the 2D layer-by-layer or Frank-Van der Merwe (FM) growth mode. Under optimal MBE growth conditions of the ideal surface temperature and ultra-high vacuum environment, monolayer-high 2D islands are formed and these laterally expand until they coalesce and form one complete monolayer. This growth mode is clearly evident through the observation of *in*-situ RHEED oscillations as shown in Fig. 2b. The RHEED oscillations correspond to different amounts

of surface coverage under the FM growth mode and can also be used to ascertain the epitaxial film growth rate by correlating with the period of the oscillations [11]. The adatoms preferentially attach to the surface sites in the FM growth mode, leading to atomically flat films, which is most common in systems with zero or low-lattice mismatch. In contrast with large lattice-mismatch systems, the preferred growth mode is Volmer-Weber (VW) or 3D island growth where the adatom interactions are much greater than that of the adatom-surface, leading to the formation of three-dimensional clusters. The coalescence of these islands with continued growth yields extremely rough films and interfaces. A third growth mode is the Stranski-Krastanov (SK) mode, which is a combination of both 2D layers and 3D islands. Depending on the lattice mismatch between the film and the substrate, as well as the MBE growth conditions, epitaxy can be performed under any of these three different growth modes [12].

The use of UHV conditions in the MBE technique allow for the use of a molecular flow regime of the incident atoms as opposed to a viscous regime in competing techniques like MOCVD. The mean free path (λ) is defined as the average distance travelled by an atom between successive collisions. In the molecular flow regime, the mean free path of the atoms is much larger than the critical dimensions of the growth chamber (distance between the cell and substrates is <0.3 m). Since the incoming atoms do not interact with each other during their paths to the substrate, mechanical shutters are used to turn the molecular/atomic beams on and off on the order of 0.1s. This allows abrupt control of thickness, doping, composition and hetero-interfaces down to a tenth of a monolayer. According to the kinetic theory of gases, the mean free path between collisions of atoms or molecules at a given pressure p is given by the expression:

$$\lambda = \frac{k_B T}{\sqrt{2}\pi p D^2} \qquad (1)$$

where k_B is the Boltzmann's constant, T is the temperature, and D is the diameter of the incoming atoms in the molecular beam. For pressures as low as 10^{-6} Torr in the UHV regime and typical MBE molecular beams, the typical value of λ is around 5 m. In comparison to techniques like MOCVD where the chamber pressure is on the order of 10 Torr and λ is around 50 μm, the gas flow is viscous and not molecular. In a viscous gas flow regime, the existence of a boundary layer (or stagnant layer) controls the mass transport of molecules, which take places through diffusion. Since different chemical species can have different diffusion coefficients, they reach the substrate surface at different times and this can lead to uncontrolled composition, doping and interface layers. Therefore, MBE is still a superior technique for producing III-V semiconductor heterostructure with different alloy compositions and abrupt interfaces for quantum confinement.

1.1.2 Basics of the MBE Technology

A basic MBE system consists of a stainless steel growth chamber equipped with effusion cells to produce molecular beams, mechanical shutters, and substrate holder with a heater, and a load-lock section for the introduction of wafers into the MBE system (Fig. 3b). Typical base pressures of 10^{-10}-10^{-11} Torr are reached using a combination of ion pumps, cryopumps, titanium-sublimation pumps, and LN_2 cryopanelling. An electron gun with a phosphor screen is used for *in-situ* RHEED analysis, and a quadrupole mass spectrometer is used to monitor the partial pressures of the background species. The cryopanels also provide thermal insulation among the different K-cells, which are located close to each other and have varying temperatures (200 ^{o}C – 11 00 ^{o}C). The substrate holder

is mounted on the wafer manipulator which rotates on an axis perpendicular to the axis of the cell flange, so the substrate and ion gauge can be faced towards the molecular beam for growing and measuring the incident molecular flux via the beam equivalent pressure (BEP).

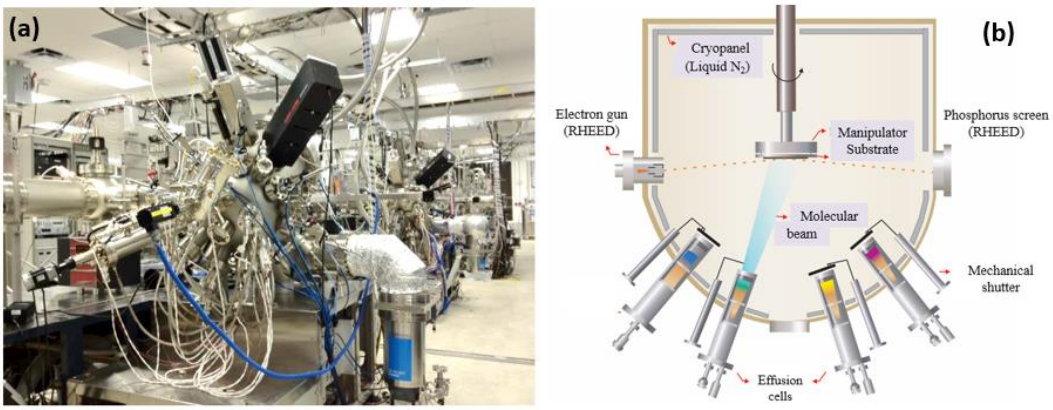

Fig. 3 (a) III-V MBE chamber at Texas State University in a UHV buffer line configuration. (b) Schematic of a typical MBE growth chamber with effusion cells, shutters, *in-situ* RHEED and LN_2 cryopanelling.

The MBE technique is essentially a physical-vapor deposition technique, where the source material is contained in a high-purity pyrolitic Boron nitride (PBN) crucibles. These crucibles are radiatively heated using Ta ribbons or wires, which are heated using the Joule effect. The cells are surrounded by radiation shields made of Ta foils in order to provide thermal insulation and cross talk between adjacent effusion cells. The incident flux from the Knudsen-cells can be measured by BEP measurements using an ion gauge, or from growth rates using RHEED intensity oscillations. For group V species, valved cracker cells are very common as they produce molecular beams with very fast time response and accurate beam intensity. The high-temperature cracker section transforms the tetrameric species to dimers, which is believed to have a more favorable surface kinetic profile. The measurement of the molecular beam fluxes is important as the group-V to group-III flux ratio controls the surface reconstruction and stoichiometry in GaAs. The flux ratio of two

different species can be calculated by measuring the BEP using an ion gauge for the individual species [13]:

$$\frac{\Phi_i}{\Phi_j} = \frac{p_i}{p_j}\frac{\eta_i}{\eta_j}\left(\frac{T_i M_i}{T_j M_j}\right)^{1/2} \qquad (2)$$

where Φ_k, p_k, T_k, and M_k are the flux, BEP, absolute temperature and the molecular weight of the species *k (k = i, j)* and η_k is the ionization constant relative to nitrogen.

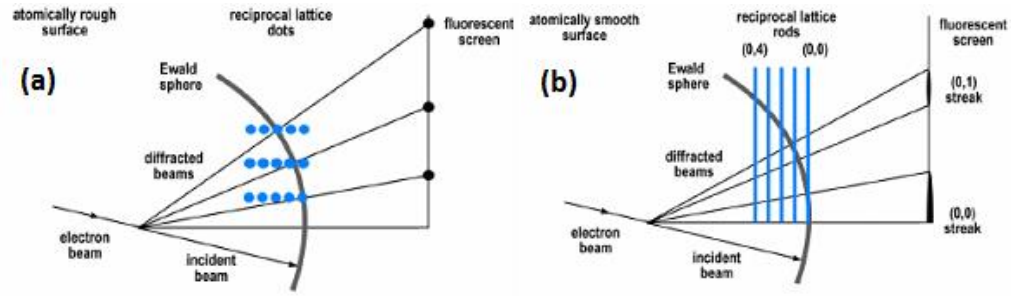

Fig. 4 Schematic representation of the origin of RHEED patterns from (a) atomically rough surfaces given by reciprocal lattice points and (b) atomically smooth surfaces given by reciprocal lattice rods, respectively. The intersection of the Ewald sphere with reciprocal lattice spots or streaks is shown on the fluorescent screen. (*Courtesy: Molecular Beam Epitaxy, 1st Ed., M. Henini*)

Reflection high-energy electron diffraction (RHEED) is an *in-situ* electron diffraction technique that has become an essential diagnostic component of the MBE technique over the years. It basically consists of an electron gun with energies from 10-50 keV, incident on the sample surface at a grazing incidence angle and the diffraction pattern from the sample surface is captured on a fluorescent screen. Under different surface reconstructions, the conditions for constructive interference from the 2D surface lattice are given by the Laue's law, which states that, the wave-vectors of the incident and diffracted electron beam must differ by reciprocal lattice vector. In case of atomically smooth surfaces, the reciprocal lattice consists of parallel lines representative of a 2D lattice and for atomically rough surfaces, the reciprocal lattice is made up of points, representative of a 3D lattice (Fig. 4). The RHEED patterns are representative of the growth mode and can

be distinguished as being streaky with integer and fractional streaks, or spotty for rougher surfaces.

1.1.3 Heteroepitaxy of III-V Semiconductors on Si

While homoepitaxy is the growth of a specific compound on top of a crystalline substrate of the same material, heteroepitaxy involves the growth of a crystalline material A on top of crystalline material B. More often than not, heteroepitaxy is lattice-mismatched which means that the lattice constants of the substrate and the film are different. The lattice mismatch can be defined as follows:

$$f = \frac{a_s - a_l}{a_s} \qquad (3)$$

where a_s is the relaxed lattice constant of the substrate, and a_l is the relaxed lattice constant of the epitaxial layer on top. The strain in the system can be either compressive ($f < 0$) or tensile ($f > 0$). For small lattice-mismatch systems ($|f| < 1\%$) with two-dimensional growth mode, the initial growth is pseudomorphic where the in-plane lattice constant of the film is the same as the lattice constant for the substrate. The pseudomorphic layer is tetragonally distorted as the out-of-plane lattice constant is different from the in-plane lattice constant. Increasing the thickness of this epilayer leads to an increase in strain energy, and at some critical thickness the strain energy is released in the form of dislocations leading to unwanted structural defects in the film.

For the growth of III-V materials such as GaAs and GaSb on Si, several problems exist which include the large lattice-mismatch, thermal mismatch, and the growth of polar on non-polar material. The large lattice-mismatch of 4% between GaAs and Si leads to the initial nucleation of GaAs on Si in the form of islands rather than a layer-by-layer growth. The Frank Van-der-Merwe (FM) growth mechanism requires the substrate surface energy

to be greater than the sum of the film and the interface surface energy for successful wetting of the surface. However, in the case of GaAs on Si, the substrate energy is low enough which leads to a Stranski-Krastanov (SK) growth mechanism due to the decrease in the energy of elastic deformations in the 3D islands as well as the low substrate surface energy which prevents the successful wetting of Si by GaAs.

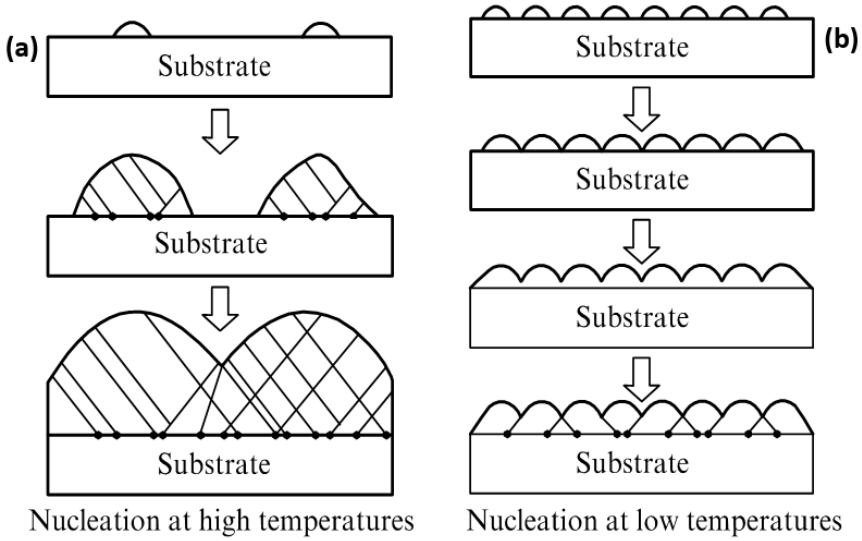

Fig. 5 (a) At high growth temperatures, the GaAs islands form misfit dislocations before coalescing (b) At low temperatures, the islands grow pseudomorphically until they coalesce and then form the dislocations with continued growth. [14]

The island growth of GaAs is pseudomorphic and the island edges are the points where most of the stress is present and these are the regions where dislocations nucleate. Continued growth leads to the coalescing of islands, which produces a high dislocation density in the epitaxial GaAs layers in the form of misfit and threading dislocations (Fig. 5). However, by using a low temperature of 400 ^{o}C for initial nucleation of GaAs on Si, the islands can be grown without significant interface defects and the threading dislocations originating from the coalescing of the islands can be mitigated to a certain extent through the use of high temperature (~600 ^{o}C) [14].

Many different techniques have been employed to improve the quality of epitaxial GaAs on Si. One of these techniques involves the growth of epitaxial Si before GaAs growth as the native Si surface can contain contaminants such as adsorbed carbon and native oxide. A clean Si surface provides higher quality growth of GaAs on Si [15]. Several buffer layer techniques have also been employed to relieve the immediate stain between the GaAs/Si system including graded Si-Ge, GaAsP, and InGaP layers. Additional *in*-situ thermal cyclic-annealing (TCA) as well as post-growth anneal have also been used to reduce the dislocation density in GaAs epilayers as a result of dislocation mobility and annihilation [16]. Amorphous GaAs layers grown at 100 ^{o}C have also been used followed by the high-temperature growth of GaAs, followed by TCA to produce films with dislocation densities on the order of 10^{6} cm^{-2}. Strained-layer super-lattices (SLS) have also been employed to bend the vertically propagating threading dislocations at the strained interfaces, leading to lower defect densities in the active GaAs epilayer[17]. Migration-enhanced epitaxy has also been used at temperatures around 300 ^{o}C for producing GaAs films with low defect densities in conjunction with GaAs/InGaAs SLS [18]. A good metric for judging the crystalline quality of the GaAs grown on Si (001) using MBE is the full-width at half-maximum (FWHM) of the (004) rocking curve as it is directly related to the defect density in the GaAs film. Thicker GaAs films also show lower FWHM values as the number of total reflecting (004) planes increases with film thickness. For GaAs films on Si which relax after the initial pseudomorphic growth of islands in the SK mode, the introduction of defects leads to lower number of perfectly aligned (004) planes, leading to a higher FWHM.

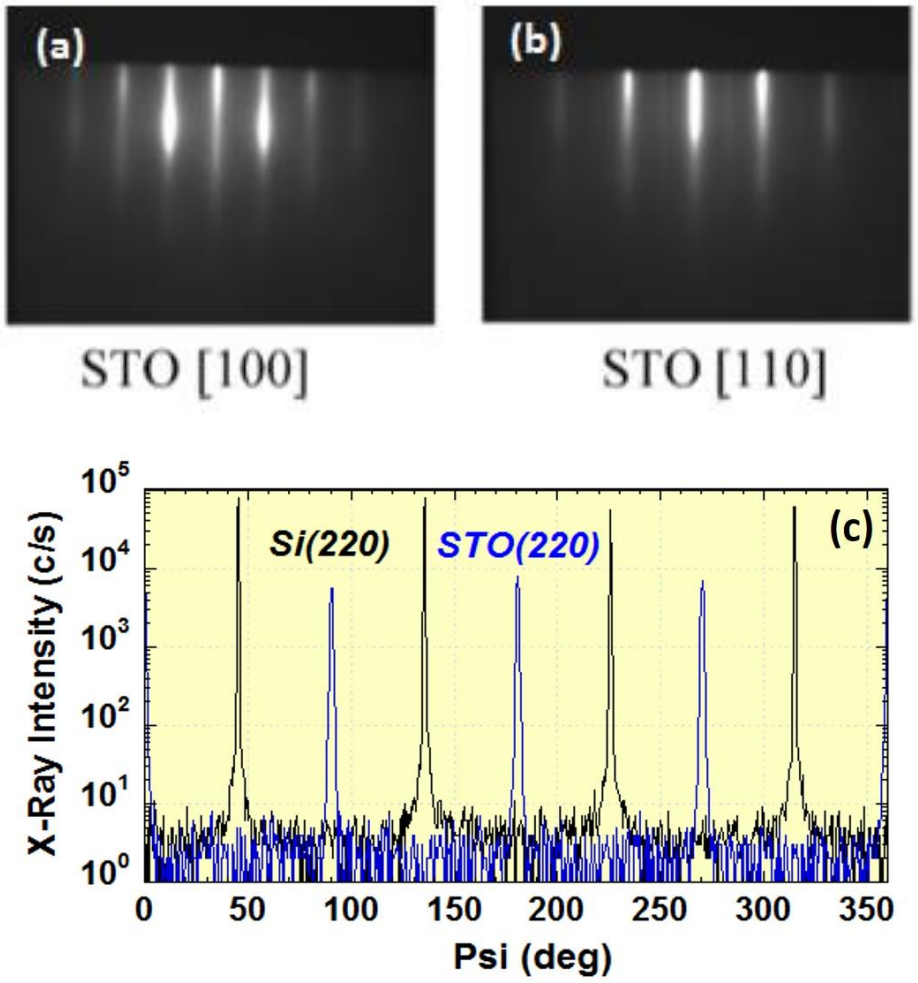

Fig. 6 (a) RHEED images after the growth of 40Å SrTiO3 on Si along the (a) [100] and (b) [110] azimuth. (c) X-ray psi scan of the STO and Si (220) planes showing the in plane epitaxial relationship where the STO peaks are exactly 45° off from the Si peaks [19].

Another interesting buffer layer approach developed by Droopad *et al* is the use of a crystalline perovskite oxide named $SrTiO_3$ (STO). The $SrTiO_3$ lattice (a_{STO} = 3.905 Å) undergoes a 45° rotation to accommodate the high lattice mismatch with the underlying Si (001) (a_{Si} = 5.431 Å) leading to a strain of 1.7%. The GaAs lattice (a_{GaAs} = 5.653 Å) grown is now strained 2.4% with respect to the 45° rotated $SrTiO_3$ lattice, thereby enabling the reduction from the original 4% strain for the GaAs/Si system. The first step in this approach is the successful growth of a crystalline STO lattice on top of a clean Si surface [19]. Since this approach involves the growth of an oxide using either molecular oxygen or oxygen

plasma, the Si surface is easily prone to oxidation leading to the formation of amorphous SiO_2. This defeats the purpose of the epitaxial growth of crystalline STO on a Si (001) surface. Therefore, a Sr-deoxidation process is used to remove the native oxide and form a Sr-passivated Si surface that shows a (2 × 1) surface reconstruction [20]. This is followed by the co-deposition of Sr and Ti in the presence of oxygen flux, which leads to streaky RHEED features along the [100] and [110] azimuths as shown in Fig. 6. An XRD psi-scan also shows the in-plane relationship where the Si (220) planes are oriented at an angle of 45^o with respect to the STO (220) planes. The high quality growth of crystalline STO on Si (001) is made possible by the layer-by-layer growth of STO in the FM growth mode. As mentioned earlier, the successful wetting of STO plays a crucial role in the 2D growth of this crystalline oxide on Si. The surface energy for (2 × 1) reconstructed Si is 1710 erg/cm^2 and the surface energy of STO depends on the surface termination. In the case of an SrO terminated STO surface, the energy is 800 erg/cm^2. For successful wetting, the interface energy needs to be less than 900 erg/cm^2, and this is achieved by having a (2 × 1) 1ML of Sr at the interface leading to an interface energy of 574 erg/cm^2 according to DFT calculations [21]. This proves the fact that the growth of stoichiometric STO on a Sr-terminated Si surface avoids island-growth, which is common in high lattice-mismatch systems as the wetting conditions allow layer-by-layer growth. After the thermodynamic condition of wetting is met, the kinetic conditions has to be met to allow enough adatom mobility on the surface so that the constituent atoms can reach their correct lattice sites, which in this case is done by the sue of high temperature. Fig. 7 shows *in-situ* RHEED oscillations observed during the growth of STO on Si (001), indicating layer-by-layer growth and a growth rate of 1 unit cell in approximately 2 minutes (0.195 nm/min).

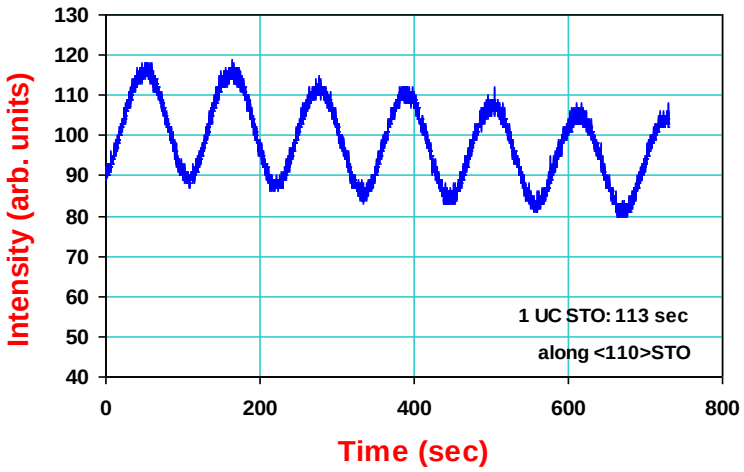

Fig. 7 RHEED oscillations observed during the growth of STO on Si (100) indicating layer-by-layer growth and a growth rate of 1 unit cell in approximately 2 minutes (0.195 nm/min).

The second step is the successful 2D growth of GaAs on the STO surface. This is accomplished by the co-deposition of Ga and As_2 on the STO surface. As in the previous case, the surface energy of STO plays an important role in the successful wetting of GaAs on the STO/Si(001) substrate. GaAs epitaxial films show extremely low defect densities as detailed by etch pit density calculations and the XRD analysis shows the presence of highly crystalline GaAs. Largeau *et al*. have shown the formation of GaAs islands on TiO_2-termiated STO, showing that the STO surface energy is not enough to allow complete wetting of GaAs for FM growth [22]. Therefore, additional interface engineering is needed to lower the interface energy and the GaAs surface energy, to allow for successful wetting of STO with GaAs and optimize the quality of Gas on STO/Si(001).

One of the earliest works on the heteroepitaxy of GaSb on Si (001) showed the use of a thin AlSb buffer layer to obtain optical quality GaSb films with FWHM as low as 215 arcsecs for the (004) XRD rocking-curve [23]. Numerous other studies have shown improvement in the film quality of GaSb by inserting an AlSb buffer layer on Si (001). Direct growth of GaSb on Si produces 3-D islands as the result of high GaSb surface energy

as well as the 12% lattice-mismatch. However, by inserting AlSb islands that are much smaller owing to the smaller diffusion length of Al on the surface as compared to the Ga adatoms, the subsequent GaSb island growth is suppressed and this leads to smoother epitaxial films (Fig. 8a) [24]. The growth of AlSb on Si occurs under the SK growth mode where initial formation of 3-D islands with {111} facets are truncated on the top with (100) planes. However, the AlSb islands create lower number of dislocations and defects due to the stronger bonding between Al-Sb as compared to Ga-Sb [25].

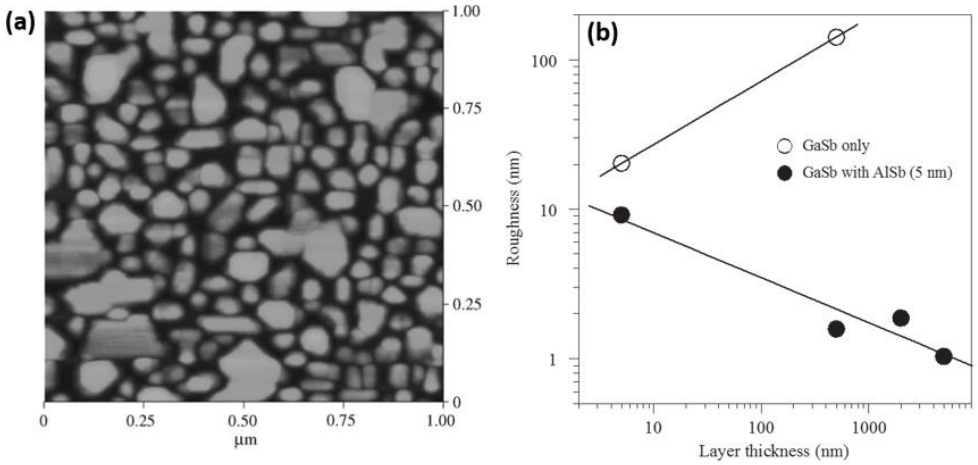

Fig. 8 (a) AFM image of the surface of 5-nm-thick GaSb grown after the formation of 5-nm thick AlSb islands on Si substrate. (b) Surface RMS roughness dependence as a function of the GaSb film thickness shows the importance of the 5 nm AlSb buffer layer. [24]

Balakrishnan *et al.* have performed extensive studies on the growth of AlSb on Si using the interfacial misfit dislocation (IMF) array technique where a 2D periodic array of pure-edge type dislocations are formed at the AlSb/Si interface, relieving most of the strain at the interface in an arranged manner, leading to strain free growth of AlSb and subsequent growth of GaSb [26]. This technique makes use of the arrangement of atoms on the surface to relieve strain in a controlled manner even before the critical thickness is reached [27]. Similar studies have also shown high quality growth of GaSb on GaAs where the Sb atoms

self-assemble on the GaAs surface under the right growth conditions and the Ga-Sb bond is skipped every 13th lattice site to relieve the strain using a periodic arrangement [28].

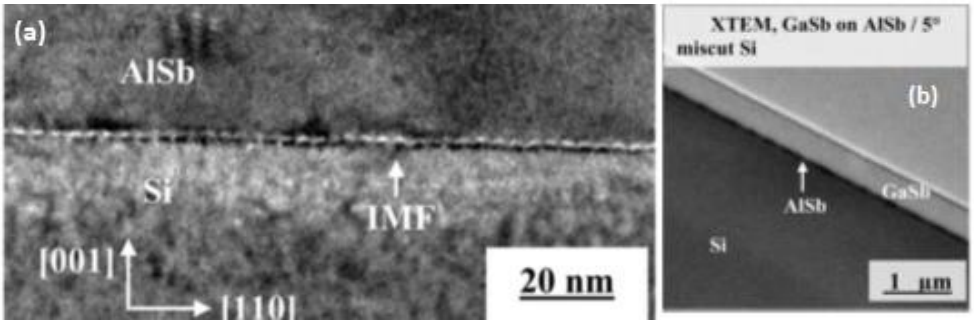

Fig. 9 (a) Cross-sectional TEM image of AlSb grown on a 5^{o} miscut Si (001) substrate showing the periodic IMF array. (b) High-quality GaSb grown on the Si using the IMF AlSb buffer layer. [27]

For the IMF growth of AlSb on Si, an initial soak of Al enables the Al-Si bond formation, while the Sb soak results in a 2D reconstruction result in the formation of an IMF array. This involves the surface packing of Sb atoms such that they skip every 9th Si atom on the substrate. Therefore, a misfit dislocation appears for every 8 AlSb lattice sites and 9 Si lattice sites, creating a periodic arrangement in the [110] and [-110] directions. Additional anti-phase domain boundaries (APDs) resulting from the growth of AlSb on Si can be suppressed by the use of miscut wafers, which exhibit double atomic-step edges [27]. A high-resolution TEM image at the AlSb-Si interface shows the misfit dislocations identified by the contrast adjacent to the high and low-strain regions (Fig. 9a). Fig. 9b also shows high quality GaSb grown on Si using an IMF AlSb buffer, where defect densities as low as ~ 7×10^{5} cm^{-2} and APD densities of $<10^{3}$ cm^{-2} have been obtained.

1.2 Band-Engineering for III-V Heterojunctions

The Tunneling-field-effect-transistor (TFET) has emerged as an alternative to traditional Si CMOS by enabling the scaling of the supply voltage (V_{DD}) for low power and energy efficient computing due to its sub 60-mV/decade operation. Unlike MOSFETs, the

source-drain design in TFETs is asymmetric as it is essentially as reverse biased *p-i-n* Esaki diode. The drive current generation is based on band-to-band tunneling (BTBT) at the source-channel junction, where the tunneling barrier effectively filters the high-energy carriers at the tail of the Fermi-Dirac distribution. The key challenges for TFETs at this point are high on-state current which is limited by the tunneling probability at the tunnel junction, and the steep subthreshold slope (SS) which is degraded by trap-assisted tunneling (TAT). Therefore, it is important to engineer a junction that reduces the effective tunneling barrier and possesses a defect-free interface, which suppresses TAT and enables a steep SS and high I_{on}/I_{off} ratio. III-V heterojunctions are ideal candidates for TFETs as they possess a direct band gap and low effective carrier masses (m^*) and the hetero-band alignment can be tailored to achieve high tunneling probability (T_{WKB}) at low voltages [29].

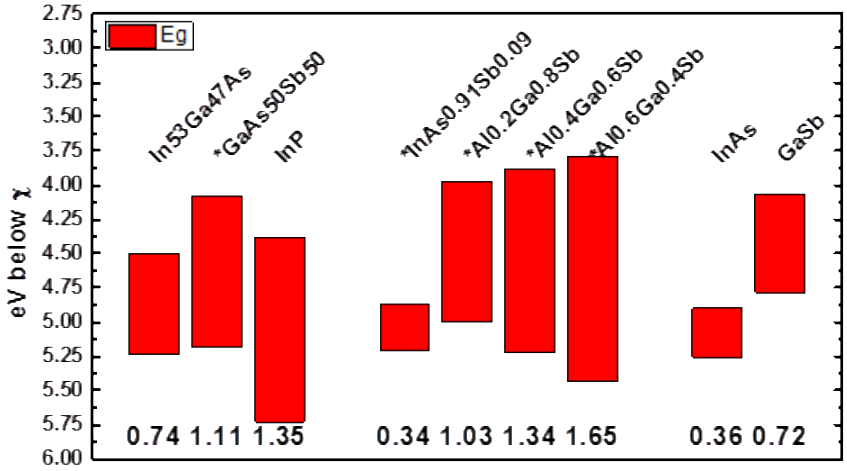

Fig. 10 Heterojunction band line-ups for several binary and ternary compound semiconductors ranging from Type-I (straddling-gap), Type-II (staggered-gap), and Type-III (broken-gap) junctions.

Previous work has demonstrated the application of many III-V heterojunctions for both *n*- and *p*-type TFETs. Different band alignments including type-II and type-III have been used to produce on-state currents on the order of traditional Si-CMOS. A complete review of the published data for TFETs in Fig. 11 shows the feasibility of TFETs as a

possible replacement for the 16 nm Fin-FET CMOS architecture [30]. Even though high on-currents have been achieved in *n*-TFETs, the technology still suffers from low on-current for *p*-TFETs as well as low subthreshold slope.

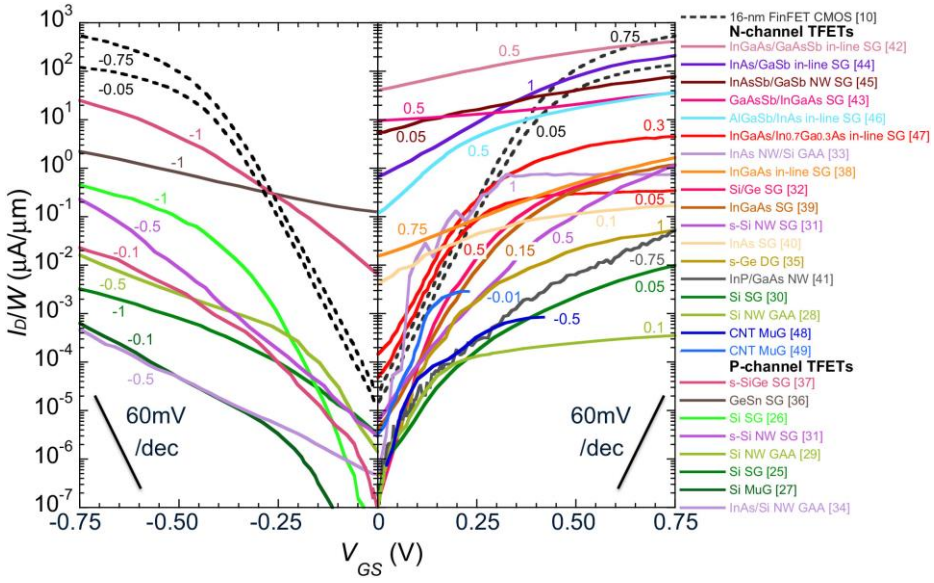

Fig. 11 Comparison of published TFET drain current per unit width versus gate-to-source voltage for *p*-channel (left) and *n*-channel (right) transistors. Dashed lines indicate experimental 16-nm low-power FinFET CMOS technology. Included devices exhibit SS < 60 mV/decade or NDR in the forward direction. The curves are shifted so that the gate voltage where the steepest sub-threshold slope occurs is at the origin.[30]

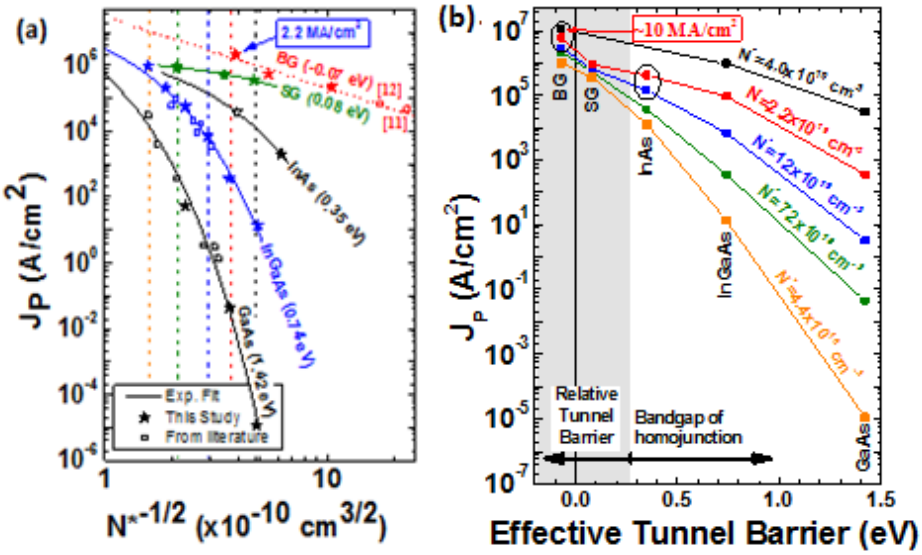

Fig. 12 (a) Peak current density of various hetero- and homo-junctions plotted as a function of the effective doping N^*. (b) Peak current density plotted as a function of effective tunnel barrier for different band alignments, showing that broken-gap system can experimentally achieve the maximum J_P.

Among all the possible III-V heterojunction combinations, the InAs-GaSb broken-gap system has the highest tunneling probability due to one of the lowest effective tunneling barriers. Simulation results have shown subthreshold slopes as low as 7 mV/decade [31] and drive currents as high as 1.9 mA/μm at V_{DD} = 0.4 V [32]. However, experimental data for TFETs has shown a steepest room-temperature subthreshold slope of 125 mV/decade, and a maximum on-current of 180 μA/μm at V_{DD} = 0.5 V due to materials defects at the tunnel junction, poor gate oxide interface, TFET geometry, and other series resistances [33]. There has also been a lot of published work based on the InAs-GaSb type-II superlattice system for long-wavelength infrared (LWIR) detectors [34]. These studies have focused on improving the interface quality of the InAs/GaSb system, strain compensation and dislocation formation to improve the electrical performance of these devices [35]. Pawlik *et al.* have also performed detailed studies comparing the peak current density (J_P) of the Esaki tunnel diodes based on various homo- and heterojunction band line-ups. Fig. 12 shows the effect of N^* ($=N_AN_D/N_A+N_D$) and the effective tunneling barrier on J_P, and experimentally shows that the InAs/GaSb heterojunction can be used to attain the highest tunnel current densities [36].

1.3 Advanced Strain Solutions for III-V *n*-channel FETs

Traditional planar Si CMOS technology has widely adopted the use of both uniaxial and biaxial strain for improving both *n*- and *p*-channel MOSFETs. The 90 nm technology node employed the use of strained Si-Ge source-drain (S/D) were used to generate compressive strain in the Si channel and enhance hole mobility and increase drive current for *p*-MOSFETs [37]. Similarly, carbon-doped Silicon (Si:C) S/D stressors [38] were used to enhance electron mobility using local tensile strain and increase I_{on} for *n*-MOSFETs

(Fig. 13). The mobility enhancement obtained by applying strain can provide higher carrier velocities in the MOS channels, as well as higher drive currents under a fixed supply voltage and gate oxide thickness.

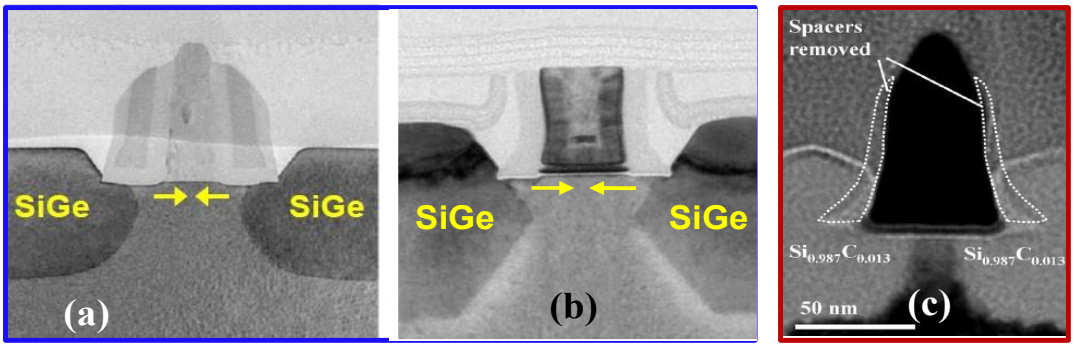

Fig. 13 Cross-sectional TEM views for (a, b) *p*-MOSFET using embedded Si-Ge as S/D and (c) *n*-MOSFET using Si:C as S/D. [37, 38]

For both the drift model and quasi-ballistic transport model in MOSFET channels, the low-field carrier mobility is one of the main factors that controls the drive current in both long and short-channel devices. In both models, the drive current is directly proportional to the product of the carrier mobility (μ) and the channel carrier concentration (N_s) [39]. For *n*-channel FETs, the electron mobility can be enhanced by the application of uniaxial tensile strain as it reduces the electron effective mass (m_e^*). Strain can also effectively increase the concentration of carriers in the channel by repopulating the valleys under the application of uniaxial stress in some cases [40].

III-V materials in general possess smaller effective masses than Si, which leads to increased carrier mobility and higher injection velocities. However, these compounds suffer from low density of states (DOS) in the Γ-valley, which leads to a reduction in the inversion layer charge and low drive currents. For instance, although InAs has six-times the electron injection velocity of Si, its inversion layer charge (Q_{inv}) is only one-third of a Si channel [41]. Therefore, it is important to improve the performance of III-V FETs for

high-volume manufacturing (HVM). As for Si CMOS, mechanical strain can be used as a performance booster for III-V transistors and enable the introduction of this technology in logic applications.

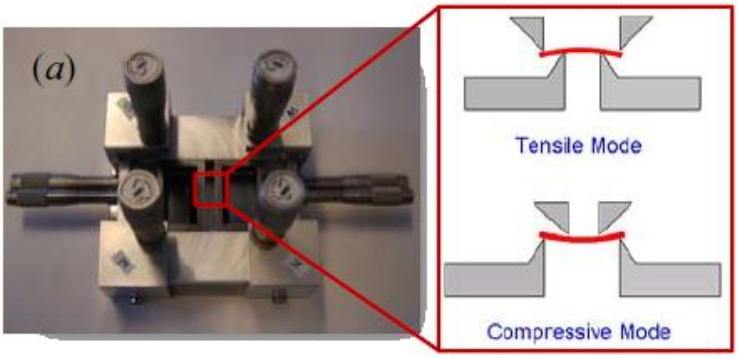

Fig. 14 (a) Picture of a common chip-bending apparatus used for mechanical tensile and compressive strain. [42]

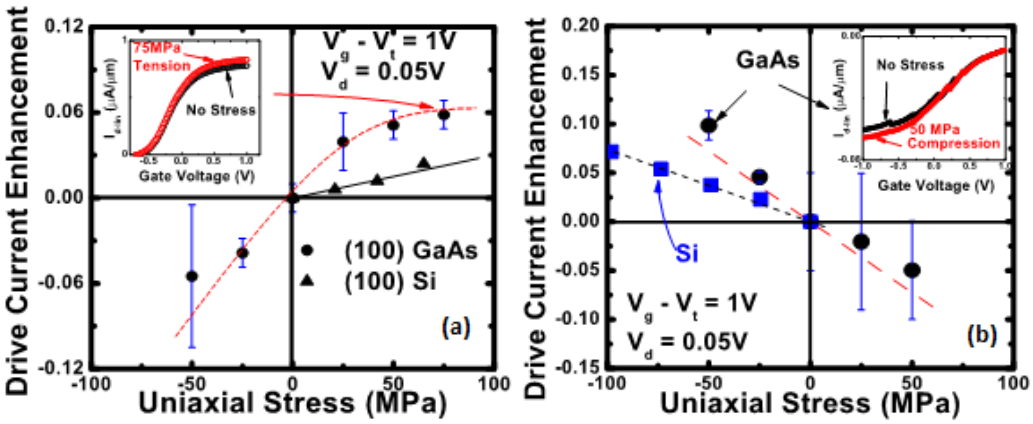

Fig. 15 Drive current enhancement in (100) GaAs (a) *n*-MOSFET with uniaxial tensile stress and (b) *p*-MOSFET with uniaxial compressive strain as compared to Si. [43]

Wafer bending experiments are the most common tool for assessing the effect of uniaxial strain on semiconductor channels (Fig. 14). Both *p*- and *n*-channel (100) GaAs MOSFETs have shown drive current enhancements under compressive and tensile uniaxial strain, respectively (Fig. 15) [43]. Electron mobility enhancements in $In_{0.7}Ga_{0.3}As$ channel HEMTs by the application of <110> uniaxial tensile strain have been reported (Fig. 16a) [42]. The drain current in the linear regime is mapped as a function of strain applied both

along the channel ($\varepsilon_{\parallel}$) and perpendicular to the channel ($\varepsilon_{\perp}$). Simulations have also shown that an unstrained-InAs channel has the capability of exceeding the effective mass reduction factor and produce higher drive currents than Si. Although the reduction in effective mass increases the electron mobility with uniaxial tensile strain, the gate capacitance (C_G) can also be lowered as it is mainly controlled by the quantum capacitance (C_q), which is directly proportional to the effective mass (m_e^*). This will eventually lead to lower drive currents as the gate capacitance is proportional to the density of states (DOS) and inversion layer concentration. However, it is important to note that C_q depends on m_{DOS}^* and this does not go considerable change under uniaxial strain. The density of states effective mass (m_{DOS}^*) is the square root of the product of $m_{\parallel}^*$ (in-plane effective mass, or "transport mass") and $m_{\perp}^*$(out-of-plane effective mass, or "confinement mass").

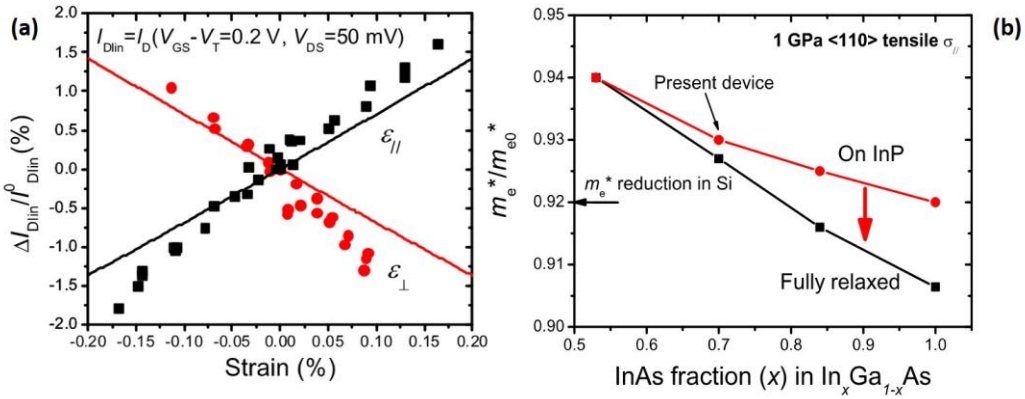

Fig. 16 (a) Relative change in drain current under the linear regime for uniaxial strain on the $In_{0.7}Ga_{0.3}As$ channel in the <110> direction. Points represent experimental data and lines represent ***k.p*** simulations (b) Effective mass reduction factors obtained from ***k.p*** simulations for $In_xGa_{1-x}As$ as a function of x. Incorporation of high InAs composition and relief of the lattice mismatch strain enlarge the m_e^* reduction factor, thereby increasing mobility and drive current.

The ideal scenario would be to decrease the transport effective mass for high injection velocity and increase the confinement mass to increase C_q and therefore, the DOS and drive current of the transistors using uniaxial strain. Additional studies have also been reported for *n*-$In_{0.2}Ga_{0.8}As$ on Si to show mobility enhancement under uniaxial strain by

measuring the piezoresistance coefficients using TLM measurements [44]. Another novel technique for the application of mechanical strain involves bonding the semiconductor chip to a $PbZrTiO_3$ (PZT) piezoactuator using epoxy. The application of a voltage bias induces a mechanical motion in the PZT piezostack that creates tensile or compressive strain on the substrate [5]. This technique has been used to tune the properties of a 2DEG in an AlAs quantum well with $Al_xGa_{1-x}As$ barriers and study the energy-level splitting and valley-repopulation under the applied strain.

1.4 Dissertation Overview and Research Objectives

The aim of this work is to show the potential for the monolithic integration of III-V heterostructures on Si substrates and demonstrate device applications for these virtual substrates, as well as the idea of using strain as a performance booster for III-V field-effect transistors.

In chapter 2, the basics of the heterointegration approach of GaAs using an STO buffer layer and GaSb using an AlSb buffer layer will be discussed in detail. The successful growth of GaAs and GaSb using appropriate buffer layers and solid-source molecular beam epitaxy will be explained in great detail. Then, the crystalline film quality and surface morphology for GaAs and GaSb on Si will be assessed using RHEED, XRD, and AFM. The effect of STO surface termination on the subsequent growth of GaAs and GaSb will be discussed and the impact of V/III flux ratio on the film properties will be presented.

In chapter 3, the integration of broken-gap Esaki tunnel diodes on Si using the buffer layer techniques developed in the previous chapter will be presented. First, a detailed description of the Tunnel-FET and Esaki diode working principle will be presented, along with the basics of conductance slope analysis. Then, the experimental details for the MBE

growth of InAs/GaSb p^+-i-n^+ structures on native and Si-virtual substrates will be presented. This will be followed by the fabrication of Esaki TDs and a detailed analysis of the film crystalline quality using XRD and surface morphology using AFM, as well as interface analysis using high-resolution X-TEM. Finally, a comparison of the electrical properties for all different platforms will be presented and the potential for use in TFET applications in terms of peak current density and conductance slope.

In chapter 4, a detailed description of the physics of strain in semiconductors will be presented followed by the experimental design of the InAs high-electron mobility (HEMT) structures, the design and fabrication of Hall bars, and the details of the strain and Hall setups. The following section will include details of strain calibration curves, and the effect of uniaxial tensile strain on sheet resistance, carrier mobility, and sheet carrier density on the <110> InAs channel. The results of electron mobility enhancement and channel carrier concentration will be presented to show the improved performance of III-V *n*-FETs under uniaxial stress.

In chapter 5, all the contributions of this dissertation will be summarized and all the accomplishments will be enlisted. Further suggestions for future research and investigations will also be made.

CHAPTER 2

Heterointegration of III-V Semiconductors on Si using Molecular Beam Epitaxy

2.1 Introduction

The cost effectiveness of silicon combined with the extremely mature processing technology has made silicon one of the most important materials of the 21st century. Even with its cadre of undeniable advantages, the silicon technology still suffers from low optical efficiency and has degraded electrical properties in scaled CMOS devices [45]. On the other hand, III–V semiconductors are ideal candidates for optoelectronic and photonic applications and because of their high carrier mobilities, they are being considered for the channel material in future Si based MOSFETs [1]. However, such implementation would require the monolithic integration of various III–V materials on silicon with low enough defects to fabricate surface channel MOS devices. The integration of III–V compound semiconductors with Si can also combine the cost advantage and maturity of the Si technology with the superior performance of III–V materials resulting in highly integrated semiconductor circuits.

GaSb in particular, is an important III-V compound with applications in MWIR and LWIR detectors [46, 47], high frequency operation in HEMTs [48, 49], improved efficiency in tandem solar cells [50], and thermo-photovoltaics cells [51]. The native GaSb substrates suffer from many issues including lack of semi-insulting option [52], optical losses [53], large wafer sizes and overall wafer quality. GaAs is a well-established technology with applications in the wireless and telecommunication industry, photonics, optoelectronics, and photovoltaics, but suffers from the same drawbacks as other III- V

substrates [54-56]. Therefore, the integration of GaSb and GaAs on Si substrates is highly desirable.

The heterointegration of III-Vs on Si in general presents several challenges including the growth of polar on non-polar substrate, large-lattice mismatch and large differences in the coefficients of thermal expansion thermal coefficient mismatch leading to the formation of anti-phase domain (APD) boundaries, dislocations and surface defects [57, 58]. Various schemes have been used to reduce the density of threading dislocations which including low temperature buffers, superlattice buffers [59], metamorphic buffers and thermal cycling [60, 61]. These methods usually require long growth periods and are inefficient in filtering out the dislocations leading to current leakage paths and non-radiative recombination centers.

In this chapter, high quality epitaxial growth of GaAs and GaSb will be demonstrated on Si substrates using solid-source molecular beam epitaxy and the concept of interfacial misfit dislocation arrays. Section 2.2 describes the integration concept behind the use of $SrTiO_3$ (STO) as a crystalline oxide buffer layer for the growth of GaSb and GaAs, as well as the use of AlSb as a popular buffer layer for GaSb epitaxial growth on Si. Section 2.3 details the experimental procedure for the growth and characterization of the different GaAs and GaSb thin films prepared on various silicon substrates. Section 2.4 presents the results and data analysis for the III-V film quality in terms in crystallinity, surface morphology and *in-situ* surface reconstructions during MBE growth. Section 2.5 summarizes the findings from this work.

2.2 Lattice-Mismatched Epitaxy Using Intermediate Buffer Layers

2.2.1 Heterointegration of GaSb on Si (100) using an AlSb buffer layer

A well-established approach to realize high quality, strain-relaxed GaSb on Si (001) wafers is the interfacial misfit (IMF) dislocation array technique through the use of AlSb as a buffer layer [25]. Using the IMF technique, highly 2D periodic arrays of pure-edge 90^o dislocations (Fig. 17) are formed in the [110] and [-110] direction on the Si (001) surface which relieves the strain immediately at the interface [27]. After forming the IMF array on the silicon surface using the AlSb nucleation layer, subsequent growth of GaSb can be carried out resulting in very low defect density layers [62]. Matthew's theory of lattice-mismatched growth using tetragonal distortion states, that the excess strain is relieved by forming misfit dislocations when a certain critical thickness is reached [63]. The critical thickness is a result of the competition between the chemical energy and strain energy during growth. However, the pure-edge misfit dislocations do not follow the tetragonal distortion method and the IMF array technique makes use of the atomic arrangement of atoms on the substrate surface to relieve the strain before reaching the critical thickness. Since most of the strain energy is relieved at the substrate-epilayer interface by misfit dislocations that propagate parallel to the interface instead of threading vertically into the active layers. The 90^o pure-edge misfit dislocations do not introduce any threading segments as they are elastically stable and cannot glide on the {111} planes, in contrast to 60^o dislocations that can easily glide along the {111} planes resulting in threading dislocations [64] .

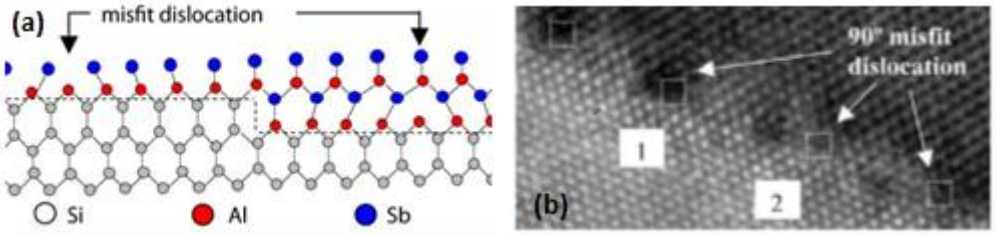

Fig. 17 (a) "Ball and stick" model of the atomic arrangement at the Si-AlSb interface showing that the Sb atom skips every 9th Si atom to form the periodic misfit dislocation array. (b) High-resolution cross-sectional TEM image for the AlSb IMF array formed on the Si (001) substrate in both [110] and [-110] directions consisting of pure 90° edge dislocations. [27]

In addition to strain relief at the AlSb-Si interface using the IMF array technique, high quality growth of GaSb on Si requires the suppression of anti-phase domain boundaries (APDs) that originate as a result of polar on non-polar growth. Successful elimination of APDs has been demonstrated for the growth of AlSb on Si using miscut substrates, which use the atomic-step height for APD annihilation [27]. As shown in Fig. 1a, the interface consists of Al-Si bonds, while Sb atoms skip every 9th Si atom in the substrate. These misfit dislocations are arranged in a highly 2-D periodic array at the AlSb-Si interface correspond to 8 AlSb lattice sites and 9 Si lattice sites in the <110> direction, which equates to approximately 3.46 nm. Once the large lattice-mismatch of 13% between Si and AlSb is relieved effectively using the IMF array technique, the GaSb film can be grown on the AlSb buffer layer which is a much lower mismatch of ~ 0.7%. In this chapter, the AlSb buffer layer approach is investigated for different substrate temperatures on both on-axis and miscut Si substrates to achieve highly crystalline and smooth GaSb films.

2.2.2 Heterointegration of GaAs on Si (100) using an $SrTiO_3$ buffer layer

A novel integration scheme that has been used for GaAs on Si includes a crystalline oxide buffer layer, viz. $SrTiO_3$ (STO) that was grown epitaxially on Si [19]. The $SrTiO_3$ lattice (a_{STO} = 3.905 Å) undergoes a 45° rotation to accommodate the high lattice mismatch

with the underlying Si (001) (a_{Si} = 5.431 Å) leading to a strain of 1.7%. The GaAs lattice (a_{GaAs} = 5.653 Å) grown is now strained 2.4% with respect to the 45^o rotated $SrTiO_3$ lattice, thereby enabling the reduction from the original 4% strain for the GaAs/Si system. The crystallographic orientation of STO with respect to Si and GaAs is that Si(001)||STO(001)||GaAs(001) and Si[110]||STO[100]||GaAs[110] as shown in Fig. 18a. Even though there is a large lattice mismatch between the Si/GaAs and STO lattice structures, the in-plane 45^o rotation of the STO buffer layer enables the reduction in lattice mismatch and interface dislocations by minimizing the in-built strain energy (Fig. 18b).

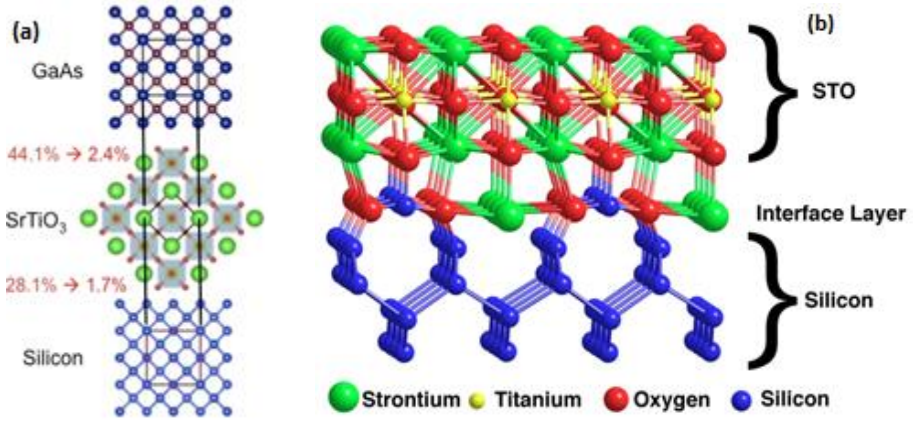

Fig. 18 (a) Top-view schematic of the Si/STO/GaAs system with the crystallographic orientation Si(001)||STO(001)||GaAs(001) and Si[110]||STO[100]||GaAs[110]. (b) "Ball and stick" model of the atomic arrangement at the STO and Si interface in the [110] direction.

A two-step growth process utilizing a high temperature nucleation layer of GaAs, followed by a low-temperature GaAs layer at a higher growth rate was employed for this work. The surface termination conditions of the $SrTiO_3$ crystalline buffer layer have a strong effect on both the crystalline and surface quality of the final GaAs epitaxial growth. The ideal growth mode for high quality epitaxial films is the Frank-van der Merwe growth mode (2D growth mode) where the growth occurs one monolayer at a time as the adatoms move preferentially to the surface sites. To accomplish 2D layer-by-layer growth of GaAs

on the STO/Si substrate, the GaAs needs to properly wet the STO. This requires that the surface energy of the STO surface should be greater than the sum of the GaAs surface energy and the interface energy. The $SrTiO_3$ surface energy can be modified with the kind of atom used to terminate the surface with three possible options: Sr-termination, Ti-termination, and stoichiometric-termination. Prior work by Largeau *et al.* has shown the growth of GaAs islands on TiO_2 terminated STO films with the coexistence of wurtzite and cubic phases [22]. This study investigates the effect of the $SrTiO_3$ surface terminations on the subsequent GaAs surface and epilayer quality.

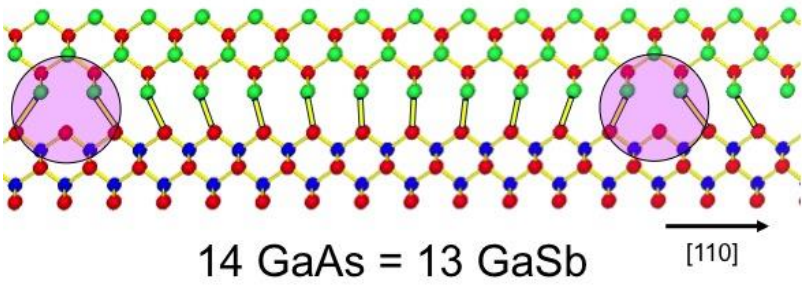

Fig. 19 "Ball and stick" model of the atomic arrangement at the GaAs-GaSb interface showing the presence of periodic misfit dislocations which corresponds to 14 GaAs lattice sites and 13 GaSb lattice sites in the [110] direction.

High quality GaSb can be achieved on GaAs using the above-mentioned IMF array growth technique. Similar to the AlSb/Si IMF array technique, the 8% lattice mismatch at the GaAs/GaSb heterointerface can be relieved in a similar manner by forming a 2-D network of 90^o pure-edge misfit dislocations [28]. The Sb atoms in this case self-assemble on the GaAs surface, forming bonds with the Ga atoms. The Ga-Sb bond bends and stretches in order to accommodate the lattice mismatch and one Sb-Ga bond is skipped every 13 atomic sites. This periodic misfit-dislocation array helps relieve the large mismatch at the interface in the form of pure-edge type dislocations where 14 GaAs lattice

sites correspond to 13 GaSb lattice sites along the [110] direction and a misfit spacing of ~ 5.6 nm (Fig. 19).

The GaAs/STO/Si platform can be used as a virtual substrate for investigating the growth of GaSb layers on Si using the IMF-based growth on the GaAs epilayer. The monolithic integration of GaSb on these Si-based virtual substrates will open up doors for high frequency, low-power tunnel- FETs and Esaki diodes which will be discussed in detail in Chapter 3. In this study we report on the effects of the oxide surface termination on the nucleation and subsequent growth of GaAs, and the use of GaAs/STO/Si as virtual substrates for the growth of GaSb heterostructures and compare this to the use of the AlSb buffer layer on Si.

2.3 Experimental Procedure

2.3.1 Growth of GaSb epitaxial layers using AlSb as a buffer layer

Initially, 3" *p*-Si (001) substrates with on-axis orientation were treated in a UV ozone system to form a thick oxide layer. The wafers were then treated in a 1:4 solution of HF acid in DI water for 2 minutes to dissolve the oxide completely, leaving a hydrogen-terminated Si (001) surface. At this point, the wafers were introduced immediately into the load lock section where they were baked at 150 ^{o}C for 1 hour. After the preliminary baking to remove water vapor and other surface contaminants, the H-terminated silicon substrates were introduced into a DCA R450 MBE III-V growth chamber. The manipulator temperature was then increased to approximately 550 ^{o}C until the RHEED pattern changed from a spotty to (2 × 2) reconstruction indicating the desorption of the hydrogen atoms from the Si (001) surface. After 10 minutes of desorption, the surface was exposed to Al atoms for 25 seconds, and then the Sb shutter was opened to allow the formation of AlSb

islands. The initial Al soak enables the Al-Si bond formation and the Sb soak leads to the formation of the IMF array in the form of island growth. Continued growth of AlSb leads to (1 × 3) reconstruction indicating layer-by-layer growth and a transition from rough islands to a smoother thin film surface. After growing a 250 nm buffer layer of AlSb at a growth rate of 0.4 ML/s and Sb_2 flux of 2×10^{-6} Torr beam equivalent pressure (BEP), a 250 nm layer of GaSb was grown on top for different substrate temperatures to see the effect on the layer crystallinity and surface roughness. The GaSb layers were grown at 0.3 ML/s for the same Sb_2 flux as before.

For the growth of GaSb on the 4^o miscut wafers with an AlSb buffer layer, similar growth conditions were used as mentioned above with both AlSb and GaSb growth rates set to 0.15 ML/s, Sb_2/Al ratio of 12 and Sb_2/Ga ratio of 7. Atomic surface diffusion length is given by $\lambda = \sqrt{2D\tau}$, where D is the surface diffusion coefficient and τ is the mean residence time of adatoms. In usual MBE growth conditions, τ for group III elements can be taken as the inverse of the growth rate. When the growth rate is low, the surface diffusion length of Ga atoms is long and the Ga atoms have enough time to move to the minimum free energy position, at the defects introduced by the highly strain between the AlSb and Si on the surface. For the growths of GaSb on these miscut wafers, a fixed substrate temperature of 500 ^{o}C was used based on previously published literature. The surface morphology of the grown samples was mapped using atomic force microscopy (AFM) the structural properties of the films were analyzed *ex-situ* using X-ray diffraction.

2.3.2 Growth of GaAs and GaSb epitaxial layers using $SrTiO_3$ as a buffer layer

The heterointegration approach was developed by growing GaAs films on Si wafers using a crystalline $SrTiO_3$ buffer layer resulting in templates of GaAs virtual substrates

with a potential to grow complex III–V structures on a Si wafer. Growing GaSb epilayers onto these GaAs templates extended the concept of this integration. Initially, 3" *p*-Si (001) wafers (on-axis and 4^{o} miscut towards <110>) were treated in a UV-ozone system to aid in the complete removal of carbon contaminants and then loaded into a load-lock section for an initial baking at 150 ^{o}C for 30 minutes. This step is critical in the elimination of carbon containing species on the Si surface that can lead to surface hillocks and non- ideal nucleation of the oxide if not eliminated. The wafers were then introduced into an oxide MBE chamber equipped with Sr and Ti effusion cells and a molecular oxygen source where 10 nm of $SrTiO_3$ with different surface terminations was grown on Si. Prior to the STO buffer layer growth, the Si wafers were cleaned using the de-oxidation procedure as developed by Wei *et al* [20]. The removal process of the native oxide involves depositing 1–2 monolayers of Sr metal on the surface at temperatures between 400 ^{o}C – 600 ^{o}C followed by a temperature anneal step greater than 750 ^{o}C. The resulting surface is a well-ordered clean (2 × 1) reconstructed Si surface. The entire growth process was monitored using *in-situ* reflection high electron energy diffraction (RHEED) to determine the growth mode and surface stoichiometry.

STO growth was performed in two steps: first a nucleation layer of 2 unit cells was grown on the Si wafer at low temperature (300 ^{o}C) by co-depositing Sr and Ti under molecular O_2 environment at a partial pressure of 6 × 10^{-8} Torr followed by a high temperature (550 ^{o}C) anneal and subsequent growth of STO using an O_2 partial pressure of 10^{-7} - 10^{-6} Torr. Typical growth rate used for the crystalline oxide film was 1 unit cell/min as determined by RHEED oscillations. Three different surface conditions of the STO film were chosen for this study: stoichiometric, Ti-terminated, and Sr-terminated. By default,

the STO growth was performed under a stoichiometric regime (as evidence by a RHEED (1 × 1) reconstruction) that can be switched to either a Ti-rich or Sr-rich surface by closing the shutter for the respective metal cell and keeping the other one open until specific termination is achieved. The surface termination was monitored by RHEED as detailed in [19]. Following the growth of crystalline STO on Si, all the wafers were unloaded from the MBE cluster tool and stored under ambient conditions. Quarters of STO/Si wafers were then cut and loaded into a III–V MBE chamber for As-based semiconductor growths. Two sets of samples consisting of 0.5 μm and 1.5 μm GaAs were grown on the different STO/Si terminations to show the effect of the STO surface conditions on GaAs epilayer growth. The STO/Si samples were degassed at 580 ^{o}C for 15 min; then, a GaAs nucleation layer of 25 nm was grown at a temperature of 450 ^{o}C using an As_2/Ga ratio of 8 and a growth rate of 0.15 ML/s. Following this, the growth temperature was decreased to 380 ^{o}C and 475 nm or 1475 nm of GaAs layer was deposited at an As_2/Ga ratio of 15 and growth rate of 0.5 ML/s. Finally, a post-growth anneal was carried out at 580 ^{o}C for 15 min with the entire growth process being monitored using *in-situ* RHEED.

The GaAs/$SrTiO_3$/Si virtual substrates with the best crystalline quality and surface morphologies were then introduced in a different III–V MBE chamber with As and Sb valved crackers present. Here an additional buffer layer of 0.5 μm GaAs was grown at 580 ^{o}C with a growth rate of 0.5 ML/s. Growth rate calibrations were performed previously on a GaAs substrate using RHEED intensity oscillations. Following this, a 0.5 μm layer of GaSb was grown on GaAs at 510 ^{o}C using the interfacial misfit (IMF) dislocation array technique as described by Huang et al. [15]. Heteroepitaxial GaSb films of extremely low dislocation density can be achieved using this technique. In this work, the GaSb surface

quality and crystalline quality was monitored as a function of the V/III flux ratios using the IMF array technique. The surface morphology of the grown samples was mapped using atomic force microscopy (AFM) in tapping mode with a Si probe tip and the structural properties of the films were analyzed *ex-situ* using a double crystal X-ray diffractometer. The interface analysis was also performed using high-resolution cross-sectional transmission electron microscopy.

2.4 Results & Discussion

2.4.1 Hetero-epitaxy of GaSb on Si using an AlSb buffer layer

After the removal of the hydrogen to form a clean Si (001) surface, the initial Al soak enables the Al-Si bond formation and the Sb soak leads to the formation of the IMF array in the form of island growth. Initial RHEED pattern consists of an interconnected spotty features with a superimposed (1 × 3) reconstruction (Fig. 20a). This is significant of AlSb SK growth with {111} facets and the AlSb (100) plane on the top. Continued growth of AlSb leads to (1 × 3) RHEED pattern indicating layer-by-layer growth and a transition from islands to a planar 2D growth mode (Fig. 20b). The subsequent GaSb epilayer growth also occurs under a FM growth mode as shown by the streaky (1 × 3) RHEED pattern in Fig. 20c.

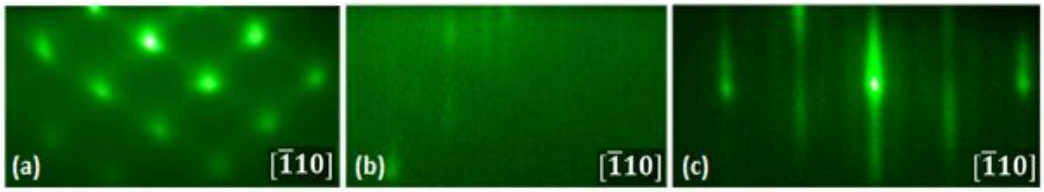

Fig. 20 (a) Interconnected spotty RHEED pattern indicating the growth of AlSb island in the 3D growth mode via IMF array (b) RHEED pattern at the end of the AlSb buffer layer showing a (1 × 3) reconstruction indicating a planar growth mode (c) RHEED pattern of the subsequent GaSb layer also showing a (1 × 3) reconstruction indicating 2D growth.

The crystalline quality of the epilayers grown was assessed using XRD measurements. First, a 2θ-ω XRD scan was performed to find out the peak positions of the (002) and (004) planes for both AlSb and GaSb as shown in Fig. 21 below. The measured values correspond very well with the expected theoretical values calculated using Bragg's law for diffraction as shown in Table 1.

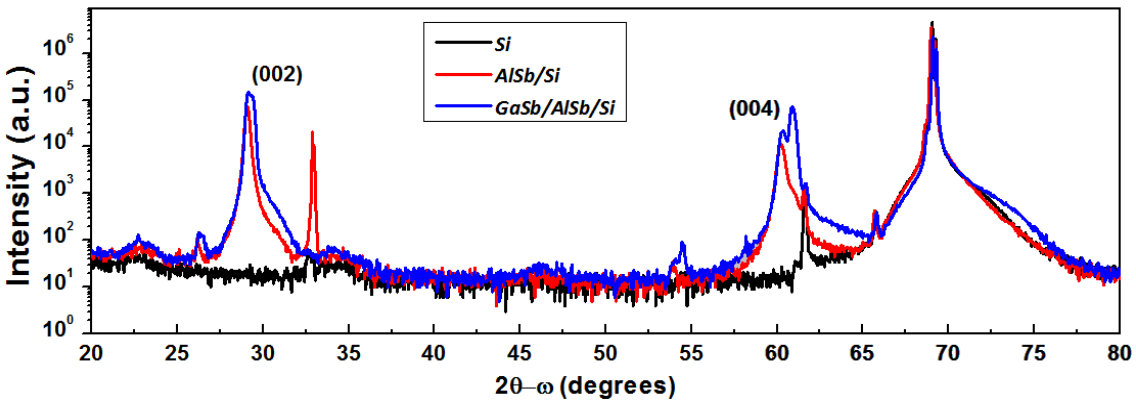

Fig. 21 2θ-ω scan comparing the different peak positions for a native Si (001) substrate, Si (001) with AlSb layer, and Si (001) with AlSb buffer layer and GaSb film on top.

After finding the exact 2θ positions for the (002) planes for both AlSb and GaSb, double-crystal XRD scans ω-2θ were measured for the different samples to extract the FWHM along with tapping mode AFM measurements to assess the RMS surface roughness for a 10 μm × 10 μm square area. The lowest FWHM of 135 arcsecs for the GaSb (002) peak was measured for the growth temperature of 545 ^{o}C and the lowest RMS roughness of 5.1 nm was measured for substrate temperature of 525 ^{o}C (Fig. 22). These samples however showed the presence of anti-phase domain boundaries (APDs) on the surface after AFM measurements, which is expected for on-axis substrates (Fig. 23a).

Table 1 Comparison of the theoretical and measured 2θ values for (002) and (004) lattice planes of GaSb and AlSb using Bragg's law.

Crystal Plane	*d (Å)*	2θ (*theoretical*)	2θ (*measured*)
GaSb (004)	1.5225	60.7864°	60.8950°
AlSb (004)	1.5339	60.2886°	60.2183°
GaSb (002)	3.0450	29.3062°	29.3894°
AlSb (002)	3.0678	29.0840°	29.0867°

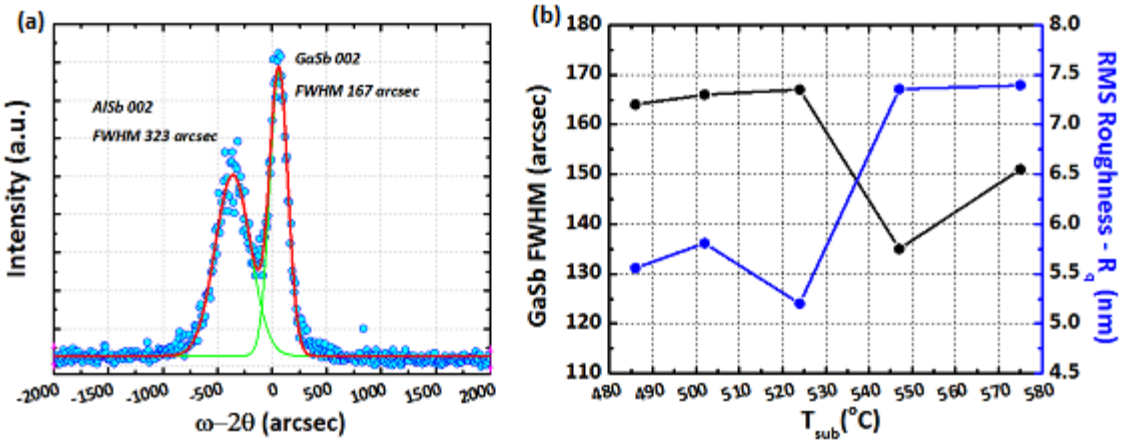

Fig. 22 (a) Double-crystal XRD rocking curve for the (002) peaks of AlSb and GaSb grown on Si (001) for a growth temperature 525 °C. Peak fitting was performed using a Gaussian distribution to extract the FWHM values. (b) FWHM for the GaSb (002) peaks and the RMS surface roughness as a function of the growth temperature.

To address the problem of APDs arising from the polar on non-polar growth, we utilized 3" Si (001) substrates with a 4° miscut in the <110> direction. The wafer miscut helps in the suppression of APDs by utilizing the double step-edge and realigning the III-V lattice sites in the right stacking formation for the growth of AlSb on Si, which is evident by the absence of domains on the surface as measured by AFM in Fig. 23b. For the growth of GaSb on the 4° miscut wafers with an AlSb buffer layer, similar growth conditions were used as mentioned above with both AlSb and GaSb growth rates set to 0.15 ML/s, Sb_2/Al ratio of 12 and Sb_2/Ga ratio of 7 and a substrate temperature of 500 °C. For these growth conditions, the RMS surface roughness obtained was 6.1 nm and a GaSb (002) peak

FWHM of 120 arcsecs.

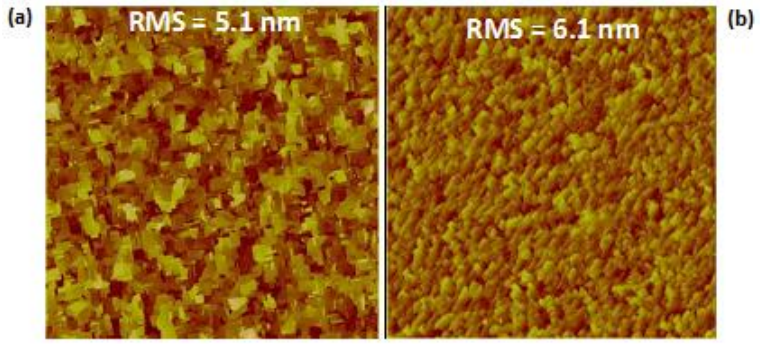

Fig. 23 (a) 10 μm × 10 μm AFM scan of the GaSb surface grown on a no-miscut Si (001) wafer showing the presence of APDs on the surface. (b) GaSb surface on a 4° miscut Si (001) towards [110] direction showing no APDs but increase in overall RMS roughness.

Due to the significant difference in the coefficients of thermal expansion of Si, AlSb, and GaSb, the cool down rate after the end of the growth can play a significant role in the final surface quality of the sample. To study this, the same growth parameters were used as mentioned above for 4° miscut Si (001) substrates with different cool down rates of the manipulator temperature. Table 2 shows that a cool down rate of 15 °C/min provides the lowest value of surface roughness for the GaSb surface. Although the RMS surface roughnesses are much lower than the initial 12-13 nm that were seen on miscut substrates under high growth rates for both the AlSb and GaSb layers, these are still on the higher side of the acceptable values for device fabrication involving active layers on the order of a couple of nanometers. However, for lattice-mismatched growth on a silicon substrate, these conditions can be used to at least demonstrate successful device performance as a starting point. Numerous other methods including strained layer superlattice (SLS) consisting of AlSb and GaSb, graded buffer layer for $AlAs_xSb_{1-x}$, and post growth high temperature anneal were also explored but failed to improve the surface roughness of the top GaSb layer.

Table 2 Effect of cool down rate of the manipulator on the final surface roughness due to the mismatch in thermal coefficient of expansion.

Cool Down Rate	*RMS roughness*
50 °C/min	8.7
30 °C/min	7.1
15 °C/min	6.1

2.4.2 Hetero-epitaxy of GaAs on Si using a $SrTiO_3$ buffer layer

The crystallographic orientation of STO with respect to Si is that Si (001)||STO(001)||GaAs(001) and Si[110]||STO[100]||GaAs[110]. This is made possible as the $SrTiO_3$ lattice (a_{STO} = 3.905 Å) undergoes a 45° rotation to accommodate the high lattice mismatch with the underlying Si (001) (a_{Si} = 5.431 Å) leading to a mismatch of 1.7%. This results in a critical thickness of 7.6 nm according the Mathews-Blakeslee model based on tetragonal distortion. Experimentally, the critical thickness was found to be around 4nm which is a much lower value compared to the model estimation [65]. Fig. 24 displays a typical 10 μm × 10 μm AFM image of 10 nm STO layer grown on both nominal and vicinal 4° miscut Si (001) wafers. The STO undergoes relaxation as it is grown well above the critical thickness on the Si substrate.

However, the misfit dislocations accommodate the lattice mismatch between the rotated STO lattice and the underlying Si leading to a surface morphology that exhibits a very flat surface with a root mean square (RMS) roughness of around ½ a_{STO} for both the wafers. The surface quality is also corroborated *in-situ* by the streaky and sharp RHEED patterns displayed in the inset of Fig. 24a, and Fig. 24b. The different surface terminations of STO exhibit similar features in AFM micrographs and RHEED patterns. These results

guarantee that the epitaxy of III-V films on STO/Si template is performed on extremely smooth surfaces.

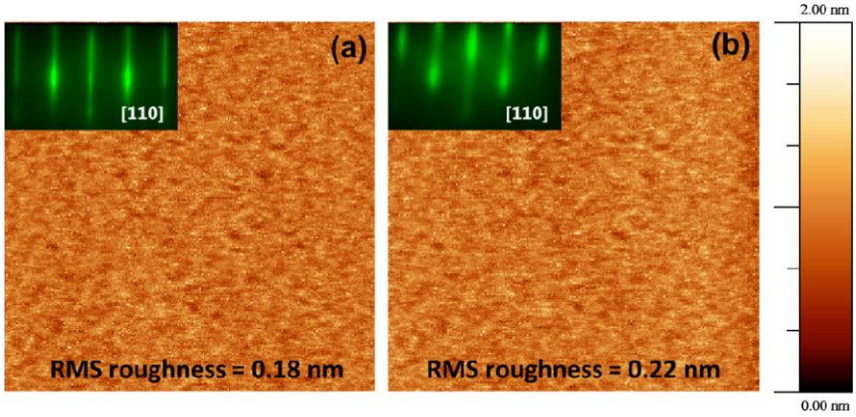

Fig. 24 AFM micrographs of 10 nm STO films grown on (a) nominal Si (001) substrate and (b) vicinal 4° miscut Si (001) towards [110] showing extremely low values of RMS roughness. Inset: RHEED patterns along the [110] direction for each case.

III-V growth was started with a 25 nm of GaAs nucleation layer. Diffraction patterns at the end of the nucleation layer along [$\bar{1}$10] azimuth are shown for the Ti- and Sr-terminated STO films in Fig. 25. Both RHEED patterns are spotty indicating 3 dimensional growth of the nucleation layer with the formation of islands. The RHEED pattern of the GaAs nucleation layer grown on the Ti-terminated STO surface is spotty with ring-like features suggesting a polycrystalline nature of this layer, i.e. crystal grains with several orientations where, possibly, cubic and hexagonal phases could coexist (Fig. 25a). On the other hand, the nucleation on the Sr-terminated surface shows a well-ordered spotty RHEED pattern where the diffraction spots arrangement and interconnection is indicative of cubic mono-crystalline faceted islands (Fig. 25b). Similar to this, the nucleation on stoichiometric STO exhibits the same behavior. From RHEED patterns, it is evident that the crystallographic relationship [110]GaAs||[100]STO||[110]Si exists confirming the 45° rotation of STO w.r.t to both the underlying Si and overlying GaAs epilayer. This relation is also confirmed by high-resolution TEM images shown in Fig. 26.

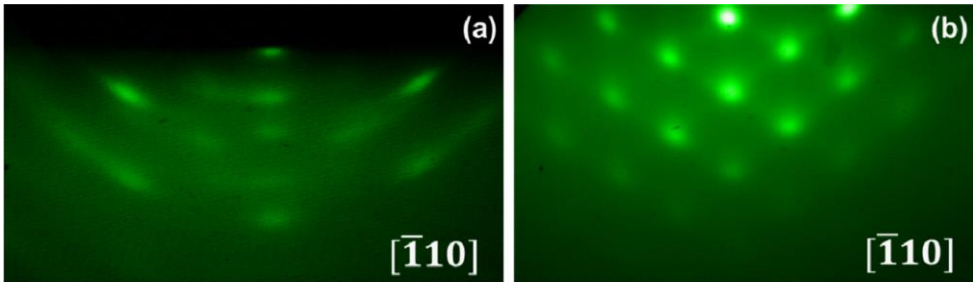

Fig. 25 RHEED patterns observed along the [$\bar{1}$10] direction during the GaAs nucleation layer growth on (a) Ti-terminated STO and (b) Sr-terminated STO.

GaAs films grown on STO show a strong dependency on the miscut of the Si substrate (nominal and miscut), the thickness of GaAs and the underlying termination of the STO as can be observed in AFM images of Fig. 27. In this figure, the topography of 1.5 μm thick GaAs film in a 10 μm × 10 μm AFM scan is shown as a function of these parameters.

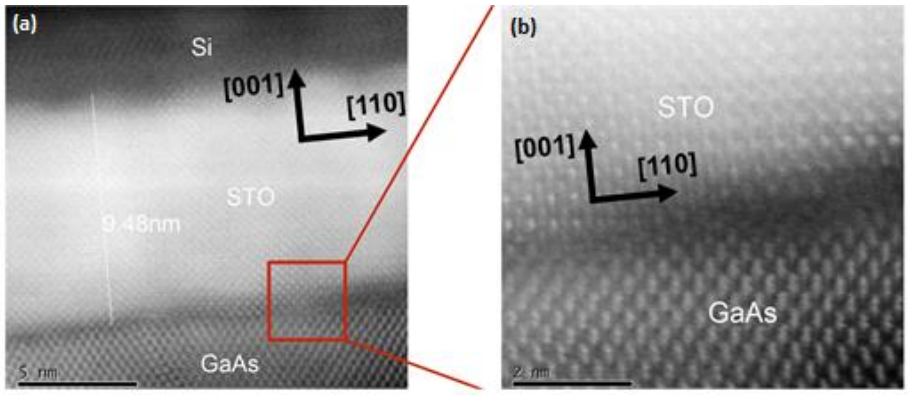

Fig. 26 High-resolution cross-sectional TEM images of the GaAs/STO and STO/Si interfaces showing the clear 45° rotation of the [100] perovskite $SrTiO_3$ crystal to align itself parallel to the [110] Si and GaAs lattices.

GaAs grown on on-axis STO/Si (001) presents a surface morphology consisting of clear antiphase domains that are isolated by well-defined boundaries (Fig. 27a) resulting, in general, from the hetero-epitaxy of polar semiconductors grown on a nonpolar surfaces as in this case where the GaAs is grown on STO(001)/Si surface with no miscut on the starting Si substrate.

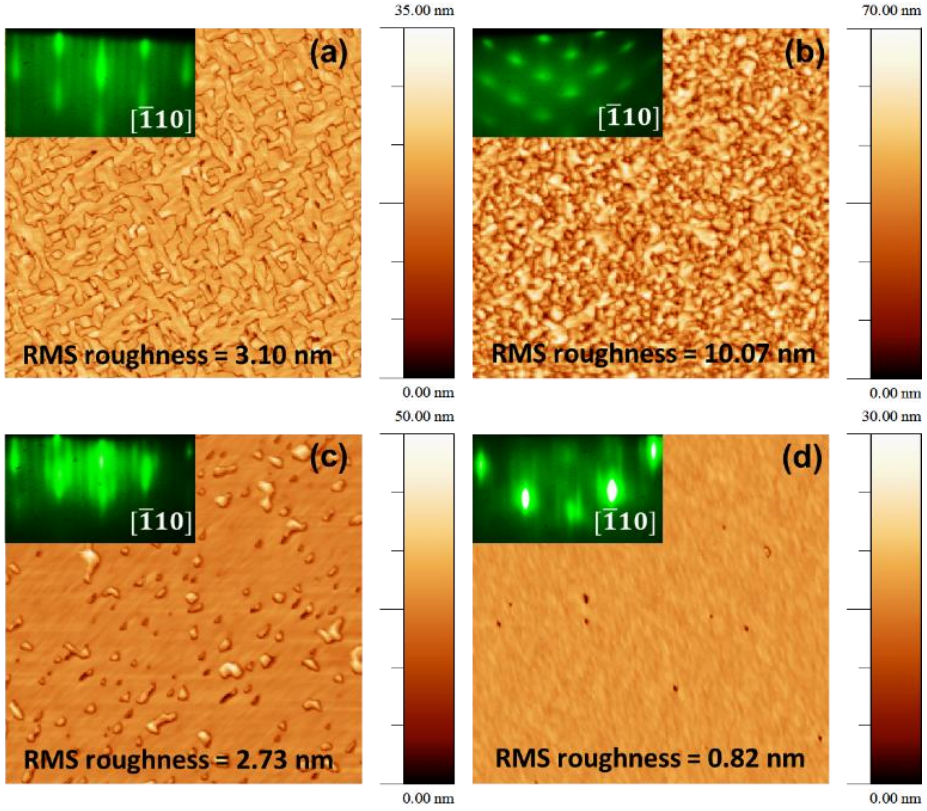

Fig. 27 AFM scans of 10 μm x 10 μm areas of the GaAs film surface on (a) nominal STO/Si (001) (b) Ti-terminated STO/miscut Si (001) (c) stoichiometric STO/miscut Si (001) (d) Sr-terminated STO/miscut Si (001). Inset: RHEED patterns along the [1̄10] direction for each case.

Although the RMS roughness is high in this sample (~3.1 nm), the individual domains exhibit very flat surfaces as is corroborated by the 4× streaky and slightly spotty RHEED pattern (inset of Fig. 27a). RHEED also confirms, in this sample, the 2-domain nature as seen in the AFM micrograph in which the 4× reconstruction from the (2 × 4) surface is present in the orthogonal [110] azimuths. The growth on 4^{o} miscut STO/Si templates promotes the growth of single domain GaAs as evidenced in AFM images (Fig. 27c and Fig. 27d), however, the growth is strongly dependent on the STO surface termination. GaAs grown on Ti-terminated STO surface depicts a grainy topography with a high RMS roughness of ~ 10 nm (Fig. 27b), this texture is in agreement with the spotty RHEED obtained at the end of the growth in inset of Fig. 27b. On the other hand, GaAs

layer grown on stoichiometric and Sr-terminated display flatter surfaces where anti-phase domains are absent.

Also, the RMS roughness has improved from 10 nm to as low as 2.7 nm and 0.8 nm for stoichiometric and Sr-rich surfaces, respectively. The stoichiometric termination shows a GaAs film mainly being flat but with small mound grains and holes that contributes to the roughness while GaAs on Sr-terminated STO surface is characterized by a very flat topography with just a few small holes and the lowest roughness a necessary requirement for device fabrication. The streaky RHEED patterns (insets Fig. 27c and Fig. 27d) are in correspondence with the observed surface features in both samples; (2 × 4) surface reconstruction is clearly seen at the growth temperature. In particular, the sample with the lowest roughness displays a RHEED pattern whose diffraction features are along a semicircle indicative of a very smooth surface.

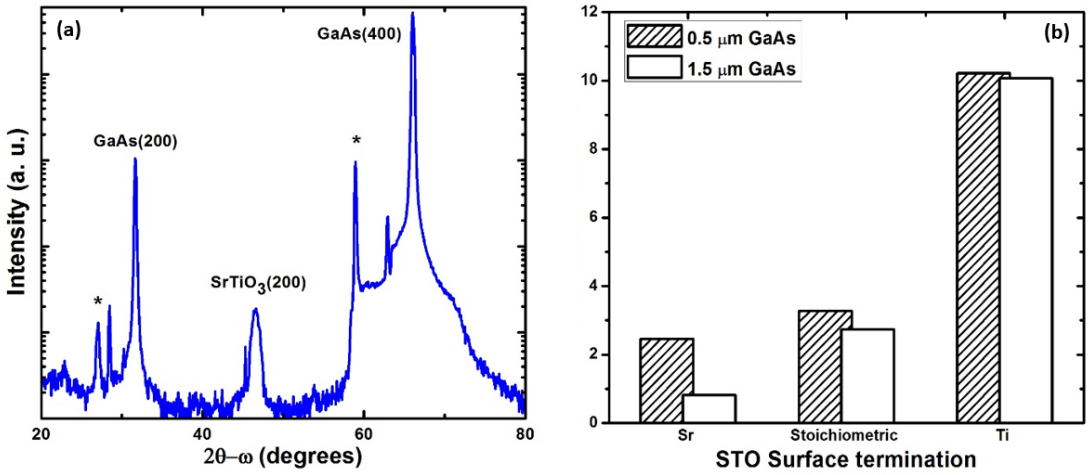

Fig. 28 (a) Coupled 2θ-ω XRD scan for GaAs grown on Sr-terminated STO/miscut Si (001) substrate. The symbol "*" represents the peaks arising from the Cu-k_β x-ray emission. The extra sharp peaks are related to instrument noise. (b) The effect of STO surface termination and the thickness of the GaAs epilayer on the final surface quality of the GaAs in terms of RMS roughness using AFM.

XRD analysis was performed for the sample with the optimum surface quality according to AFM. Diffraction peaks are clearly observed from relaxed (200) STO planes

and relaxed (200) and (400) GaAs lattice planes (Fig. 28a). The wafer miscut inhibits the detection of the Si (400) planes since the Bragg condition is no longer satisfied in this orientation of the substrate. We observe, that the best results for surface roughness (0.8 nm) are obtained for GaAs films grown on a Sr-terminated STO buffer layer for a 1.5 μm thick layer on Si (001) with a 4^o miscut in the [110] direction (Fig. 28b).

As mentioned before, the crystalline quality and surface morphology of the GaAs epilayer depends strongly on the surface energy of the STO film, which is governed by the surface termination. In order for GaAs to wet the STO surface properly leading eventually to a 2D growth mode, the surface energy of the STO surface should be greater than the sum of the GaAs surface energy and the interface energy. The surface energy of a Sr-terminated STO surface has been calculated to be 1433 erg/cm^2 according to Zhang *et al* [21]. The surface energy of different GaAs (100) reconstructions have also been calculated using *ab initio* density functional methods, and for $\beta(2 \times 4)$ reconstruction, this value is around 1000 erg/cm^2 according to Haugk *et al* [66]. Recent calculations by Demkov *et al* have shown that the interface energy for this system can be as low as 300 erg/cm^2, which means that the Sr-terminated STO provides enough energy to the surface to exceed the sum of the GaAs surface energy and the interface energy [67].

This leads to complete wetting of the GaAs layer and subsequent layer-by-layer growth responsible for high crystalline quality and optimum surface quality. As compared to the Ti-terminated STO, the surface energy is not enough to overcome this sum and leads to the formation of polycrystalline films, which do not exhibit the 2D growth mode and are much rougher than the Sr-terminated case.

2.4.3 High-quality GaSb on GaAs/STO/Si virtual substrates

For the integration of GaSb on Si needed for the development of high mobility transistors in next-generation CMOS applications, the GaAs/STO/Si virtual substrate platform was used. Here a buffer layer of GaAs was first grown onto the GaAs/STO/Si (001) virtual substrate with a 4^{o} miscut in the [110] direction leading to a clear (2 × 4) reconstruction at a substrate temperature of 580 ^{o}C. The surface was then Ga-stabilized leading to a (4 × 2) reconstruction by closing the As shutter. At this point, the introduction of Sb flux leads to a (2 × 8) reconstruction indicating atomic packing instead of tetragonal distortion, resulting in 90^{o} pure edge dislocations for the formation of the IMF dislocation array. The substrate was then cooled down to 510 ^{o}C while maintaining the (2 × 8) reconstruction, and the GaSb deposition was then resumed with the growth showing Stranski-Krastanov (SK) mode as observed in the RHEED patterns. Fig. 29a shows island growth after an initial thin layer of GaSb and as growth commences, the islands coalesce and the RHEED transforms into a clear (1 × 3) surface reconstruction depicting layer by layer growth as in Fig. 29b.

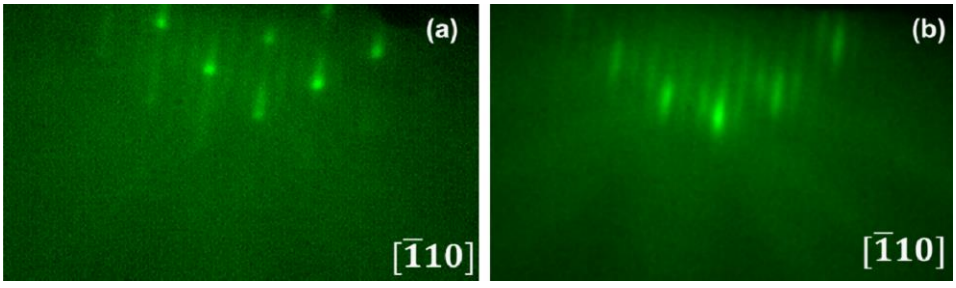

Fig. 29 RHEED patterns observed along the [$\bar{1}$10] direction during the GaSb growth on Ga-rich GaAs surface (a) initial stages showing GaSb islands and 2D growth and (b) (1 × 3) reconstruction after 50 nm GaSb showing two-dimensional growth.

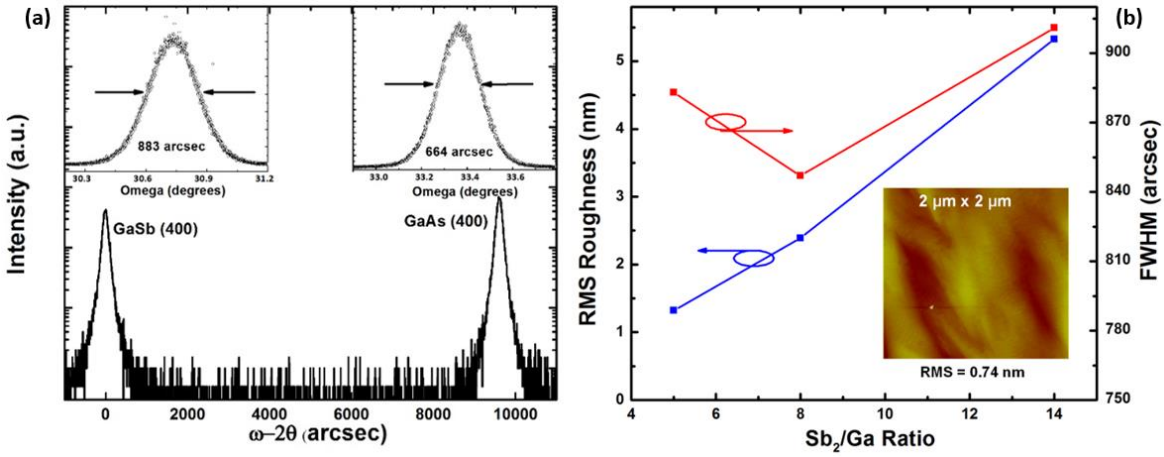

Fig. 30 (a) Triple-axis ω-2θ scan for GaAs (400) and GaSb (400) showing complete relaxation of the GaSb epilayer and narrow FWHM for both peaks indicating high crystalline quality layers. Inset: Rocking curves for GaSb and GaAs (400) peaks. (b) RMS surface roughness of 10 μm × 10 μm areas and GaSb (400) rocking curve FWHM mapped as a function of Sb_2/Ga flux ratio. Inset: AFM micrograph of a 2 μm × 2 μm area showing extremely smooth surface quality for a flux ratio of 5.

Fig. 30a shows the triple-axis ω-2θ scan for the GaAs (400) and GaSb (400) peaks which reveals a completely relaxed GaSb layer with respect to the underlying GaAs. The inset for this figure shows the respective omega rocking curves for GaSb and GaAs with FWHM values of 883 arcsecs and 664 arcsecs respectively indicating high crystalline quality with low density of dislocations in these films. To optimize the parameters for high quality growth of GaSb on the silicon-based virtual substrates, different V/III flux ratios were used; this was determined by measuring the beam equivalent pressures (BEP) using an ion gauge. Fig. 30b summarizes the rocking curve FWHM of the GaSb (400) peaks as a function of Sb_2/Ga flux ratio. AFM scans were also performed for all the samples to determine the growth parameters needed to produce the lowest RMS roughness, also shown in Fig. 30b. The data shows that the minimum surface roughness was obtained for a V/III flux ratio of 5 and the minimum FWHM was obtained for a flux ratio of 8, suggesting that a growth window exists for optimal surface and epilayer quality.

2.5 Chapter Summary

In this chapter, we have successfully demonstrated high quality growth of GaAs on $SrTiO_3$/Si substrates and GaSb on AlSb/Si using solid-source MBE. The crystalline and surface qualities of the GaAs films were monitored as a function of the surface termination of the STO layer. The Sr- terminated STO surface has sufficient surface energy to allow for complete wetting and 2D growth of the GaAs film and produces the best surface morphologies. Using the GaAs/STO/Si wafers as virtual substrates, GaSb films were grown on the Ga-rich GaAs surface via the IMF array technique. The growth of GaSb was optimized to achieve films with high crystalline quality and extremely low RMS surface roughness. This study shows that the GaAs/STO/Si integration approach is superior to the AlSb buffer layer approach in terms of surface and crystalline quality of the GaSb films [68]. Successful monolithic integration of GaAs and GaSb on Si can lead to future III-V low cost CMOS devices as well as multifunctional devices on a single Si chip.

CHAPTER 3

Growth and Fabrication of Broken-gap Heterojunction InAs/GaSb Esaki Tunnel Diodes on Silicon

3.1 Introduction

Continuous scaling of traditional Si CMOS technology has seen the advancement of the semiconductor industry in the past few decades. However, shrinking the devices comes at the cost of degraded electrical performance in logic applications by reducing the I_{on}/I_{off} ratio. Another inherent issue with device scaling is the power consumption, which can be improved by reducing the supply voltage (V_{DD}) for integrated circuits. In recent years, there has been a drive to replace the traditional Si channel with III-V semiconductors that have lower effective masses and direct band gaps for ultra-low power electronic applications [69]. Owing to the unavailability of larger wafer sizes for III-V substrates and the cost disadvantage for high-volume manufacturing, such implementation would require the monolithic integration of various III-V materials on silicon with low enough surface defects to fabricate surface channel transistors [70]. The integration of III-V compound semiconductors with Si can also combine the cost advantage and maturity of the Si technology with the superior performance of these III-V materials.

Along with a new integration platform, the Tunnel field effect transistor (TFET) has emerged as a possible replacement for the traditional CMOS architecture. The TFET operates using the principle of band-to-band tunneling (BTBT) where charged carriers are transferred from one energy band to another with a gated p^+-i-n^+ structure. This allows a sub-threshold swing (SS) of less than 60 mV/dec at 300 K, which is the fundamental limit in MOSFETs due to thermal injection of charged carriers over a potential barrier [4].

Reducing the SS below the fundamental limit for traditional Si CMOS can enable ultra-low power electronics with supply voltages of less than 0.5 V. Therefore, the integration of III-V TFETs on a Si platform is highly desirable for next-generation post-Si-CMOS microelectronics.

However, an inherent issue in TFETs is the realization of high ON currents (I_{on}), which is limited by the transmission probability of the interband-tunneling barrier [71]. The broken-gap heterojunction consisting of *n*-InAs and *p*-GaSb, first discovered by Sakaki *et al.* in 1977 has been shown to have the lowest effective tunneling barriers and is one of the top candidates for high on current in III-V TFETs [72]. Record high I_{on} of 180 μA/μm at $V_{DS} = V_{GS} = 0.5$V with an I_{on}/I_{off} ratio of 6×10^3 have been reported for gate-recessed vertical InAs/GaSb TFETs [33]. This broken-gap heterojunction has also shown the highest peak current density of 2.2 MA/cm^2 and Zener current density of 11 MA/cm^2 at -0.3 V as a result of optimized band-to-band carrier tunneling in heavily doped Esaki tunnel diodes [36]. All these results have been obtained through lattice-matched MBE growth on GaSb substrates.

Conversely, while growing III-V semiconductors on lattice mismatched substrates, dislocations and structural defects can dominate the heterostructure and enhance Shockley-Read-Hall (SRH) generation-recombination (G-R) as well as trap-assisted tunneling or interband tunneling increasing the OFF state current [73]. The crystalline and interface quality of the III-V heterojunction plays a significant role in determining higher I_{on}, lower I_{off}, and an improved I_{on}/I_{off} ratio [74, 75]. Therefore, the integration of InAs/GaSb broken-gap heterojunction on lattice-mismatched substrates needs the careful selection and

implementation of suitable MBE growth techniques that minimize the propagation of threading dislocations into the active device region.

In this work, we compare the structural properties and electrical performance of InAs/GaSb p^+-i-n^+ Esaki diodes with a GaSb i-layer on various platforms, viz., GaSb (control), GaAs, $SrTiO_3$/Si, and AlSb/Si. Since, TFETs operate as reversed-biased p^+-i-n^+ diodes with a gate over the intrinsic region, the OFF state current of a TFET can be defined as the reverse bias current or leakage current [76]. The forward bias characteristics for Esaki tunnel diodes include important parameters such as peak current density (J_P), peak valley density (J_V) and the peak to valley current ratio (PVCR) which are important figures if merit for evaluating the tunneling probability at the heterojunction [77]. By comparing the performance of the same device structure on several different platforms, we can assess the advantages and limitations for various integration schemes. The results presented here hold important implications for the integration of III-V TFETs on Si and GaAs substrates for future advancement of low-power electronic applications and tunnel-junctions in photovoltaics.

3.2 III-V Tunnel-FET: A Potential post-CMOS solution

3.2.1 Basic Physics of Tunnel-FETs

In a traditional MOSFET, the transistor is operated by thermionic emission of charged carriers over a potential barrier, which creates a fundamental limit to the transition slope of the drain current between the ON and OFF states. The gate voltage (V_G) needed to change the drain current (I_{DS}) by one order of magnitude when the transistor is operated in the subthreshold region is given by the sub-threshold swing (SS) as follows [4]:

$$SS = \frac{dV_g}{d\ log_{10} I_{DS}} \cong \left(1 + \frac{C_d}{C_{ox}}\right) ln\ 10 \frac{kT}{q} \qquad (4)$$

where C_d is the depletion capacitance, C_{ox} is the oxide capacitance and T is the temperature. The theoretical minimum value of SS from this expression at room temperature is 60 mV/dec. This means that will take at least 60 mV to increase the drain current by one order of magnitude. Current Si-MOSFET technology can obtain a SS of 100 mV/dec which means that to achieve an I_{on}/I_{off} ratio of 10^4, it requires 400 mV, and 800mV for CMOS as it consists of both *n*-MOSFET and *p*-MOSFET. The average subthreshold swing can be defined as:

$$S_{avg} = \frac{V_{DD}}{log_{10}\left(\frac{I_{on}}{I_{off}}\right)} \qquad (5)$$

Therefore, to enable low-power devices and reduce power consumption and heat dissipation, the S_{avg} needs to be lowered below 60 mV/dec to enable successful scaling of the supply voltage V_{DD} which requires steep-slope devices with large I_{on}/I_{off} ratios. In contrast to a MOSFET where carriers are thermally injected over the source-channel energy barrier, the Tunnel-FET (TFET) uses interband tunneling to inject carriers into the channel of a p^+-i-n^+ structure. The tunneling in the p^+-i-n^+ region can be controlled by applying the gate bias on the intrinsic-channel region just as in the case of a MOSFET, thereby switching the TFET between ON and OFF states. As shown in Fig. 31, a TFET consists of a reverse-biased p^+-i-n^+ junction with a gate over the intrinsic region. In the off state when no gate bias is applied, the valence band edge of the intrinsic channel is below the conduction band edge of the n^+ source region leading to very low BTBT currents. On the application of a negative gate voltage, the bands in the channel are pulled up and this

creates a conductive channel for the electrons to tunnel from the source conduction band to the channel valence band, which is limited to the low-energy $\Delta\Phi$ region. Contrary to MOSFETs, where the channel conduction is limited by the high-energy Fermi-tail of the carriers at the source-channel potential barrier, current generation in TFETs is enabled by the filtering of the high energy tail, thereby allowing carriers in the energy window ($\Delta\Phi$) to contribute to the on-state current and effectively producing a sub-60 mV/dec subthreshold swing. Another important thing to note is that SS in a TFET is not constant but a function of the applied gate bias as a consequence of the tunneling mechanism as shown in Fig. 31c.

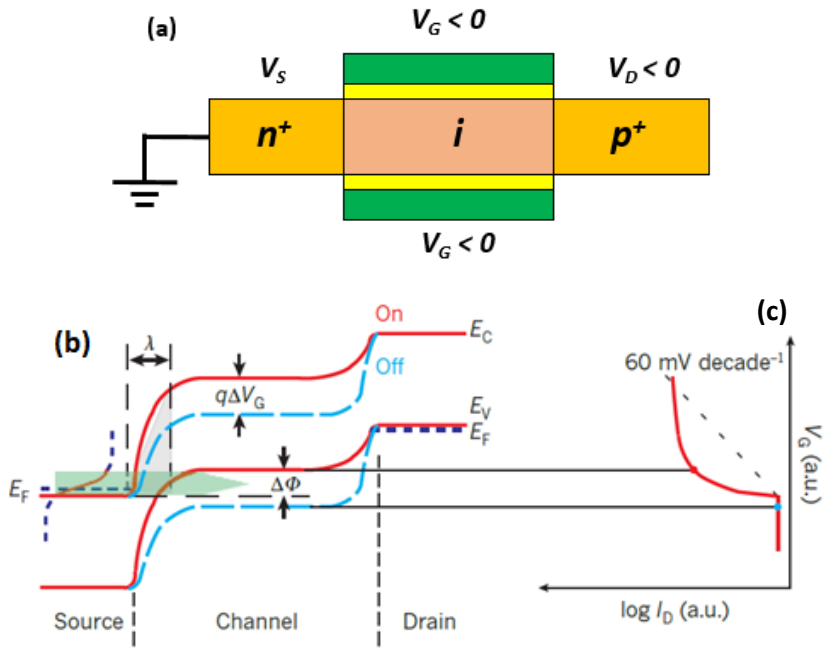

Fig. 31 (a) Schematic of a *p*-type TFET showing the applied gate voltage (V_G), source bias (V_S) and the drain bias (V_D). (b) The energy band-diagram for both the ON and OFF states in the *p*-type TFET achieved using gate voltage and source-channel tunnel junction modulation. (c) The resultant transfer characteristics (log I_D-V_G) show that the subthreshold slope depends on the applied gate bias and is not linear on a log scale as for a MOSFET.

In principle, the TFET is an ambipolar device which can be made *p*-type or *n*-type based on the dominant carrier concentration. Fig. 31b represents a *p*-type homojunction

TFET where the p^+-i-n^+junction is reverse-biased, and hole-conduction dominates in the on-state as the holes move from the source (n^+) conduction band to the drain (p^+) valence band. For a *n*-type TFET, the opposite holds true where the electrons move from the (p^+) source valence band to the drain (n^+) conduction band under reverse bias. The ambipolarity can however be suppressed by using asymmetric doping profiles or by the use of heterojunctions to block the movement of one type of charged carriers. III-V semiconductors not only provide heterojunction engineering capabilities but also offer low effective mass for carriers and low band-gaps resulting in higher on currents and lower-supply voltages. The on currents achieved in TFETs are directly proportional to the tunneling probability at the source-channel which can be estimated using the Wentzel–Kramer–Brillouin (WKB) approximation as follows [29]:

$$I_{on} \sim T_{WKB} \sim exp(-\beta E_{Beff}^{1.5}) \qquad (6)$$

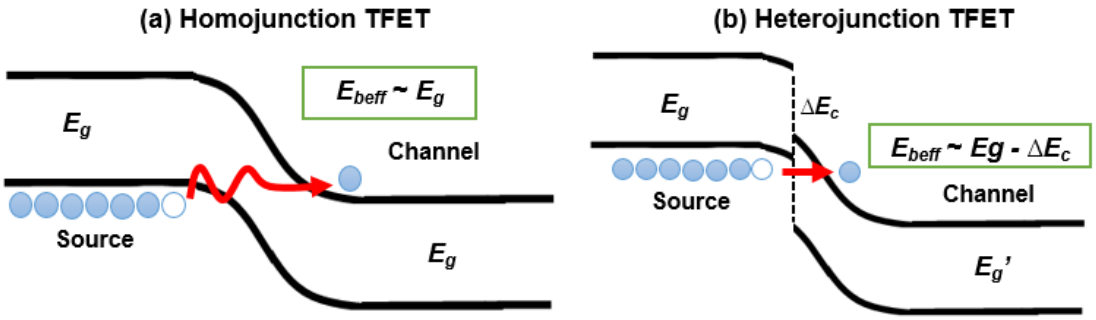

Fig. 32 Tunneling barrier engineering from (a) homojunction TFET to (b) heterojunction TFET improves the on-state current by reduction of the effective tunneling barrier E_{Beff}.

where β depends on the carrier effective mass (m^*) and screening tunneling length (λ), and E_{Beff} is the effective tunneling barrier at the junction. For III-V heterojunctions with type-II and type-III band line-ups, the E_{Beff} can be reduced significantly to allow high on currents for heterojunction-TFETs (Fig. 32).

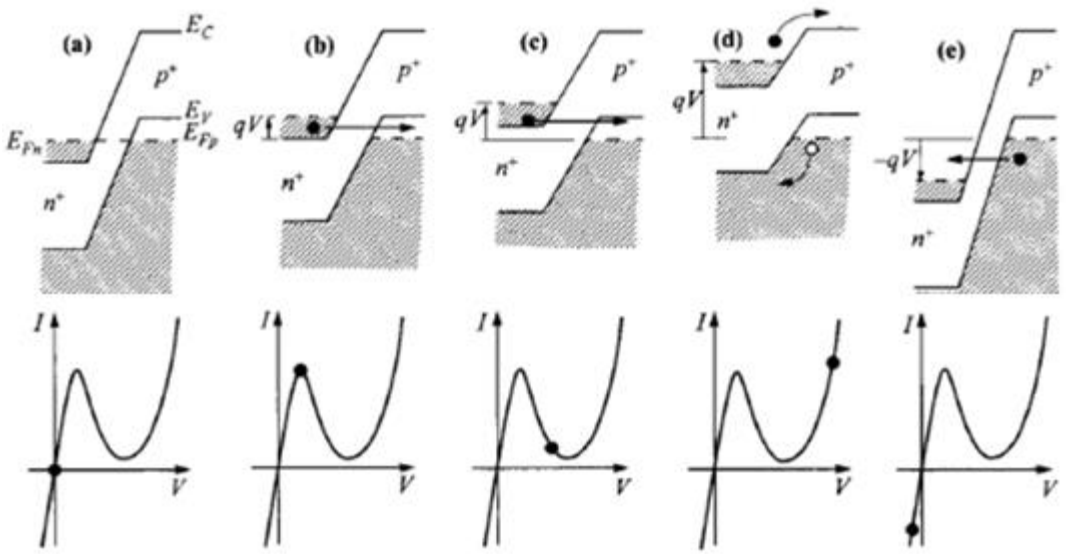

Fig. 33 *I-V* characteristics and corresponding energy-band diagram of a p^+-n^+ homojunction Esaki tunnel diode. *Courtesy: Sze*

3.2.2 Working principle of an Esaki tunnel diode

Esaki diodes are the ideal candidates for understanding the band-to-band-tunneling (BTBT) in TFETs with different band-alignments at the heterojunctions. An Esaki diode is a p^+-i-n^+junction with no gate over the intrinsic channel. This helps in evaluating the tunneling junction without parasitic effects from the gate capacitance and interface trap density from the semiconductor/high-k dielectric interface. The characteristics of a typical homojunction Esaki tunneling diode can be easily understood by examining the energy band diagram and taking into account the different processes that occur as a function of applied bias (Fig. 33).

At equilibrium, the Fermi levels for both the p^+ and n^+ sides are inside the valence and conduction bands respectively, due to degenerate levels of doping. Therefore, at zero bias there is not current flow. If a small forward bias is applied, the potential barrier is still very high so there is no noticeable injection and forward current through the junction. However, electrons in the conduction band of the n^+ region will tunnel to the empty states

of the valence band in p^+ region. This creates a forward bias tunnel current. With increase in forward bias, a maximum tunneling current (I_P) is achieved after which a decrease in the current begins as the number of electrons in the n^+ side that are directly opposite to the empty states in the valence band (in terms of their energy) decrease (Fig. 33c). As more forward voltage is applied, the tunneling current drops to zero. But the regular diode forward current due to thermionic emission increases due to the lower potential barrier, which leads to the valley current (I_V). With further voltage increase, the tunnel diode *I-V* characteristic is similar to that of a regular *p-n* diode (Fig. 33d). In case of reverse bias (Fig. 33e), electrons in the valence band of the p^+ side tunnel directly towards the empty states present in the conduction band of the n^+ side creating large tunneling current which increases with the application of reverse voltage. The region between the peak current and the valley current is known as the negative differential resistance (NDR) region. Important metrics for Esaki diode performance are the peak-to-valley current ratio (PVCR) and the peak current density (J_P) which correlate directly to the drive current in a TFET as well as the subthreshold swing. An improved J_P indicates increased tunneling probability at the junction, where as a high PVCR relates to low valley current density (J_V) which is a result of trap-assisted tunneling and structural defects in the tunnel diode.

3.2.3 Conductance analysis for broken-gap tunnel diodes

Heterojunction tunneling junctions are expected to have the highest ON currents as they possess lower effective tunneling barriers, which increases the transmission probability. Additionally, the channel conductance is much improved due to the overlap between the conduction band on one side and the valence band on the other side of the tunnel junction. The band-edges provide a sharp cut-off in the density of states, thereby

removing the high-energy thermal tail from the Fermi-distribution and allowing sub-60 mV/dec operation. As mentioned previously, TFETs are assessed on the basis of their on-state current and subthreshold swing (SS) for use in low-power applications. These important characteristics for TFET devices depend not only on the quality of the tunneling hetero-junction, but also on the quality of the gate oxide-semiconductor interface, the TFET geometry, contact and series resistance, amongst other factors.

Since a TFET is just a gated tunnel diode, two-terminal Esaki diode measurements offer a great alternative to separate the parasitic effects of the third-gate oxide terminal and assess solely the quality of the tunneling junction and the heterointerface [77]. Using 2-terminal measurements, the electrical characteristics of the Esaki p^+-i-n^+ junction can be used to study the effect of structural defects and interface quality on device performance. Absolute conductance for a 2-terminal diode has recently been proposed as a tool to get an idea of the subthreshold swing in a 3-terminal TFET [78]. This technique shows the contribution to the subthreshold swing of a TFET, solely due to the tunneling junction. This analysis can be used to improve the conductance slope of an Esaki diode, which directly leads to a steeper SS for TFETs designed using these tunnel junctions. The tunneling current density at a tunnel junction can be given by the following expression:

$$J \propto \int [F_C(E) - F_V(E)] \,.\, T.\, N_C(E) N_V(E) \boldsymbol{dE} \qquad (7)$$

where $F_C(E)$ and $F_V(E)$ are the Fermi-Dirac distributions on the n^+ and p^+ sides, respectively, T is the tunneling probability, and $N_C(E)$ and $N_V(E)$ are the density of states in the conduction and valence band, respectively. The applied voltage on p^+-i-n^+junction changes the band overlap by shifting $N_C(E)$ and $N_V(E)$ away from each other as well as

changes the difference in the Fermi levels across the junction $F_C(E)$ - $F_V(E)$. For a 3-terminal device, the gate voltage controls the overlap between $N_C(E)$ and $N_V(E)$ but has no effect on the value of $F_C(E)$ - $F_V(E)$, which is solely controlled by the source-drain bias and therefore, has no effect on the transfer characteristics and the subthreshold slope of a TFET.

In order to approximate this scenario in a 2-terminal diode, the $F_C(E)$ - $F_V(E)$ factor needs to be removed from the integrand. To a first order, the difference in Fermi-levels across the tunnel junction is simply the applied voltage (V_a) that drops across the junction. If the applied voltage is around $4k_BT/q$ (100 mV), the first order approximation holds good and $F_C(E)$ - $F_V(E) \approx V_a$. Even if the applied voltage bias is as high as 400 mV, the correction factor is only 4 times, which is still negligible compared to exponential increase in the joint density of states ($N_C(E).N_V(E)$). Therefore, the absolute conductance (G) of the junction can be used to examine the scenario in a diode, and the conductance slope gives a comparable metric to the subthreshold slope for a TFET, if the diode was converted to a 3-terminal device.

$$G = \frac{J}{V_a} \approx \int T.N_C(E)N_V(E)\boldsymbol{dE} \qquad (8)$$

By plotting the G-V characteristics of a tunnel diode, the conductance slope gives an equivalent metric to the subthreshold swing in terms of mV/dec. The conductance slope (G*) can be expressed as follows:

$$G^* = \frac{dV_a}{d\,log\,G}\ mV/dec \qquad (9)$$

It is also important to note that the conductance slope is calculated in the NDR region of the Esaki-diode G-V curve. Even though there are some instability-driven

oscillations in NDR region, an average value of the conductance slope can be calculate in this region using the following equation:

$$G^* = \frac{|V_P - V_V|}{\left|log_{10}\left(\frac{J_P}{V_P}\right) - log_{10}\left(\frac{J_V}{V_V}\right)\right|}\ mV/dec \qquad (10)$$

where J_P is the peak current density, V_P is the peak voltage, J_V is the valley current density, and V_V is the valley voltage.

3.3 Experimental Procedure

3.3.1 Growth of InAs/GaSb p^+-i-n^+ diodes using MBE

The basic p^+-i-n^+ structure consisting of p^+ GaSb and n^+ InAs was grown on various substrates for comparison of crystalline quality, defects and surface morphology along with electrical performance. For the control sample (TD1) as shown in Fig. 34a, 300 nm p^+ GaSb (Be-doped: 5×10^{18} cm^{-3}) was grown on a *p*-GaSb (001) substrate, followed by a 3 nm thick intrinsic GaSb layer and a top layer of 25 nm n^+ InAs (Te-doped: 1×10^{19} cm^{-3}). The thickness of the InAs was so chosen as to not exceed the critical thickness, h_c, according to the expression [79]:

$$h_c = \frac{a_0\left(1 - \frac{\nu_{PR}}{4}\right)\left[ln\left(\frac{h_c\sqrt{2}}{a_0}\right) + 1\right]}{2\sqrt{2}\pi|f|(1+\nu_{PR})} \qquad (11)$$

where a_o is the lattice constant of the substrate, f is the lattice mismatch between the substrate and the epilayer, and ν_{PR} is Poisson's ratio. For an InAs epilayer on GaSb substrate, the critical thickness is almost 40 nm before relaxation occurs leading to misfit and threading dislocations in the epilayer.

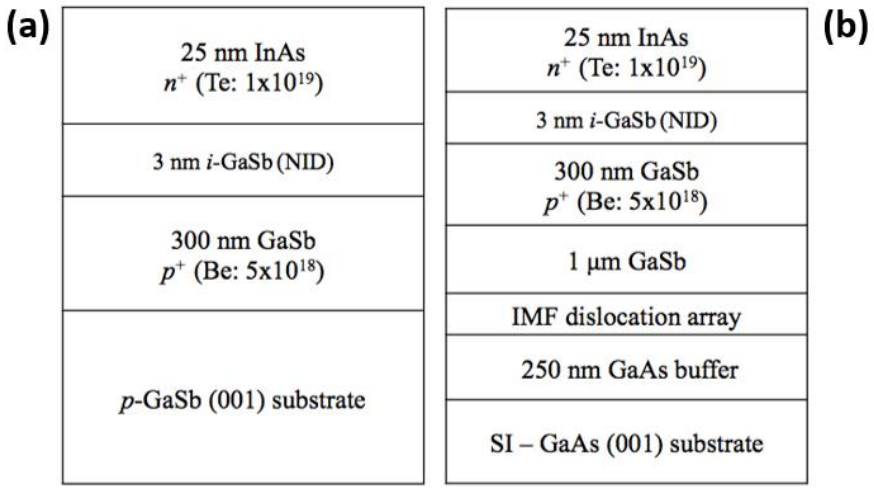

Fig. 34 InAs/GaSb broken-gap p^+-i-n^+ Esaki tunnel diode structures grown using MBE on (a) native GaSb substrate - TD1 and (b) SI-GaAs substrate using the IMF array technique - TD2.

For the integration of InAs/GaSb p^+-i-n^+ Esaki diodes on GaAs substrate, the well-established interfacial misfit dislocation (IMF) array technique was used to grow a 1µm thick GaSb layer on a (4 × 2) reconstructed GaAs (001) surface as discussed in the previous chapter. Using the IMF technique, highly two-dimensional periodic arrays of pure-edge 90^o misfit dislocations can be formed in both the [110] and [$\bar{1}$10] directions, relieving most of the excess strain due to the 7% lattice mismatch at the GaSb/GaAs hetero-interface. The periodic nature of the misfit dislocations is evident from the fact that exactly 13 GaSb lattice sites can be grown on 14 GaAs lattice sites along the [110] direction. Since 90^o pure-edge dislocation travel parallel to the growth plane rather than into the epilayers, the structural quality of the GaSb epilayer grown on GaAs is close to the optimal under this technique. The same p^+-i-n^+structure was then grown on top of the undoped GaSb layer on the GaAs (100) substrate and the complete structure (TD2) is shown in Fig. 34b.

The integration of GaSb on Si (001) is quite challenging, as it involves not only a large lattice mismatch of 13% but also the growth of a polar material on a non-polar substrate creating anti-phase domains in the epilayer. We employed two different buffer

layer schemes to achieve high quality growth of GaSb on Si (001) substrates. The first approach involved the growth of an AlSb buffer layer on Si (001) using the IMF array technique as discussed previously. The 12% mismatch between the AlSb layer and Si was relieved at the interface through the formation of a 2D periodic array of 90^{o} edge-type misfit dislocations, leading to a high quality relaxed buffer layer of 250 nm AlSb. The use of miscut substrates, in this case a Si (001) miscut 4^{o} towards the <110> direction also aids in the suppression of anti-phase domain (APD) boundaries. The AlSb layer now serves as a buffer layer for the subsequent growth of GaSb, which is much closely lattice-matched to AlSb than Si. The p^{+}-i-n^{+} structure is then grown on top of the 50 nm GaSb layer and the complete structure (TD3) grown using this approach is shown in Fig. 35a.

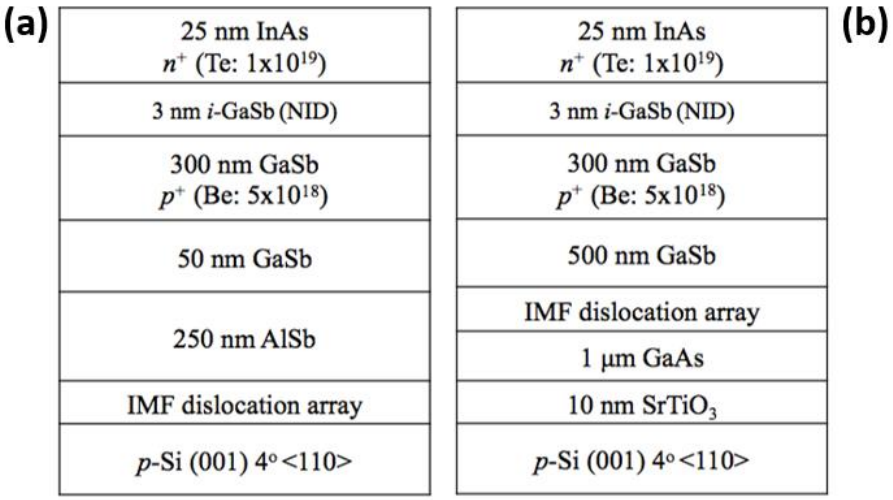

Fig. 35 InAs/GaSb broken-gap p^{+}-i-n^{+} Esaki tunnel diode structures grown using MBE on (a) a miscut Si substrate using an AlSb buffer layer - TD3 and (b) using an $SrTiO_3$/GaAs buffer scheme - TD4.

The second buffer layer scheme involves the growth of a crystalline oxide buffer layer of $SrTiO_3$ (STO) on a Si (001) miscut substrate to integrate high-crystalline quality GaAs. The $SrTiO_3$ lattice (a_{STO} = 3.905 Å) undergoes a 45° rotation to accommodate the high lattice mismatch with the underlying Si (001) (a_{Si} = 5.431 Å) leading to a strain of 1.7%. The GaAs lattice (a_{GaAs} = 5.653 Å) grown is now strained 2.4% with respect to the

45^{o} rotated $SrTiO_3$ lattice, thereby enabling the reduction from the original 4% strain for the GaAs/Si system. A two-step growth process utilizing a high temperature nucleation layer of GaAs, followed by a low-temperature GaAs layer at a higher growth rate was employed. As discussed in Chapter 2, Sr-terminated STO surface has the optimum surface energy for successful wetting of GaAs epilayer and results in GaAs films with improved structural qualities and extremely smooth surface morphologies. The successful growth of STO buffer along with GaAs epilayer is followed by the IMF growth of 500 nm GaSb layer as discussed above. Following this, the same InAs/GaSb p^{+}-i-n^{+} Esaki diode structure is grown as for all the others samples. The complete structure (TD4) grown using the STO buffer scheme is shown in Fig. 35b. The structural properties of all the grown samples were characterized using double crystal X-ray diffraction (XRD) and the surface morphologies were mapped using atomic force microscopy (AFM) in tapping mode. The defect analysis was performed using high-resolution cross-sectional transmission electron microscopy (TEM).

3.3.2 Fabrication and Electrical Characterization of Esaki Diodes

Esaki diode fabrication was performed using general procedures established in prior work. First, the sample surface was cleaned in a 10:1 H_2O:HCl solution for 10 seconds, followed by a 200 nm thick layer of molybdenum (Mo) using RF sputtering. nLOF, diluted in PGMEA (≈1:1) and e-beam lithography defined the metal contacts. SF_6 -based reactive ion etching (RIE) was used to define mesa contacts ranging from 100 nm to 20 μm squares. A brief oxygen surface clean was used to remove residual photoresist. A 20:1 citric acid ($C_6H_8O_7$): hydrogen peroxide (H_2O_2) solution etched the sample for 65 seconds to form Esaki diode mesas. The contact area and undercut were measured for

representative devices in a scanning electron microscope (SEM) to increase the precision of the J_P estimation (Fig. 36a). Bis-benzocyclobutane (BCB) was then used as an inter-layer dielectric (ILD) and planarization layer. Level 2 metal contacts were then defined by a second e-beam lithography and a lift-off process, producing devices depicted in Fig. 36b.

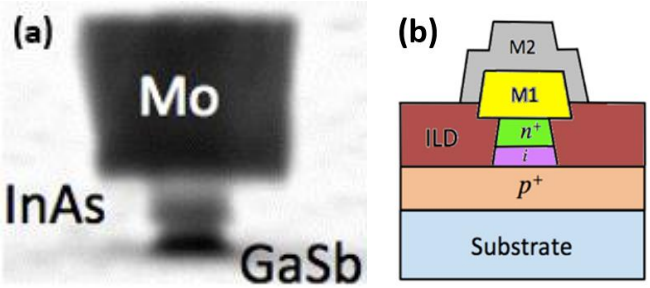

Fig. 36 (a) Scanning electron micrograph of a fabricated Esaki diode. The sample is then rotated to a steep angle, often 84◦, or higher, to measure the undercut in two perpendicular planes to account for etch anisotropy. (b) A second level metal and ILD must be used with these mesas to contact devices below 2 μm widths.

The electrical properties of the InAs/GaSb Esaki tunnel diodes were assessed by measuring the current-voltage (*I-V*) characteristics using a Keithley 4200 Semiconductor Parameter Analyzer. A large area Esaki diode (greater than 1000× the measured junction area) was used as a virtual ground. The ground plane was designed to fully surround the devices to minimize any effect from current crowding as this is critical for measuring high current density tunnel junctions and minimizes unwanted resistive latching that obscures the negative differential resistance (NDR). Data was collected for over 100 devices on each of the four different platforms including the control sample, GaAs substrate, $SrTiO_3$ buffer on Si, and AlSb buffer on Si miscut wafers. J_P and J_V were extracted and corrected based on the area analysis and a statistical analysis was performed to get a representative value of J_P, PVCR and G^* for the broken-gap Esaki tunnel diodes on different lattice mismatched substrates.

3.4 Results & Discussion

3.4.1 Structural Properties

To assess the crystalline quality and strain properties of the epilayers grown for the four different samples, high-resolution X-ray diffraction (HRXRD) measurements were carried out for all the different samples on a Bede-D1 diffractometer with a Cu-Kα1 x-ray source. Coupled Omega-2theta scans for the GaSb (004) and InAs (004) diffraction peaks in the p^+-i-n^+ structure show the presence of strained InAs with respect to the underlying GaSb lattice (Fig. 37a). As mentioned before, the InAs layer is grown below its critical thickness to avoid strain relaxation that can lead to defects in this epilayer.

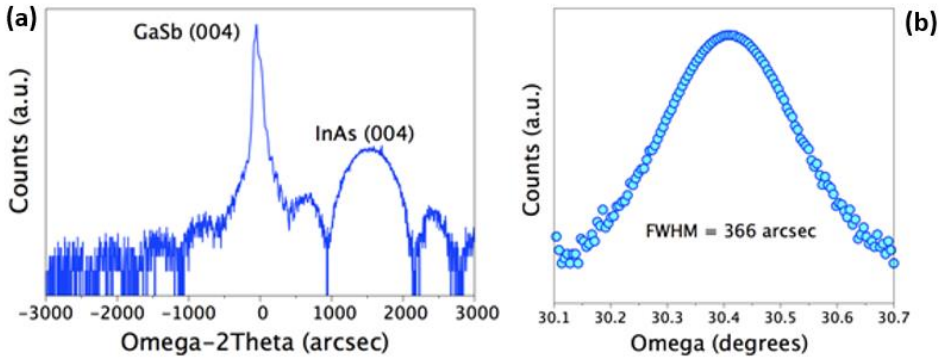

Fig. 37 (a) Coupled omega-2theta scan showing the GaSb (004) and InAs (004) diffraction peaks for sample TD1. The InAs epilayer is grown below the critical thickness to avoid relaxation and is strained with respect to the underlying GaSb lattice. (b) GaSb (004) omega rocking curve for sample TD2 with a FWHM of 366 arcsecs, which corresponds to a threading dislocation density of approximately 3.89×10^8 cm^{-2}.

An important metric to compare across the different integration platforms is the threading dislocation density in the GaSb epilayer, which is directly influenced by the epitaxial quality of the underlying buffer layers and substrates. The electrical performance of the Esaki diodes will be affected by the number of defects within the GaSb layer due to excess leakage currents. Therefore, to determine the crystalline quality of the GaSb epilayers, rocking curve analysis was performed for the GaSb (004) diffraction peak (Fig. 37b), which can estimate the threading dislocation density (TDD) from the full-width at

half-maximum (FWHM) [80]. The following equation can be used to estimate the TDD using the FWHM of the GaSb (004) rocking curve:

$$TDD \approx \frac{\beta_m^2}{4.36\, b^2} \qquad (12)$$

where β_m is the FWHM in units of radians and b is the Burgers vector which is assumed to be *a/2*[110] for GaSb. The defect density calculated using this method for III-V layers grown on Si has been shown to be within an order of magnitude as measured by TEM.

The control sample TD1 shows the lowest value of FWHM since it employs a lattice-matched epitaxial growth mode (Table 3). Sample TD2 shows a higher value of dislocation density since the IMF growth of GaSb on lattice-mismatched GaAs surface produces a significant number of 60^o misfit dislocations along with the non-propagating 90^o pure-edge dislocations [81]. Ideally, if the growth technique produces only 90^o dislocations, then no threading segments are produced since these dislocations are elastically stable and cannot glide in the closed packed {111} planes. However, there is always a finite number of 60^o dislocations that nucleate in the GaSb epilayer and can easily glide along the {111} planes resulting in threading segments. This leads to an increased dislocation density measured in the GaSb epilayer and the overall structure for TD2.

Table 3 A comparison of the threading dislocation densities (TDD) of the GaSb epilayers for the p^+-i-n^+ Esaki diode heterostructures on the different integration platforms.

Sample	*FWHM (arcsecs)*	*TDD (cm^{-2})*
TD1	70	Lattice-matched
TD2	366	3.89×10^8
TD3	1408	5.77×10^9
TD4	883	2.27×10^9

The p^+-i-n^+ structure grown on miscut silicon using the AlSb buffer layer approach, TD3, shows almost one order of magnitude higher value for TDD as compared to TD2 which can be attributed to the dislocations originating at the AlSb-Si heterointerface. In this case, the possible formation of anti-phase domains (APDs) and the presence of both 60^o and 90^o dislocations that propagate vertically into the epilayers is responsible for the increase in dislocation density [82]. Another possible reason that can lead to the broadening of the rocking curve is the large thermal mismatch between the III-V layers and the Si substrate in sample TD3. During the cool down period from growth temperatures of around 500 ^{o}C to room temperature, the component layers contract at different rates creating additional structural defects within the p^+-i-n^+ stack. For sample TD4 grown using the GaAs/STO buffer on Si, the dislocation density is less compared to that of sample TD3. Although the same type of dislocations and defects are present here as in the samples above, the reduction in dislocation density is due to the fact that this integration technique creates lower number of defects as the lattice mismatch is gradually reduced over the intermediate STO buffer layer [68]. The resultant GaAs layer is much smoother and has a lower dislocation density as compared to GaAs grown directly on Si. This provides a smoother and higher crystalline quality platform for the IMF-based growth of GaSb on the GaAs epilayer.

3.4.2 InAs/GaSb Interface Properties

When looking at device applications for the p^+-i-n^+ Esaki diode structures, it is important to analyze the interface at the heterojunction between InAs and GaSb. This is because most lattice-mismatched systems have the tendency to form dislocations at the interface, which lead to structural defects in the device layers and degrade electrical

performance. The presence of defect states at the InAs/GaSb interface can lead to leakage in the OFF state due to trap-assisted tunneling. Additionally, the change in band alignment at the interface due to the presence of these electrically active defects can cause local band-bending and affect the conductance slope of these devices.

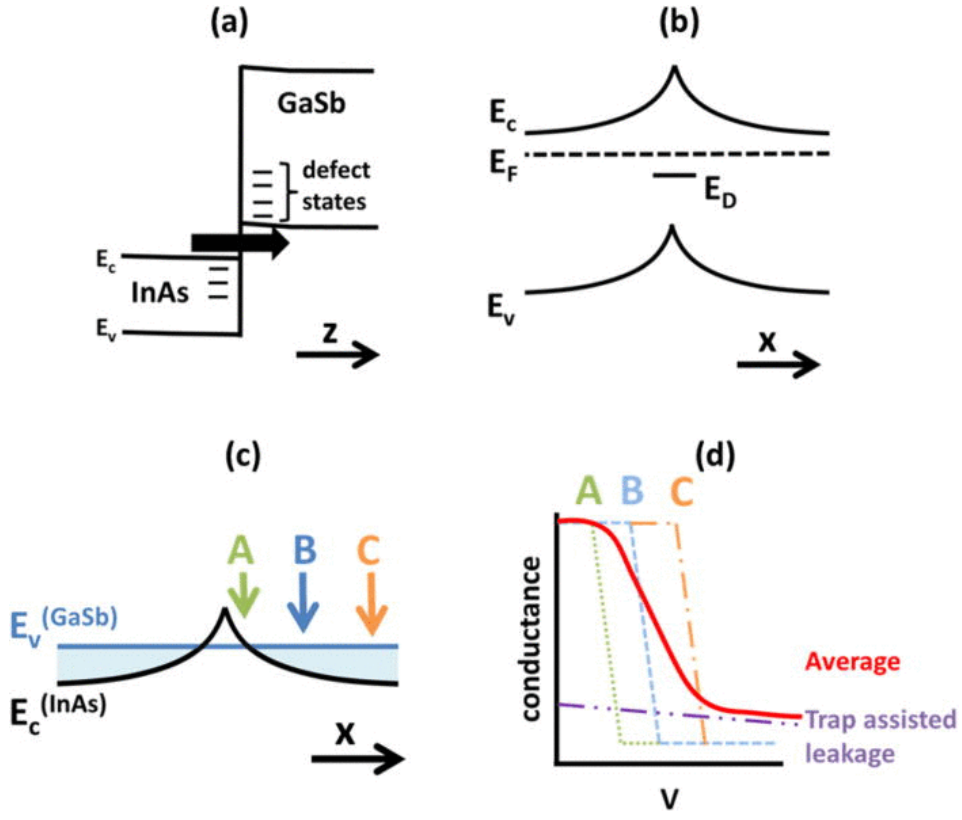

Fig. 38 (a) Band diagram of InAs/GaSb diode. The arrow shows the direction of electron current due to tunnelling, and defect states are shown near the interface, which can also act as sites for tunnelling. (b) Band diagram of InAs along a direction parallel to the interface, showing a defect state and an example of band bending around the defect (c) Valence band energy of GaSb near the interface shown. Light blue region represents where tunnelling can occur, and three reference points are marked as A, B, and C. (d) Conductance-voltage curve showing sharpness of switching for current at each point A, B, and C, as well as a trap-assisted leakage current. The solid red curve shows the measured result, which is a weighted average of all of these conductance pathways, and the conductance slope is considerably less steep. [78]

Fig. 38a shows the effect of defect states present in the band-gap of either InAs or GaSb can induce OFF state current through tunneling mechanisms. Fig. 38b shows how interface defects can alter the local band-alignment and can change the tunneling current at different voltages. If we assume that the GaSb valence band edge remains constant, and

the InAs conduction band edge is altered by the interface defects, tunneling will occur as long as the GaSb VB is below the InAs CB (Fig. 38c). As positive bias is applied, the bands move closer and the tunneling at point A will turn-off before point C, which leads to non-uniform turn-off of the tunneling current. This will directly lead to a change in the peak and valley voltages in the NDR region, and consequently reduce the steepness of the conductance slope (Fig. 38d) as it will be a convolution of all the three different curves from points A-C. Therefore, a high dislocation density in the films and interface defects will lead to a less-steeper subthreshold swing for a TFET-device application.

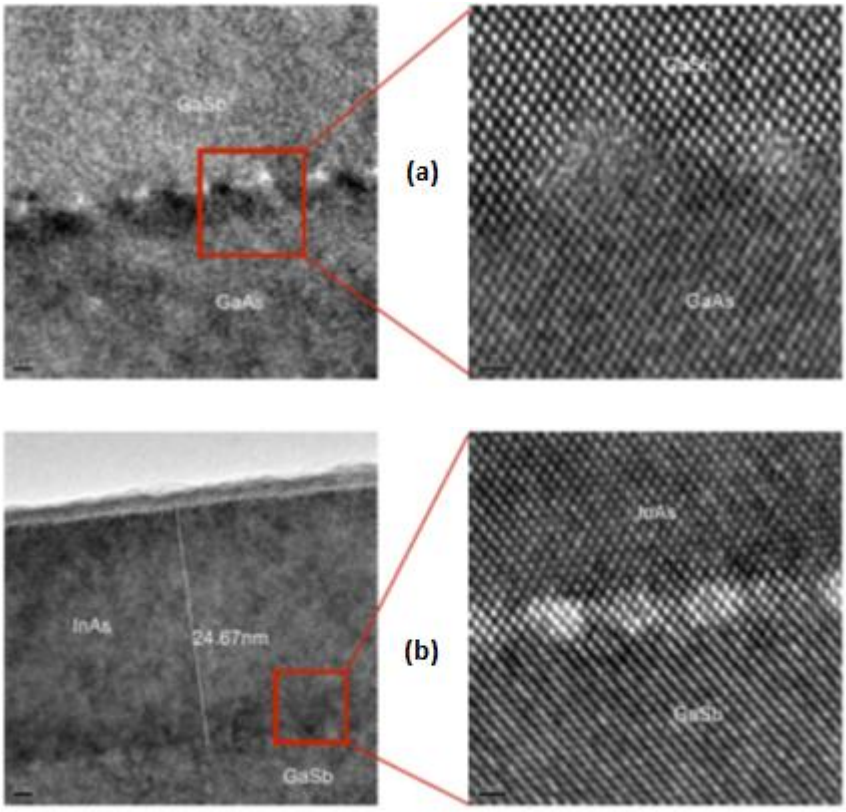

Fig. 39 (a) Cross-sectional TEM image of the GaAs-GaSb interface showing the presence of periodic interface-misfit dislocations in the [110] direction. (b) TEM image of the InAs-GaSb heterointerface showing the absence of dislocations and structural defects, with local strain present at the interface.

Fig. 39a shows the cross-sectional TEM image of the GaAs-GaSb interface for sample TD2 where the Esaki diode is grown on SI-GaAs using the IMF array technique.

This micrograph shows the clear presence of a periodic array of misfit dislocations at the interface in the [110] direction. Although there are no 60^{o} dislocations in this image, the XRD analysis done previously shows the higher dislocation density as compared to the control sample TD1. The TEM image of the InAs-GaSb interface also shows the absence of significant dislocations at the interface (Fig. 39b). Although there is local strain at the interface, the growth conditions chosen for all the samples should inhibit the relaxation of InAs on GaSb as the InAs layer thickness is grown much below the critical thickness as explained the Section 3.4.1. This is evident from the absence of dislocations at the InAs/GaSb interface. The sharpness of the interface also rules at any possibilities of inter-diffusion of constituent atoms between the two layers, which is a common observance in MOCVD epitaxy of InAs/GaSb heterostructures. This abrupt interface is also ideal for device applications as it closely follows the assumptions for band-alignments in heterojunctions under the assumption of sharp interfaces.

3.4.3 Surface Morphology

The surface morphology for these structures is an important parameter for device fabrication as a smooth surface leads to ease in defining device patterns as well as aids in careful etching of the device layers. Surface features also give an insight in to the crystal defects within the epilayers of the grown structure. AFM scans of 10 μm × 10 μm areas were taken on a Veeco Dimension-3100 using a Si tip in tapping-mode to compare the surface features and the root mean square (RMS) roughness among the different samples. The control sample TD1, shows the lowest surface roughness of 0.11 nm as the p^{+}-i-n^{+} structure was grown on a GaSb substrate using the Frank-van der Merwe (FM) growth

mode where the incoming adatoms attach preferentially to surface sites resulting in atomically smooth surfaces.

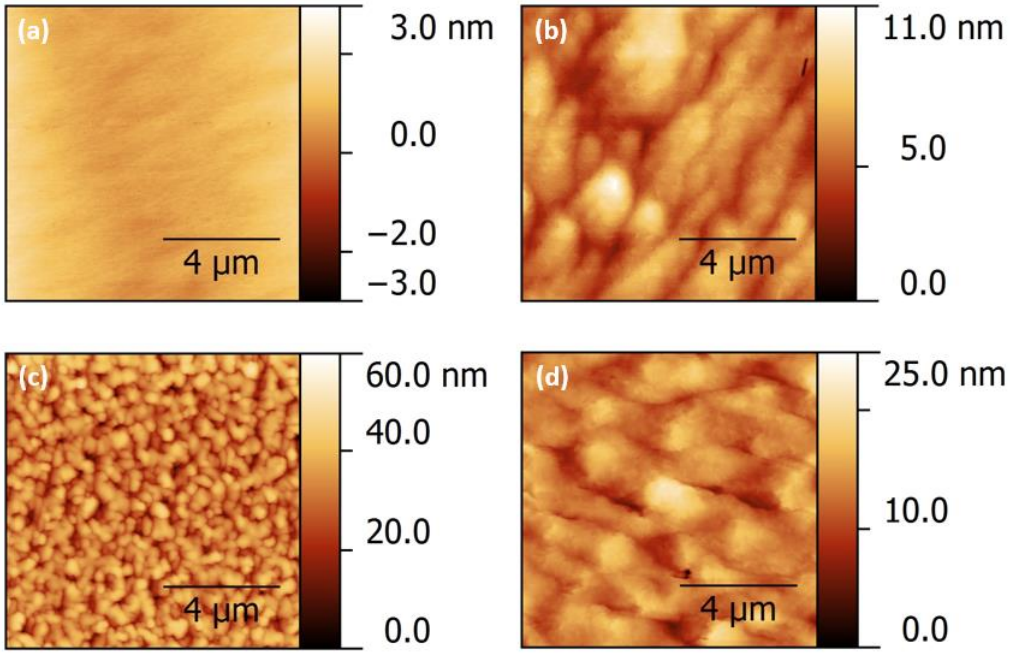

Fig. 40 AFM micrographs of 10 μm × 10 μm areas for (a) control sample - TD1 (b) Esaki diode on GaAs - TD2 (c) InAs/GaSb p^+-i-n^+ on AlSb/Si - TD3 (d) Esaki diode on GaAs/STO/Si - TD4.

The atomic step edges are evident in the surface morphology, which shows that the substrate surface topography was clearly transferred throughout the growth of the whole structure to all the epilayers since the GaSb (001) substrate used was miscut 0.35^o in the <111> direction. Homoepitaxy of GaSb is usually plagued with oval surface defects as a result of limited adatom diffusion on the surface, but no such defects were observed sample TD1 as the growth proceeded in the step-flow regime producing an extremely smooth surface [83]. For sample TD2 with the InAs/GaSb Esaki diode structure on a GaAs substrate, the RMS surface roughness was 1.23 nm. The morphology shows a rough surface with the presence of spiral mounds that are commonly observed in the heteroepitaxy of GaSb on GaAs (001) surfaces [84]. Even though the IMF array technique creates primarily

90^{o} edge dislocations, there are still 60^{o} misfit dislocations that propagate vertically into the epilayers and create the observed surface features. These screw dislocations create threading segments that show a spiral appearance on the sample surface. Group III Ga adatoms that arrive on the surface during the growth process with a high density of screw dislocations, preferentially attach themselves on the step-edge of these spiral features and as growth proceeds, the different spiral mounds coalesce leading to a steady-state step-flow growth mode.

Sample TD3 shows the highest RMS surface roughness of 5.74 nm since the AlSb buffer layer approach creates the highest threading dislocation density from the relaxation that occurs at the AlSb-Si heterointerface. There are no spiral features observed in this case except the presence of mounds or bumps over the entire surface. Although the screw dislocations created at the AlSb-Si interface propagate through the epilayers, the shorter diffusion length of the Al adatom is responsible for the absence of spiral features that were observed in TD2. Due to the presence of a much smoother STO and GaAs buffer layer on Si for TD4, the RMS roughness of this sample is only 2.32 nm. The STO buffer layer helps better relieve the lattice mismatch between the Si and intermediate GaAs epilayer, leading to a lower dislocation density and a smoother surface for the InAs/GaSb p^{+}-i-n^{+}stack in case of TD4. There is still some evidence of spiral features on the surface for this sample, as the Ga adatom diffusion length is large enough to have sufficient mobility on the surface of the epilayer during growth.

3.4.4 Electrical Properties

The working principle of the InAs/GaSb broken-gap Esaki tunnel diodes can be easily understood in terms of the energy band diagram (. A one-dimensional Poisson solver

was used to calculate the conduction and valence band profiles for the InAs/GaSb p^+-i-n^+ junction at equilibrium as well as under forward and reverse bias. At a zero applied bias, the effective tunneling barrier, which corresponds to difference between the conduction band in InAs and the valence band of GaSb at the interface is -150 meV. As forward bias is applied, increased band-bending leads to the lowest conduction sub-band on the InAs side to be pushed above the highest hole sub-band on the GaSb side, disabling direct band-to-band tunneling. This leads to the observation of a negative differential resistance (NDR) region in the *I-V* characteristics [85].

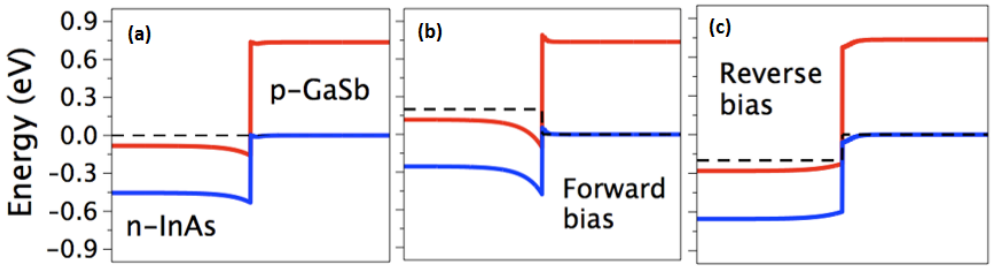

Fig. 41 Poisson simulations for the bandstructure calculation of the InAs/GaSb p^+-i-n^+diode at (a) equilibrium (b) forward bias at +0.20 V and (c) reverse bias at -0.20V.

For electrical characterization of the p^+-i-n^+ Esaki tunnel diodes on various platforms, over 100 devices were measured ranging from 500 nm × 500 nm to 1 μm × 1 μm square. Fig. 42a shows the *I-V* data from the control sample (TD1) clearly depicting the NDR region under forward bias at room temperature. Both the peak current and valley current show excellent linear scaling with area. Representative values of J_P, J_V and PVCR (=J_P/J_V) were extracted for TD1 by doing a statistical analysis and using a Gaussian fit to achieve the mean value and standard deviation (Fig. 42). The conductance slope analysis was performed as detailed in the previous sections to obtain a statistical distribution for G^* and use this as a figure of merit for comparison with the other samples.

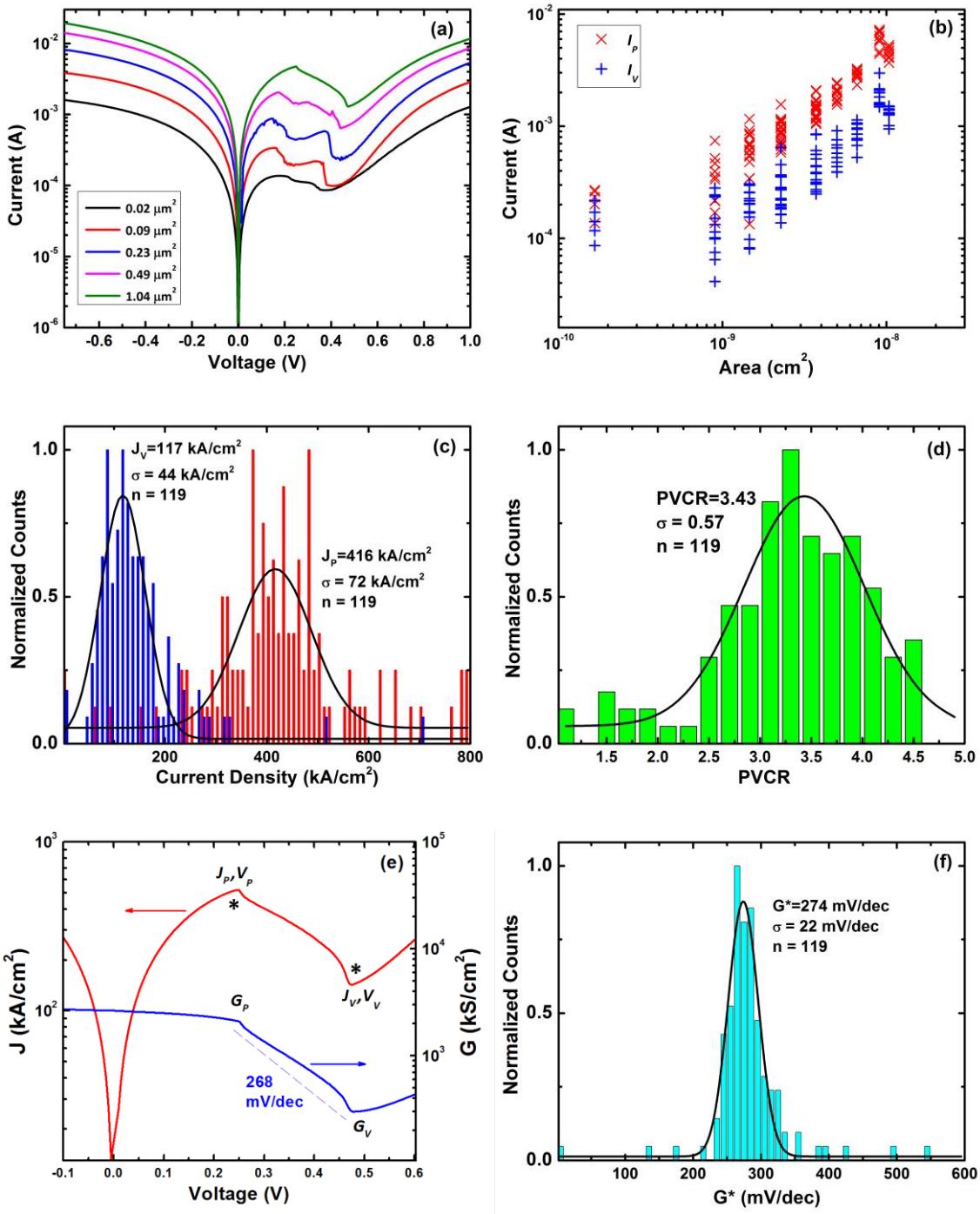

Fig. 42 (a) Representative *I-V* curves for p^+-*i*-n^+ diodes on control sample - TD1 for areas ranging from 0.01 μm^2 to 1 μm^2 showing NDR characteristics at room temperature. (b) The fabricated devices show excellent linear scaling of both peak and valley current with the mesa diode cross-sectional area. Statistical distribution obtained for the (c) peak and valley current densities, and (d) PVCR and Gaussian fit use to determine the mean and standard deviation for a total of n = 119 devices. (e) Representative *I-V* and corresponding *G-V* curve shown along with the extraction of conductance slope in the NDR region. (f) Statistical distribution and Gaussian fit yields a mean value of the conductance slope (*G** = 274 mV/decade) for the control sample TD1.

Sample TD1 shows a clear negative-differential-resistance (NDR) region and the two-steep drops available in the NDR region as result of the instabilities in the testing circuit, and is commonly observed in these types of measurements (Fig. 42a). The conductance slope is analayzed only in the NDR region and taken as an average slope as shown in Fig. 42e. The same analysis is performed for sample TD2 with the broken-gap diodes fabricated on a SI-GaAs using the IMF array technique for the GaAs buffer. Representative values of J_P, J_V, PVCR and G^* were extracted as shown in Fig. 43. The peak and valley carrier densities, and PVCR are considerably lower for this sample as compared to the control sample TD1.

This can be explained in terms of the increased defect density for this integration scheme as shown by the XRD and AFM results in the previous sections. The presence of greater dislocation densities increases the excess current in the Esaki diode that is directly correlated to the valley current density and the number of structural defects in the entire structure. The value of the conductance slope G^* however has improved to 185 mV/decade. This result is contrary to the expected observance of the decrease in the steepness of the conductance slope as a result of increased dislocation density. This anomaly could be explained by incomplete analysis of smaller Esaki diodes which can skew the value of G^* to lower numbers. Additional data needs to be collected to fully understand the reduction of G^*.

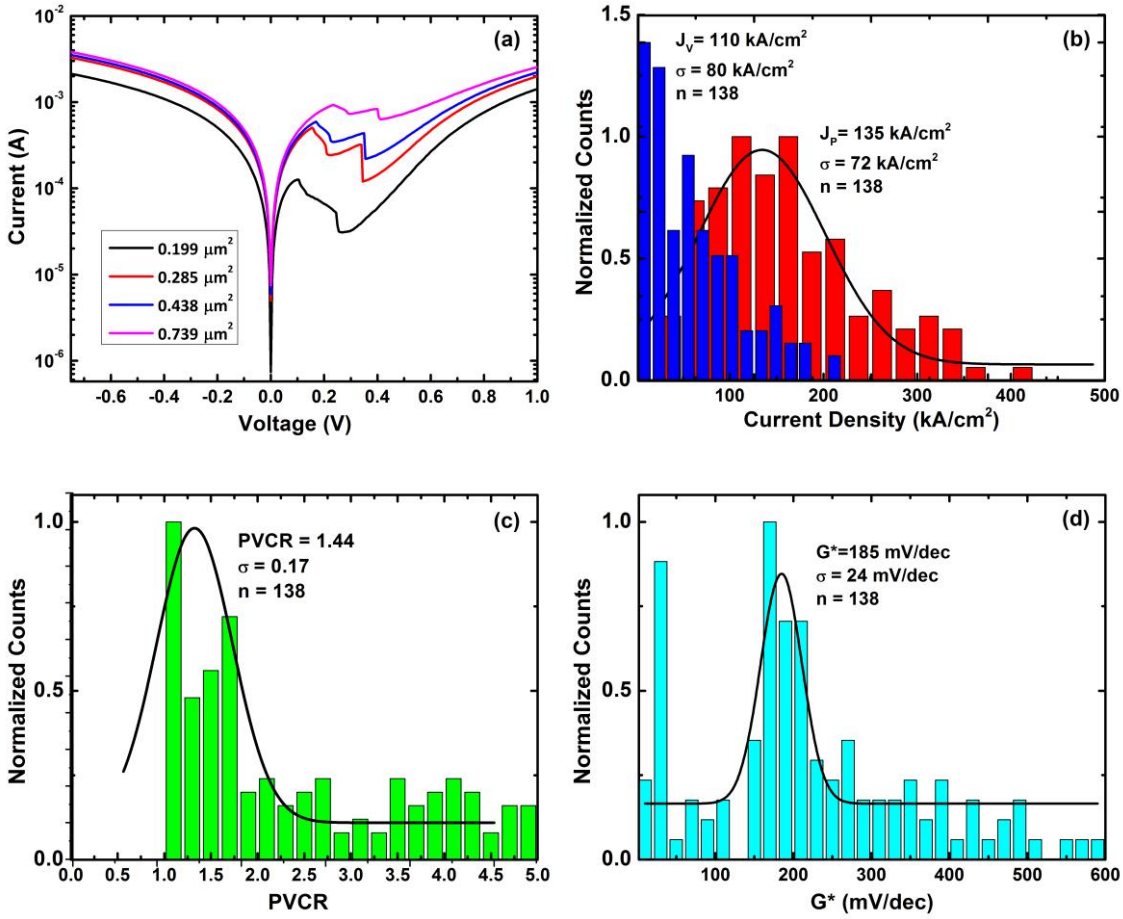

Fig. 43 (a) Representative *I-V* curves for p^+-*i*-n^+ diodes on sample – TD2 for areas ranging from 0.2 μm^2 to 0.73 μm^2 showing NDR characteristics at room temperature. Statistical distribution obtained for the (b) peak and valley current densities, (c) PVCR and (d) *G** and Gaussian fit used to determine the mean and standard deviation for a total of n = 138 devices.

Similar electrical analysis was performed for sample TD3 with the AlSb buffer layer on Si and the representative values of J_P, J_V, PVCR and *G** were extracted (Fig. 44). This sample also shows a low peak and valley current densities and PVCR as compared to the control sample TD1. This effect is traced back to the high dislocation density and surface roughness due to the screw dislocations that create threading segments in the broken-gap diode epi-structure. The structural defects create energy states within the band-gaps leading to trap-assisted tunneling and local band-bending at the interface, which leads to a much higher value of 385 mV/decade for the conductance slope. The presence of both

60^{o} misfit dislocations and 90^{o} pure-edge dislocation in this case results in the less-steep slope for TD3.

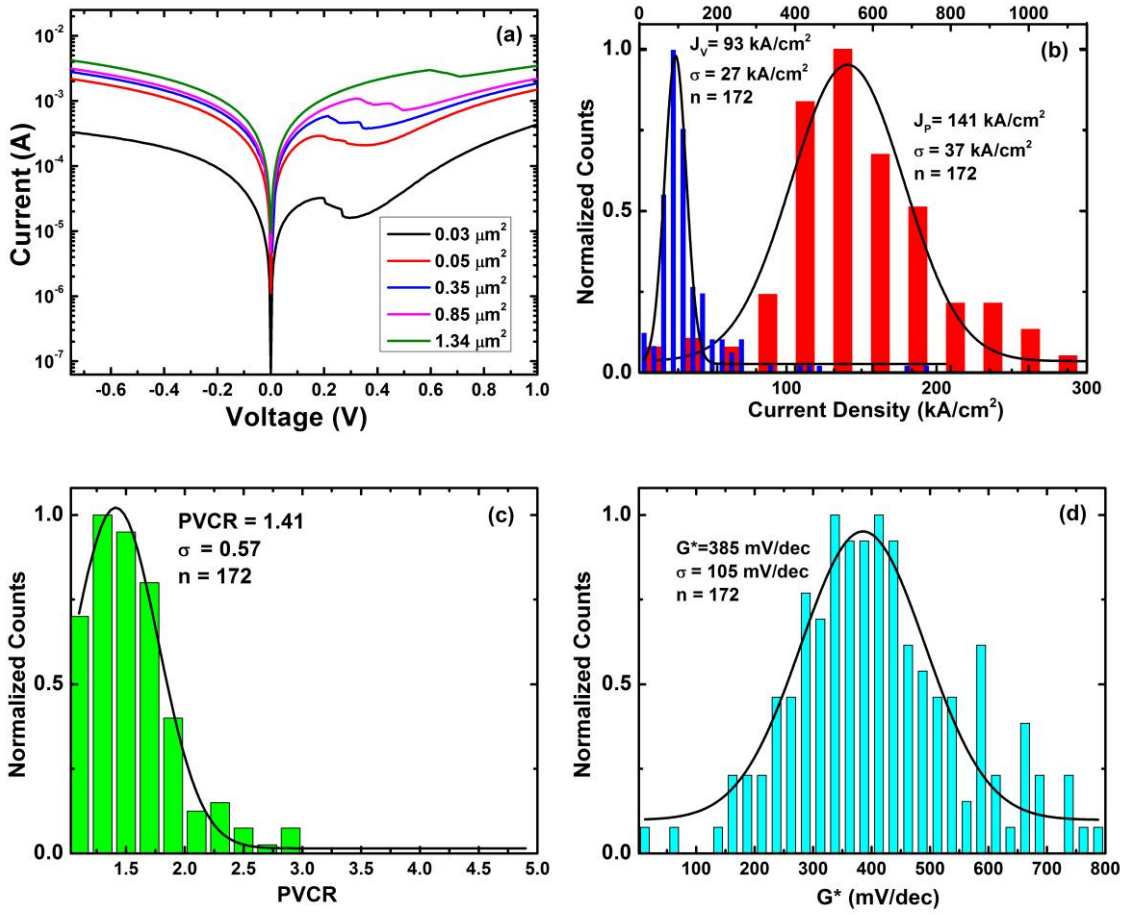

Fig. 44 (a) Representative *I-V* curves for p^{+}-*i*-n^{+} diodes on sample – TD3 for areas ranging from 0.03 μm^2 to 1.34 μm^2 showing NDR characteristics at room temperature. Statistical distribution obtained for the (b) peak and valley current densities, (c) PVCR and (d) *G** and Gaussian fit used to determine the mean and standard deviation for a total of n = 172 devices.

Finally, sample TD4 with the STO/GaAs buffer layer scheme was analyzed using the same procedure and the representative values of J_P, J_V, PVCR and *G** were extracted using statistical analysis (Fig. 45). The use of the STO/GaAs buffer on miscut Si substrates to integrate the broken-gap junction showed much improved results in terms of the peak current densities and the conductance slope. This improved performance and steepness of the conductance slope in comparison to sample TD3 is attributed to the reduced dislocation

density and structural defects observed in TD4 using the XRD analysis and AFM surface morphologies. These results show the benefits of using the STO/GaAs buffer layer scheme developed as a part of this work to create high-quality III-V tunneling devices on a Si substrate. Although the peak current density is still lower than the control sample, the conductance slope analysis suggests that the same level of subthreshold swing can be expected in Tunnel-FETs fabricated on both GaSb and GaAs/STO/Si virtual substrates.

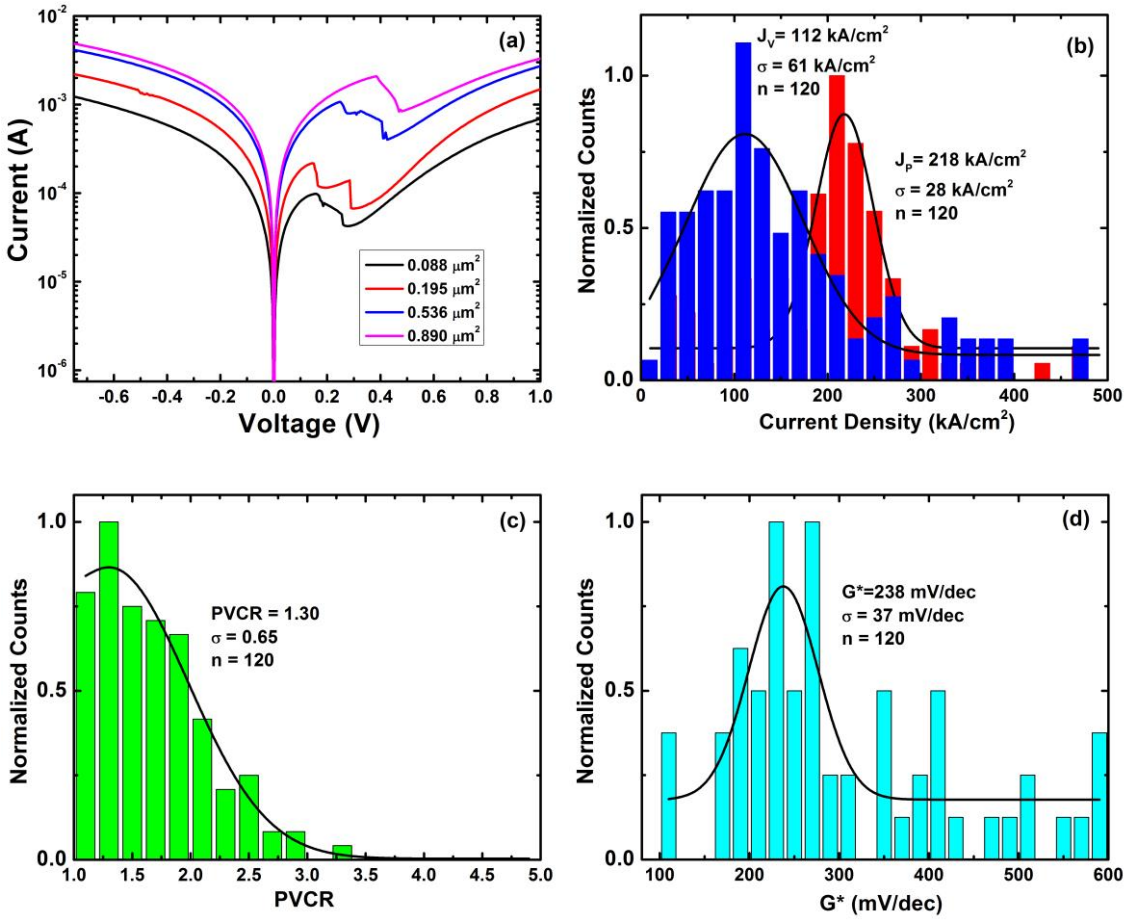

Fig. 45 (a) Representative *I-V* curves for p^+-*i*-n^+ diodes on sample – TD4 for areas ranging from 0.088 μm² to 0.89 μm² showing NDR characteristics at room temperature. Statistical distribution obtained for the (b) peak and valley current densities, (c) PVCR and (d) *G** and Gaussian fit used to determine the mean and standard deviation for a total of n = 120 devices.

Table 4 A comparison of the threading dislocation densities (TDD), RMS surface roughness, J_P, PVCR, and G^* of the GaSb epilayers for all the different samples in this study

Sample	*TDD (cm^{-2})*	*RMS (nm)*	*J_P (kA/cm^2)*	*PVCR*	*G^* (mV/decade)*
TD1	Lattice-matched	0.11	416 ± 72	3.43 ± 0.57	274 ± 22
TD2	3.89×10^8	1.23	135 ± 72	1.44 ± 0.17	185 ± 24
TD3	5.77×10^9	5.74	141 ± 37	1.41 ± 0.57	385 ± 105
TD4	2.27×10^9	2.32	218 ± 28	1.31 ± 0.65	238 ± 37

3.5 Chapter Summary

In this chapter, we successfully demonstrated the high-quality growth of InAs/GaSb broken-gap p^+-i-n^+ heterostructures on different substrate including GaSb, GaAs, and Si using solid-source MBE. The structural properties of the various samples were analyzed using rocking-curve XRD analysis and the surface morphology was measured using AFM and correlated using defect densities. Electrical characterization of the fabricated Esaki tunnel diodes show that the STO/GaAs buffer layer scheme on Si can produce better performing devices as compared to the AlSb buffer layer scheme on Si (Table 4). Although the device performance is still degraded compared to the control sample on GaSb, the conductance slope analysis proves that good quality electrical performance can be expected from InAs/GaSb tunnel junctions on Si substrates, and that certain applications may see acceptable performance despite the defect density from the heterointegration approach.

CHAPTER 4

Quantitative Effect of Uniaxial Strain on Carrier Transport Properties in InAs Channel

4.1 Introduction

Continuous scaling of the conventional planar silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) has continued to improve the performance and cost per unit function of modern integrated circuits (ICs). However, as we move towards advanced technology nodes down to the sub-20 nm gate length, the traditional Si complementary metal-oxide-semiconductor (CMOS) technology suffers from degraded electrical performance due to short-channel effects and a reduced I_{on}/I_{off} ratio [86]. The effective use of strain technology on planar Si CMOS has already been adapted in the 90 nm, 65 nm, and 45 nm technology nodes for logic, communication and consumer applications [87]. Embedded Si-Ge source/drain (S/D) have been adapted successfully to induce high compressive uniaxial strain along the Si channel (due to the larger lattice constant of Si-Ge) to enhance hole mobility and *p*-MOSFET drive currents Re. For *n*-MOSFETs, carbon-doped Si (C: Si) has been used in the S/D scheme to provide uniaxial tensile strain along the channel (due to the smaller lattice constant of C) and boost electron mobility. The strained-Contact etch-stop linear (sCESL) technology that utilizes a nitride layer to induce both tensile and compressive uniaxial strain has also been shown to improve MOSFET performance [88]. The mobility enhancement obtained by applying appropriate uniaxial strain leads to higher carrier velocities in Si channels, resulting in increased drive currents (I_{on}) and reduced supply voltage (V_{DD}) for both *n*- and *p*-MOSFETs [89].

As we approach the limits of the Si CMOS technology, for the first time, ITRS has included the use of III-V compound semiconductors as a potential channel material. With their lower effective carrier masses, III-V semiconductors exhibit much higher carrier velocities and mobilites, leading to increased drive current in III-V MOSFETs [90]. In particular, the III-V material system centered around the 6.1 Å lattice parameter (a_o) with lower band-gaps as compare to Si, is a promising candidate for future ultra-low power CMOS [48]. Therefore, it is important to understand the effects of uniaxial strain on III-V channels for future implementation of strain technology in III-V FETs.

In this chapter, the effect of uniaxial strain on the electron mobility and channel carrier concentration for an InAs channel will be evaluated for application in III-V *n*-channel FETs. InAs is an ideal candidate for future III-V CMOS applications as it possesses a low band-gap (E_g = 0.354 *eV*) and bulk electron mobilites on the order of 30,000 $cm^2/V.s$ at 300K [91]. Section 4.2 describes the theoretical principles behind the effect of strain on band-structure in bulk as well as semiconductor channels. In section 4.3, the experimental design for uniaxial strain and Hall measurements is explored in detail. Section 4.4 presents the results and data analysis for the change in electron mobility and sheet carrier density observed in the InAs channel under the application of <110> uniaxial tensile strain. Section 4.5 summarizes the findings from this work.

4.2 The Physics of Strain Effects in Semiconductors

4.2.1 Strain Effects on Semiconductor Band Structure

Band structure is a direct consequence of crystal symmetry and periodicity of the lattice. The application of strain alters the symmetry of a crystalline semiconductor, and inherently changes the band structure of the semiconductor. Strain which lowers the crystal

symmetry removes band degeneracies and the breaking of symmetry also causes band warping and results in the modification of carrier effective mass.

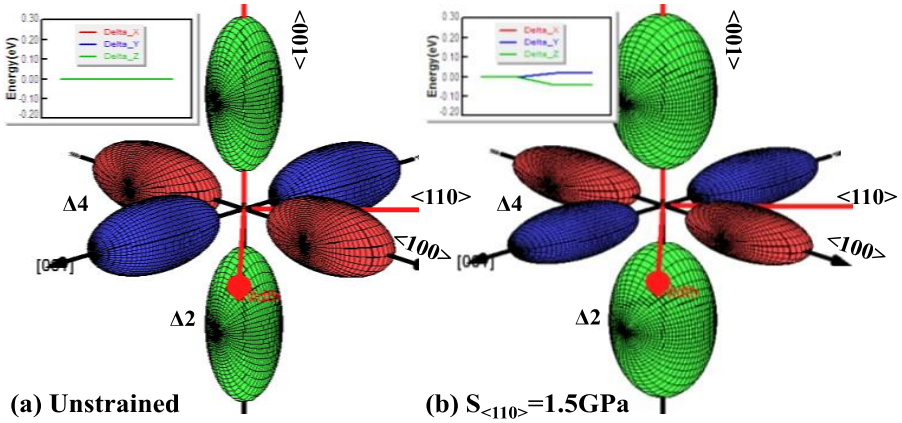

Fig. 46 Silicon band structures showing equi-energy contours for the conduction band electrons under (a) unstrained and (b) 1.5 GPa uniaxial strain in the <110> direction. The inset shows the splitting of the 6-fold degeneracy into Δ_2 and Δ_4 valleys. (*Courtesy: Nuo Xu, PhD, UC Berkley*)

Let us first consider the case of Si, where the conduction band consists of six ellipsoidal-shaped valleys (with two-fold spin degeneracy in each valley) located at Δ-point along the three orthogonal axes in three-dimensional space, as shown in Fig. 46. Therefore, the conduction band (CB) minimum for Si shows six-fold degeneracy. Under in-plane biaxial strain, the crystal symmetry is lowered by reducing the *z*-direction lattice spacing (biaxial tensile strain) or by elongating the *z*-direction lattice spacing (biaxial compressive strain). Due to the difference of the *z* direction with respect to the other two directions, the conduction band minima of Si along the *z* axis splits away from those along the *x* and *y* direction. The six-fold degenerate valleys then split in energy into the Δ_2 and Δ_4 valleys. Therefore, the degeneracy in the CB minima in Si can be lifted through the application of biaxial strain. For the valence band, even though the degeneracy between the heavy-hole (HH) and light-hole (LH) sub-bands is lifted, the band curvature remains unchanged under

biaxial strain. For the application of longitudinal uniaxial strain along the <110> direction, the conduction band splits in to Δ_2 and Δ_4 valleys due to the non-equivalency of the *z*-direction with the *x* and *y* directions. However, the *x* and *y* axes are no longer high symmetry directions as in the case for biaxial strain. The big distinction comes from the band warping which changes both the electron and hole mobility through a change the carrier effective mass [92]. Conduction band warping results from the breaking of the four-fold symmetry in the *x*-*y* plane, with the symmetry now reduced in the two <110> diagonal directions. Under uniaxial strain, the mixing of the HH and LH bands leads to significant band warping in addition to the degeneracy lifting [93].

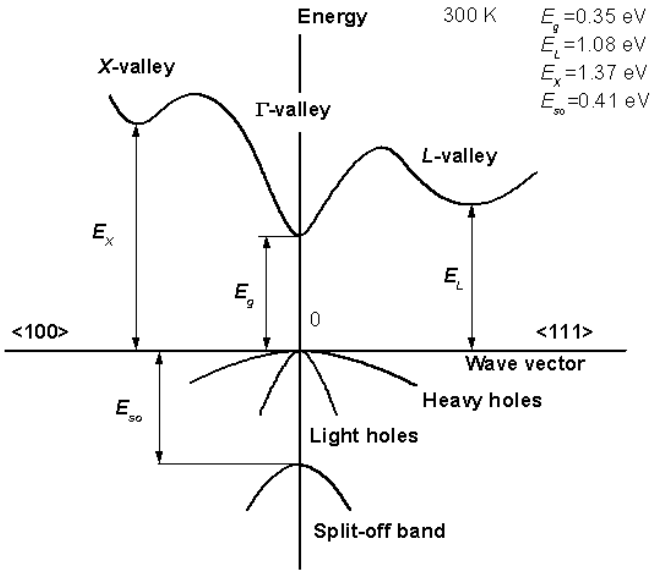

Fig. 47 E-k diagram for InAs depicting the direct band-gap nature at the Γ-point, singly degenerate conduction band edge and HH-LH degeneracy in the valence band. (*Courtesy: IOFFE*)

In the case of direct band-gap III-V semiconductors such as InAs, the conduction band minimum is singly degenerate at the Γ-point and the valence band maxima at the Γ-point have the HH and LH degenerate sub-bands and the split-off band at a lower energy (Fig. 47). The application of in-plane biaxial strain causes a shift in the conduction band-

edge without any band-edge splitting. As in the case of Si, the degeneracy in the HH and LH is lifted upon the application of biaxial strain in InAs [7]. Both the conduction and valence band structures undergo warping from the application of longitudinal uniaxial strain and this induces a change in the carrier effective mass and mobility. For this work, we are concerned with the behavior of electrons under uniaxial strain for applications in *n*-type InAs high-electron mobility field-effect transistors (FETs) and we will explore the change only in the conduction band structure. The tight-binding theory can be used to study the effects of strain on band splitting and band edge shifts in a qualitative way. However, the ***k.p*** method based on perturbation theory provides a much more complete picture of the effects of strain on bandstructure [94].

Previous work has shown the calculation of band structures using 8×8 ***k.p*** simulations for $In_{0.7}Ga_{0.3}As$ <110> channel under uniaxial strain [42]. Constant energy contours for the conduction band in the $In_{0.7}Ga_{0.3}As$ 2D-electron gas (2DEG) are represented in Fig. 48 for both compressive and tensile uniaxial strain. For compressive strain along the III-V <110> channel, the elliptical constant energy contours elongate along the direction of the compressive strain and this decrease in curvature leads to a larger electron effective mass (m_e^*). The energy contours are contracted in the case of tensile uniaxial strain along the <110> channel, which leads to an increase in conduction band curvature and a smaller m_e^*.

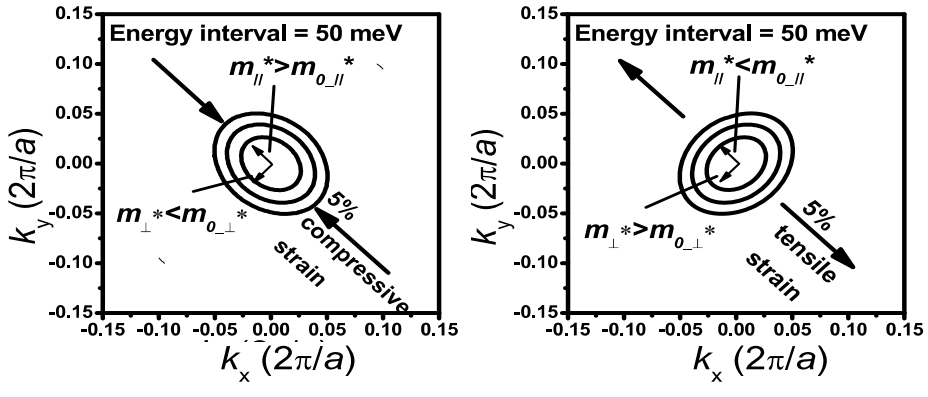

Fig. 48 Constant energy contours on the 2DEG conduction plane of $In_{0.7}Ga_{0.3}As$, under 5% <110> uniaxial compression (left) and tension (right).

Therefore, we can expect electron mobility enhancement in an InAs <110> channel under uniaxial tensile strain from the reduction of m_e^* along the channel direction. From ***k.p*** simulations it has been shown that a pure InAs channel on an InP substrate (which will be inherently under biaxial compressive strain owing to the condition of lattice-matched epitaxy) has the potential to show the same level of m_e^* reduction as in the case of a Si channel. This means that the application of uniaxial strain in InAs *n*-FETs has the potential to reach the same levels of electron mobility enhancement and MOSFET drive currents as in state-of-the-art Si CMOS logic applications.

4.2.2 Electron Scattering under Uniaxial Strain in Semiconductor Channels

According to the Drude model, the low-field carrier mobility is given by:

$$\mu = \frac{q.\tau}{m^*} \qquad (13)$$

where m^* is the carrier effective mass along the current conduction direction, τ is the momentum relaxation time, and q is the charge of the carrier. The main scattering mechanism at room temperature in bulk semiconductors is phonon scattering. The interaction between carriers and phonons (lattice vibrations) causes a change in the position or momentum to induce a time-relaxation process. For electrons, scattering within the same

conduction band valley is called “intra-valley” scattering and is elastic in nature. When electrons are scattered between degenerate conduction band valleys along the same axis, it is known as *g-type* “inter-valley” scattering, which is inelastic in nature and occurs as result of electron-optical phonon interactions. Electrons can also be scattered to other non-degenerate valleys, which is known as *f-type* inter-valley scattering, and are also inelastic in nature.

As discussed before, the application of uniaxial tensile strain in the <110> direction results in the splitting of Δ_2 and Δ_4 valleys and the lifting of degeneracy in Si. This splitting results in electron repopulation in both the valleys, with the Δ_2 valleys getting preferentially populated. This leads to a slight increase in intra-valley scattering, while the strain-induced inter-valley scattering is reduced considerably. This leads to electron mobility enhancement caused by a reduction of conductivity effective mass as well as increased τ by reducing phonon scattering. For III-V semiconductors such as InAs, uniaxial tensile strain in the <110> direction leads to a reduction in the effective mass of the electron and enhances mobility.

For an InAs channel with a 2DEG, this can be understood by looking at the 2D energy contour diagrams, which is directly related to the density of states. To a first order, the value of τ can be determined by the density of states mass (m_{DOS}^*), which depends on band curvature in both parallel and perpendicular to the application of uniaxial strain and the total valley population. Since the Γ-valley in InAs is singly degenerate, no splitting occurs on the application uniaxial tensile strain as in the case of Si. However, the conduction band edge is lowered by the uniaxial strain which has an impact on the proximity of the Fermi level to the CB edge, directly influencing the total carrier

concentration in the InAs 2DEG (Fig. 49a). In addition, the L-valley degeneracy in III-Vs is also lifted, which leads to the reduction in Γ-L energy gap and unfavorable repopulation of the L-valley at high charge density values of ~ 1×10^{13} cm^{-2} (Fig. 49b). The low band curvature in the L-valley increases the electron effective mass and also enhances intra-valley and inter-valley phonon scattering [43]. While this might be the case in GaAs, for InAs the Γ-L separation is much higher and there is not enough repopulation of the L-valley in InAs. An ideal case scenario would involve most of the electron population in the low-mass Γ-valley, which leads to an enhanced mobility and high carrier density from the movement of the Fermi level closer to the conduction band edge.

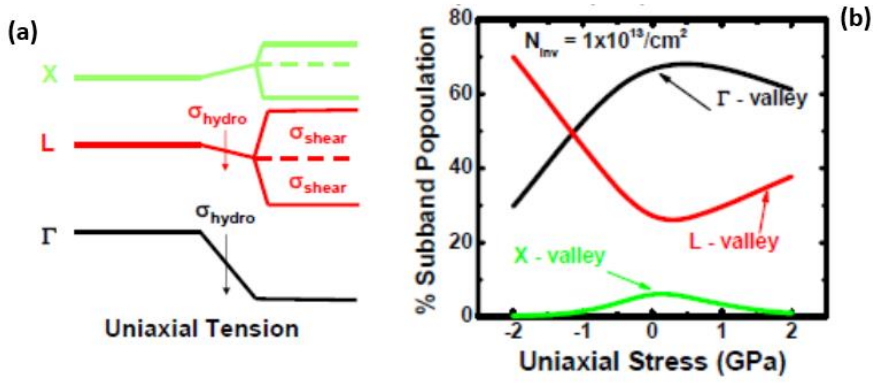

Fig. 49 (a) Schematic showing the valley shift in III-V semiconductors under uniaxial tensile stress. (b) Percentage of sub-band population for different conduction band valleys under uniaxial stress for a carrier density of 1×10^{13} cm^{-2}. [43]

In previous research work, characteristics such as transistor drive current and threshold voltage were monitored as a function of uniaxial strain. These experiments gave a direct measure of the change in mobility without any direct measurement of the 2DEG sheet carrier density. They fail to disentangle the effects of band warping (effective mass and mobility) and carrier concentration (N_s, density of states) upon the application of uniaxial strain [95]. Through novel experimental design and a well-defined measurement

technique, this work aims at a direct analysis of the change in electron mobility and sheet carrier density in the InAs <110> channel under uniaxial tensile strain.

4.3 Experimental Design

4.3.1 Hall Bar Design, Growth & Fabrication

The epitaxial structures in this study were designed to include an InAs channel on InP (001) through the use of lattice matched buffer layers via solid-source MBE. Original experiments were planned around lattice matched quaternary layers of $Al_xIn_{1-x}As_ySb_{1-y}$ lattice matched on low-resistivity InAs and GaSb substrates to create a surface InAs channel [96]. However, initial Hall bar fabrication on these epi-structures revealed undesirable leakage to the conductive substrates leading to very low values of sheet resistance. Therefore, semi-insulating InP was chosen to be the substrate of preference as it provides enough isolation from the active layers of the high-electron mobility transistor (HEMT) structure to avoid effects such as parasitic conduction paths to the substrate, confining the flow of electrons in the InAs channel.

The basic HEMT structures are shown in Fig. 50 where lattice-matched $In_{0.52}Al_{0.48}As$ is grown as a buffer for the growth of $In_{0.53}Ga_{0.47}As$ with an InAs quantum well channel [97]. Two different samples with different δ-doping layers were grown to see the effect of channel carrier concentration on the mobility under <110> uniaxial strain. Sample HB1 had a Si δ-doping layer right below the $In_{0.52}Al_{0.48}As$ barrier with an expected carrier density of 5×10^{12} cm^{-2}. Sample HB2 had Si δ-doping layers both on the top and the bottom of the InAs channel. It should be noted that the HEMT structure inherently has the InAs channel under 3.2% compressive biaxial strain due to the lattice-mismatch. An ideal structure would contain an unstrained InAs channel, but such an epilayer structure

would have to be designed on a semi-insulating InAs substrate, which is not available at this point.

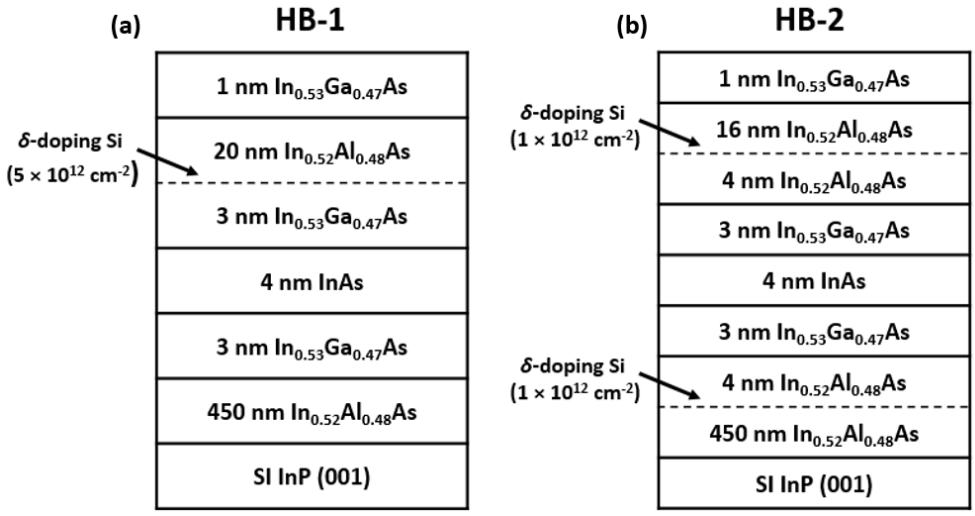

Fig. 50 The two HEMT structures with a top high δ-doping layer (HB1) and bottom and top low δ-doping layers (HB2) grown using lattice-matched epitaxy on semi-insulating InP (001) substrates.

For the epitaxial growth of these structures, InP wafers were first introduced into a load-lock section of an ultra-high vacuum (UHV) where it undergoes an initial baking at 150 ^{o}C for 30 minutes. Then, the substrates were introduced in a III-V MBE growth chamber with In, Ga, and Al effusion cells and As valved cracker. The δ-doping layer was accomplished using Si as an *n*-type dopant to provide carrier density in the InAs-channel. The complete HEMT structure was grown around a substrate temperature of 490 ^{o}C measured using an *in-situ* infrared pyrometer. Each sample went through a similar metrology inspection sequence with double-crystal XRD measurements to ensure lattice-matched epitaxy, AFM scans to ensure low RMS surface roughness, and dark-field microscopy to observe additional surface defects.

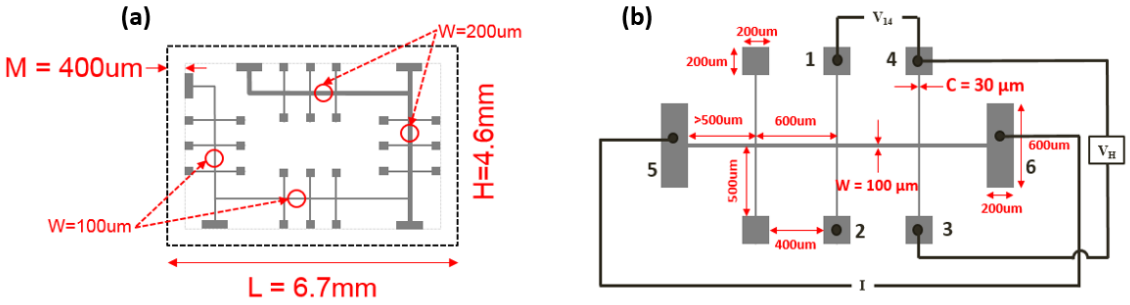

Fig. 51 (a) Single chip Hall bar layout showing 8-terminal devices in both the <110> and <$\bar{1}$10> directions with two different bar widths and lengths. (b) Schematic of a single Hall bar showing the dimensions of the fabricated features and the current and voltage contacts.

Six-terminal hall bars are close to the ideal structures for measuring the transport properties in semiconductor channels [98]. The Hall bar layout was designed to observe the properties of the 4 nm InAs channel in both the <110> and <$\bar{1}$10> directions when uniaxial tensile strain is applied both parallel and perpendicular to these directions (Fig. 51) [99]. Each chip contains 4 Hall bars in 2 different orientation and 2 different bar widths.

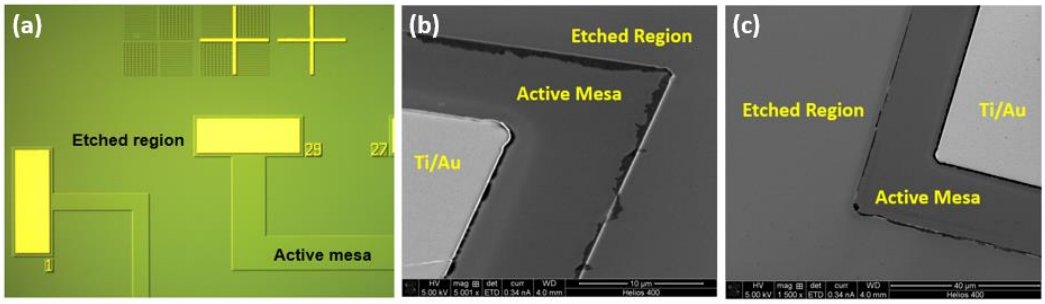

Fig. 52 (a) Optical micrograph of the fabricated Hall bars showing the etched region as well as the active Mesa regions and the Ti/Au top contacts. (b) Scanning electron micrographs taken at a 45° angle for similar areas. (c) Top-view SEM image for the Hall bar.

The fabrication of the Hall bars was carried out using standard photolithography to pattern the Hall bar layout shown above [100]. A RIE dry etch was used to create mesa structures with etch depth around 60 nm to electrically isolate all the different terminals of the Hall bars from each other. Following the mesa formation, a second level litho step was used to create openings in the middle of the Hall bar terminals and a metallization step was

performed via lift-off. The top bonding pads consisted of a 10nm Ti adhesion layer followed by a 100 nm Au layer using thermal evaporation. The contacts were annealed post-fabrication to 300 ^{o}C for 1 minute to diffuse the metal into the InAs channel and form low-resistance ohmic contacts. Fig. 52 shows an SEM image and optical micrograph of the Hall bars for one of the samples with the active mesa and top ohmic contacts visible.

4.3.2 Strain Setup & Modified Hall System

To introduce uniaxial strain in the InAs channel, the InP substrates with the Hall bars were thinned down to 250 μm by grinding the back side (unpolished side) with a grit 40 sanding paper from their original thickness of 500 μm and then mounted on 5mm × 5mm × 9mm piezoelectric actuators, which induce the strain based on the applied voltage. Calibration curves for the measured strain vs. the applied bias voltage were obtained with a strain gage mounted both on the reference side of the piezo as well as on the sample side using an epoxy adhesive (Fig. 53). The epoxy is usually cured for 24 hours at room temperature under static pressure ensuring epoxy thickness uniformity and maximum strain transfer efficiency. An EK strain gage with a resistance of 350 Ω and a foil pattern was used to convert the change in resistance on the application of stress to the corresponding value of strain. This was accomplished by using a data acquisition system based on a Wheatstone bridge configuration that provides extreme sensitivity in resistance on the order of micro ohms. After the initial strain experiments on InP substrates, the InP samples with Hall bars fabricated on them were thinned and mounted on the piezoactuators to assess carrier transport in uniaxially strained InAs channel.

In a Hall bar measurement, terminals 5 and 6 are used to pass current (I) in both directions and the voltage between contacts 1 and 4 (V_{14}) and contacts 2 and 3 (V_{23}) are

measured to calculate the sheet resistance which takes into account the length and width of the Hall bar (Fig. 51b). Under the application of an external magnetic field, the Lorentz force cause the motion of charged carriers, electrons in this case, to move perpendicular to the current direction leading to a Hall voltage at contacts 1 and 2 (V_{12}) and contacts 3 and 4 (V_{34}). The following equations are used to calculate the sheet resistance (R_{sh}) of the 2D channel, the electron mobility (μ_n), and the sheet carrier density (N_s) from the raw voltage measurements:

$$R_{sh} = \frac{1}{2}\left(\frac{V_{14}}{I} + \frac{V_{23}}{I}\right).\frac{W}{L}\ \Omega/\blacksquare \qquad N_s = \left[q.\frac{V_{12}+V_{34}}{2I.B}\right]^{-1}\ cm^{-2} \qquad \mu_n = \frac{\left[\frac{V_{12}+V_{34}}{2I.B}\right]\ cm^2/V.s}{R_{sh}} \quad (14)$$

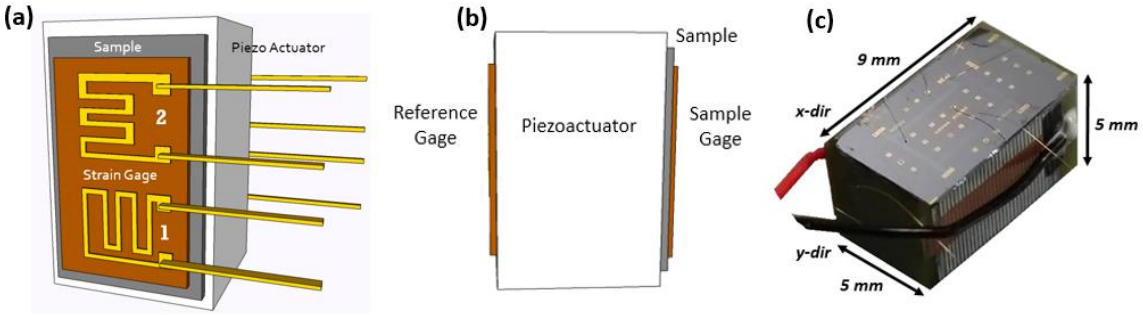

Fig. 53 (a) Schematic showing the strain setup with the piezoactuator and the strain gage mounted using 2-component epoxy. (b) Strain apparatus showing the piezoactuator with the mounted Hall bar chip on the long side.

To test the fabricated structures, the gold contact pads on the Hall bar were wire-bonded to indium connection pads on a glass slide that is connected to a Bio-Rad HL5500PC Hall measurement tool with 6 measurement probes and a fixed magnetic field of B = 0.33 T. The Hall measurement tool was customized to include an ultra-sensitive Keithley 2182A Nanovoltmeter to measure the change in Hall voltage as a function of the applied uniaxial strain. Data acquisition was enabled via GPIB communication with a PCI interface and NI-LabVIEW. Strain was applied on the InAs channel using piezo voltages ranging from 0 V to +150 V with steps of +30V. A wait time of 10-15 minutes was used between each bias point to allow the application of stable strain on the mounted samples.

The carrier transport properties of InAs <110> channel were measured under uniaxial tensile strain for both the up-sweep and the down-sweep to study the hysteresis and its effects.

4.4 Results & Discussion

4.4.1 Strain Calibration Curves for Piezoactuator

The measured strain curves as a function of the piezo bias present little hysteresis and can be seen in Fig. 54 below. Strain has an almost linear dependence on the applied piezo voltage and can be used to determine the amount of strain in both the *x* and *y* directions to separate the two components of strain due to the applied stress from the piezoactuators. For convenience, the *x*-axis is defined along the long side of the piezo and the *y*-axis is the short side. The strain experienced by the 250 μm InP substrate mounted on the sample side is a little less than two-thirds of the maximum achievable strain (0.12%) from the piezoactuator at +150V. This corresponds to approximately 0.07% tensile strain in the *x*-direction (ε_{xx}) and 0.02% compressive strain in the *y*-direction (ε_{yy}). Therefore, we assume that the piezoactuators provides almost uniaxial strain in the *x*-direction as the strain magnitude in the *y*-direction is much layer. For the InP substrate, the maximum strain of 0.07% roughly corresponds to 50 MPa stress when the Young's modulus is taken into consideration.

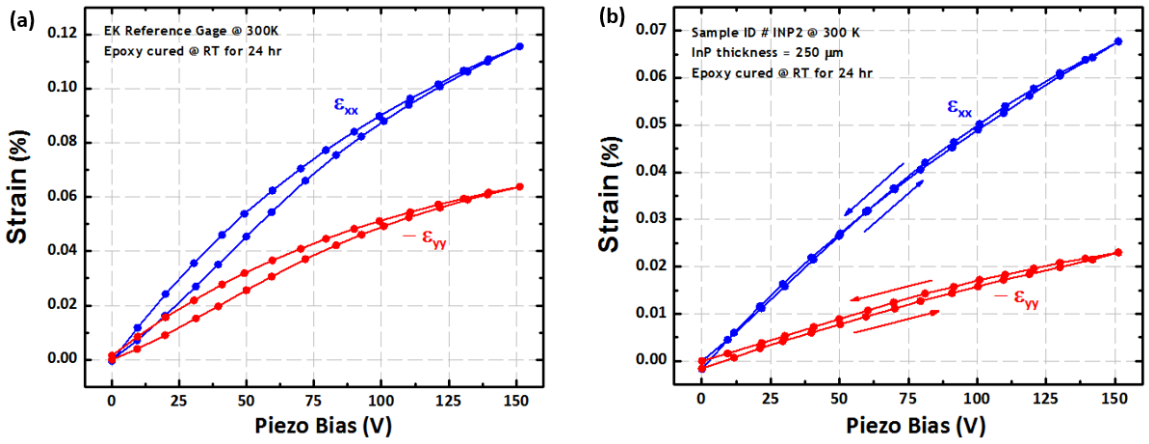

Fig. 54 Calibration curves measured using an EK gage on the (a) reference side and (b) 250 µm InP substrate on the piezoactuator as a function of the applied voltage bias. The maximum achievable strain with this setup is 0.07% corresponding to a uniaxial stress of 50 MPa.

4.4.2 Hall Measurements under Uniaxial Tensile Strain for InAs <110> Channel

4.4.2.1 Top High δ-doping – Sample HB1

The first set of Hall measurements were carried out for sample HB1 with a top δ-doping layer. Initial measurements were made for unstrained samples to establish a baseline. HB1 showed an R_{sh} value of 1670 Ω/square, an electron mobility of 1220 $cm^2/V.s$, and N_s of 3×10^{12} cm^{-2} without any strain application. The measured N_s is lower than the intended sheet carrier density during MBE growth an absolute μ_n of 1220 $cm^2/V.s$ measured for this structure is quite low, which can be attributed to the quality of the epitaxial layers as well as interface scattering in the InAs channel. Interface-roughness scattering can have a significant impact on carrier mobility at room temperature.

The hall bar measured had a width of 200 µm and length of 1200 µm and was aligned parallel to the direction of almost-uniaxial tensile strain (ε_{xx}) in the *x*-direction. Fig. 55 shows the change in sheet resistance (R_{sh}), InAs channel mobility (μ_n) and sheet carrier density (N_s) as the uniaxial strain is increased and decreased by applying voltage on the piezo from 0 V to +150V and then back to 0V in intervals of 30 V with a wait time of 10-

20 minutes. From the strain calibration curves shown above, the voltage bias can be related to the applied uniaxial strain on the HEMT structures.

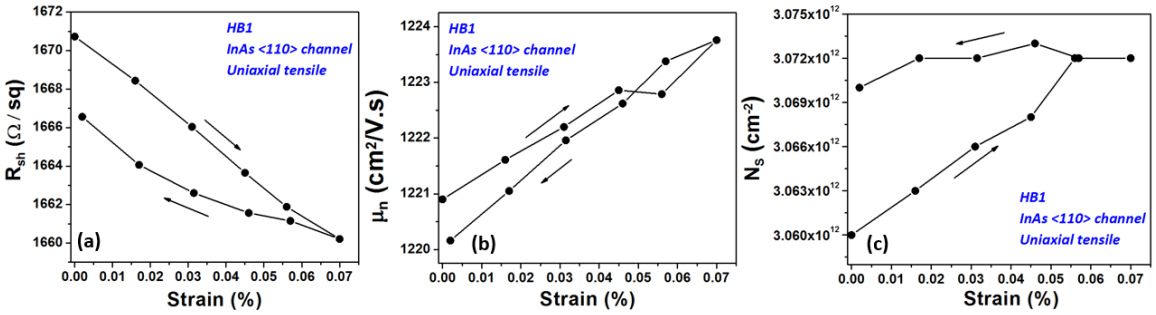

Fig. 55 Hall parameters (R_{sh}, μ_n, and N_s) mapped as a function of increasing and decreasing uniaxial tensile strain along the InAs <110> channel for sample HB1.

Uniaxial tensile strain in the <110> InAs channel reduces the R_{sh} by 0.6% from the original unstrained position at the maximum strain value of 0.07% possible from this strain setup. The value of μ_n in the InAs 2DEG shows a 0.2% increase at the maximum strain and the N_s also increases by 0.4%. The hysteresis observed in these measurements can be attributed to the stability of the epoxy under repeated measurements at room temperature. Since the applied strain depends strongly on the transfer efficiency of the cured epoxy, the difference in values measured between up-sweep and down-sweep of piezo voltage is quite significant. The slight increase in μ_n can be attributed to the change in conduction band curvature and lowering off electron effective mass due to uniaxial tensile strain along the <110> direction. The increase in N_s can be attributed to movement of the conduction band edge towards the Fermi level leading to an increased total carrier density in the InAs <110> channel.

4.4.2.2 Top & Bottom Low δ-doping – Sample HB2

The second set of Hall measurements were carried out for sample HB2 with top and bottom δ-doping layers of equal concentration. Here, both Hall bars with their length

parallel to the <110> direction (*x*-axis) were measured on multiple chips to obtain a statistical dataset and evaluate the change in μ_n and N_s as a function of uniaxial tensile strain. The nomenclature used here for different hall bars on different chips is "C#B#", which refers to the chip number and the bar number for sample HB2. To compare the different hall bars measured, Fig. 56 shows the ratio of the strained to the unstrained values of the three different transport parameters.

In this case, we see a maximum decrease in R_{sh} by 3.5% from the original unstrained value as well as 1.7% increase in N_s and 1.8% increase in the electron channel mobility. On average, sample HB2 shows a higher degree of change in both μ_n and N_s as a function of uniaxial tensile strain on the InAs <110> channel. The table below summarizes the percent change in all the different Hall parameters for both HB1 and HB2 for the maximum applied strain on 0.07%.

In strained Si technology, mobility enhancement is usually evaluated in reference to the uniaxial stress (as opposed to strain). A stress of 1 GPa corresponds to a uniaxial strain of approximately 1.4% for InP.

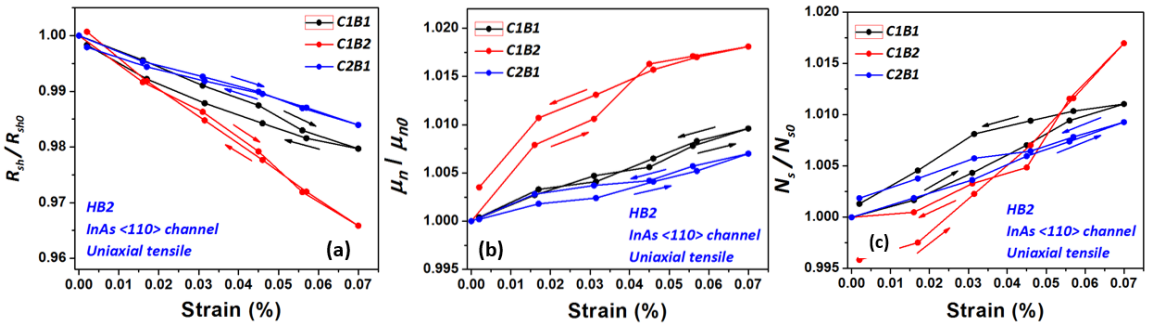

Fig. 56 The ratio of the strained over unstrained Hall parameters shown as a function of strain for three different Hall bars for sample HB2.

Considering HB2 – C1B1 as a representative sample in terms of mobility and carrier density enhancement, a linear extrapolation can be used to assess the performance

of the InAs <110> channel under 1 GPa uniaxial tensile stress. Fig. 12 shows the linear fit for μ_n and N_s which translates to an 18.5% electron mobility enhancement and 23.3% increase in channel carrier density. In comparison to previous work done on HEMT structures composed of $In_{0.7}Ga_{0.3}As$ channel under uniaxial strain, the maximum experimental mobility enhancement was 9.9% per 1% strain as compared to 13.2% per 1% strain in this work. This increase can be attributed to a pure InAs channel where the uniaxial tensile strain in the <110> direction induced conduction band warping leads to further electron effective mass reduction and lower repopulation of the heavier m_e^* L-valley.

Table 5 A summary of the different Hall parameters and the % change for the maximum amount of applied uniaxial strain on the InAs 2DEG via the previously described strain apparatus.

Sample ID	*Width / Length*	R_{sh0} */ % decrease*	μ_{n0} */ % increase*	N_{s0} */ % increase*
HB1	200 / 1200	1670 / 0.6%	1220 / 0.2%	3.06×10^{12} / 0.4%
HB2 – C1B1	100 / 600	3745 / 2.1%	2017 / 0.9%	8.26×10^{11} / 1.1%
HB2 – C1B2	200 / 1200	3546 / 3.5%	2026 / 1.8%	8.69×10^{11} / 1.7%
HB2 – C2B1	200 / 1200	2610 / 1.6%	2967 / 0.7%	8.06×10^{11} / 0.9%

The increase in N_s can be explained by the lowering of the conduction band (CB) edge towards the Fermi level E_F, which is a direct consequence of the lowering of the band-gap under uniaxial tensile strain. Since the corresponding shift of the highest valence band edge E_v is smaller, the band gap variation is therefore dominated by the shift of the CB edge E_c. These results are in good qualitative agreement with the simulation work of Weigele *et al.* using ***k.p*** simulations [101].

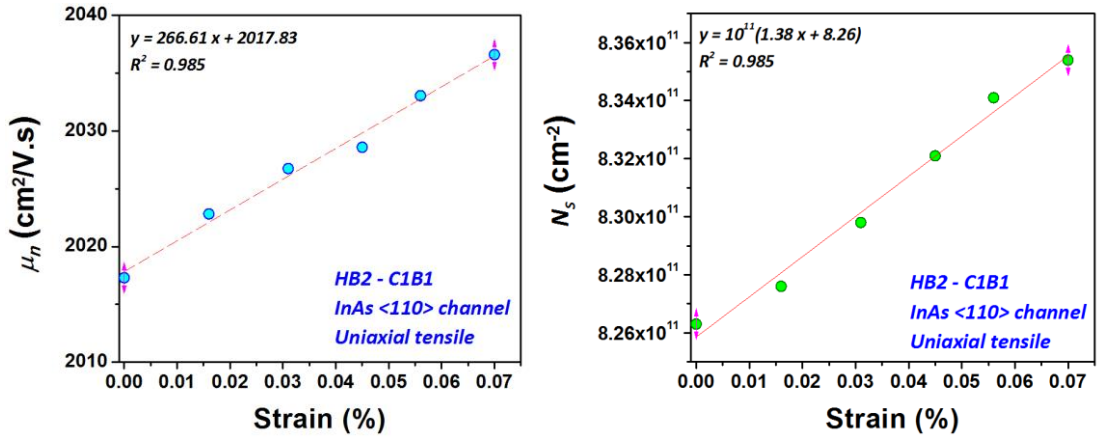

Fig. 57 Linear fit obtained for both electron mobility and sheet carrier density for sample HB2 – C1B1 to extrapolate the mobility enhancement at 1 GPa uniaxial tensile strain.

4.5 Chapter Summary

In this chapter, we successfully investigated the quantitative effects of <110> uniaxial tensile strain on the carrier transport properties in InAs channel. Based on a novel experimental setup using a piezoactuator for uniaxial stress application in conjunction with an ultra-sensitive Hall measurement system, the effects of mobility and carrier density were independently measured. This enabled us to disentangle the effects of both μ_n and N_s simultaneously under uniaxial <110> tensile strain, which is usually hard to accomplish through transfer characteristic (I_D-V_{GS}) measurements. We have shown that a pure InAs channel on an InP substrate can show both electron mobility enhancement via effective mass reduction and sheet carrier density enhancement through closer proximity of the Γ-valley conduction band edge to the Fermi level. This translates directly to high drive currents (I_{on}) for III-V *n*-FETs as both the channel mobility and carrier density can be simultaneously improved by the application of uniaxial tensile strain. These results indicate that strain engineering can be leveraged to improve the transport properties and drivability of InAs *n*-channel FETs.

CHAPTER 5

Conclusion

Since the inception of the integrated circuit, device performance and cost reduction have been attained by continuous miniaturization, modification in device geometries and architectures, and the use of novel materials. However with aggressive scaling, traditional Si CMOS suffers from increased OFF-state leakage current and power dissipation. III-V semiconductors are ideal candidates for replacing the channel in Si CMOS owing to their high electron mobilities and smaller band gaps for low-power solutions. The integration of III-V compound semiconductors with Si can combine the cost advantage and maturity of the Si technology with the superior performance of III-V materials. Therefore, it is important to achieve monolithic integration of commercially relevant III-V semiconductors on Si substrates and show the demonstration of electrical devices on these virtual substrates. Strain technology is another performance booster that has been used in planar bulk CMOS for improving drive currents. However, the use of strain on III-V channels is still being explored for commercial use and a lot can be gained from experimental studies of mechanical strain on low band-gap III-V semiconductor channels. This dissertation aims at investigating the use of III-V heterostructures for post-Si CMOS by their integration on Si substrates as well the use of uniaxial strain on III-V heterostructures for improved transistor performance.

5.1 Contributions of This Work

This work contributes significantly to the following areas: the monolithic integration of III-V semiconductors; GaAs and GaSb on Si using a crystalline oxide buffer layer and solid-source molecular beam epitaxy; the use these virtual substrates for broken-

gap heterojunction Esaki tunnel diodes and their performance evaluation in comparison to control devices on native III-V substrates; and the use of uniaxial tensile strain on an InAs channel for improved electron transport and drive current enhancement.

First, the basics of the integration of GaSb on Si using an AlSb buffer layer and the IMF array dislocation approach were discussed, followed by the use of crystalline $SrTiO_3$ as a buffer layer on Si, for the growth of epitaxial GaAs. The use of a thick AlSb layer grown using the IMF technique produced high-quality GaSb films and the suppression of APDs was confirmed by the use of miscut Si wafers. Different STO surface terminations were assessed for the optimum surface energy to grow epitaxial GaAs, and it was shown that a Sr-terminated surface yields high crystalline quality and the smoothest surface quality. GaSb films were grow using the GaAs/STO/Si virtual substrates and the film quality was optimized in terms of the V/III flux ratio to produce films with RMS roughness as low as 1.2 nm.

Next, the InAs/GaSb p^+-i-n^+ Esaki diodes were grown using MBE on various substrates, viz., GaSb (control), GaAs, $SrTiO_3$/Si, and AlSb/Si. The crystalline quality, surface morphology, and interface quality was assessed using XRD, AFM, and TEM for all the samples. The peak and valley current densities, PVCR, and conductance slope were analyzed from *I-V* measurements on the different tunnel diodes and the performance of the broken-gap tunnel diodes was evaluated in comparison to the control sample on a GaSb substrate. This study shows the potential use of III-V heterostructure tunnel junctions on Si substrates for future applications in Tunnel-FET logic devices.

Last, the quantitative effect of uniaxial strain on the carrier transport properties in an InAs channel was investigated. Using a piezoactuator and strain gage setup, the mechanical uniaxial tensile strain was induced on thinned InP wafers with a strained InAs channel grown using a HEMT structure scheme. Hall measurements show an increase in channel mobility and sheet carrier concentration with tensile strain in the <110> direction. Strain induced conduction band warping leads to effective mass reduction and lower repopulation of the heavier m_e^* L-valley in InAs. The lowering of the CB edge towards the Fermi level E_F increase the electron density of states and leads to an increase in N_s. Transistor drive current in the InAs-based channel transistor can be improved by the simultaneous increase of mobility and carrier density with tensile strain.

The following articles have been published as a result of this PhD work conducted at Texas State University:

1. **K. Bhatnagar**, J.S. Rojas-Ramirez, R. Contreras-Guerrero, M. Caro, R. Droopad "Heterointegration of III-V on Silicon using a Crystalline Oxide Buffer Layer", 2015 *Journal of Crystal Growth*.
2. **K. Bhatnagar**, J.S. Rojas-Ramirez, M. Caro, R. Contreras-Guerrero, B. Henninger, R. Droopad "*In-Situ* Monitoring During MBE Growth of InAs Based Heterostructures", 2015 *Journal of Crystal Growth.*
3. **K. Bhatnagar**, M. Caro, J.S. Rojas-Ramirez, P. M. Thomas, A. Gaur, M.J. Filmer, S. L. Rommel, R. Droopad "Integration of High Current Density InAs/GaSb Esaki Tunnel Diodes on Silicon" 2015 *Applied Physics Letters (Manuscript in preparation)*

4. A. Gaur, I. Manwaring, M.J. Filmer, P. M. Thomas, S. L. Rommel, **K. Bhatnagar**, R. Droopad "Surface treatments to reduce leakage current in $In_{0.53}Ga_{0.47}As$ *p-i-n* diodes", 2015 *Journal of Vacuum Science & Technology B* 33 021210.
5. J.S. Rojas-Ramirez, S. Wang, R. Contreras-Guerrero, M. Caro, **K. Bhatnagar**, M. Holland, R. Oxland, G. Doornbos, M. Passlack, C.H. Diaz, R. Droopad "$Al_xIn_{1-x}As_ySb_{1-y}$ alloys lattice matched to InAs (100) grown by molecular beam epitaxy", 2015 *Journal of Crystal Growth.*
6. A. Gaur, M.J. Filmer, P. M. Thomas**, K. Bhatnagar**, R. Droopad, S. L. Rommel "Fabrication and Characterization of sub-micron $In_{0.53}Ga_{0.47}As$ *p-i-n* diodes", 2015 *Solid State Electronics.*
7. P. M. Thomas, M. J. Filmer, A. Gaur, D. J. Pawlik, B. Romanczyk, S. L. Rommel, K. Majumdar, W. Y. Loh, M. H. Wong, C. Hobbs, **K. Bhatnagar**, R. Contreras-Guerrero, R. Droopad "Performance Evaluation of $In_{0.53}Ga_{0.47}As$ Esaki Tunnel Diodes on Silicon and InP substrates" 2015 *Transaction on Electronic Devices (Manuscript accepted)*
8. P. M. Thomas, M. J. Filmer, A. Gaur, S. L. Rommel, K. Majumdar, W. Y. Loh, C. Hobbs, **K. Bhatnagar**, R. Droopad "Impact of *i*-layer Material on InAs/GaSb Broken Gap Esaki Tunnel Diode Performance" 2015 *Electronic Device Letters (Manuscript submitted)*

5.2 Future Work

Besides the InAs/GaSb broken-gap heterojunction, staggered-gap III-V tunnel junctions have also gained a lot of attention for applications in TFETs for reduced supply voltage and sub- 60-mV/decade operation. The $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ staggered gap

TFET structure can be tailored for both *n*- and *p*-channel TFET and can be grown with abrupt interfaces and composition control using solid-source MBE on (100) InP substrates [29, 73, 75]. Initial results for the growth of staggered gap p^+-i-n^+ have already been obtained showing the growth on InP using a linear-graded $In_xAl_{1-x}As$ buffer layer where the lattice constant is graded from $x = 0.52$ to $x = 0.65$.

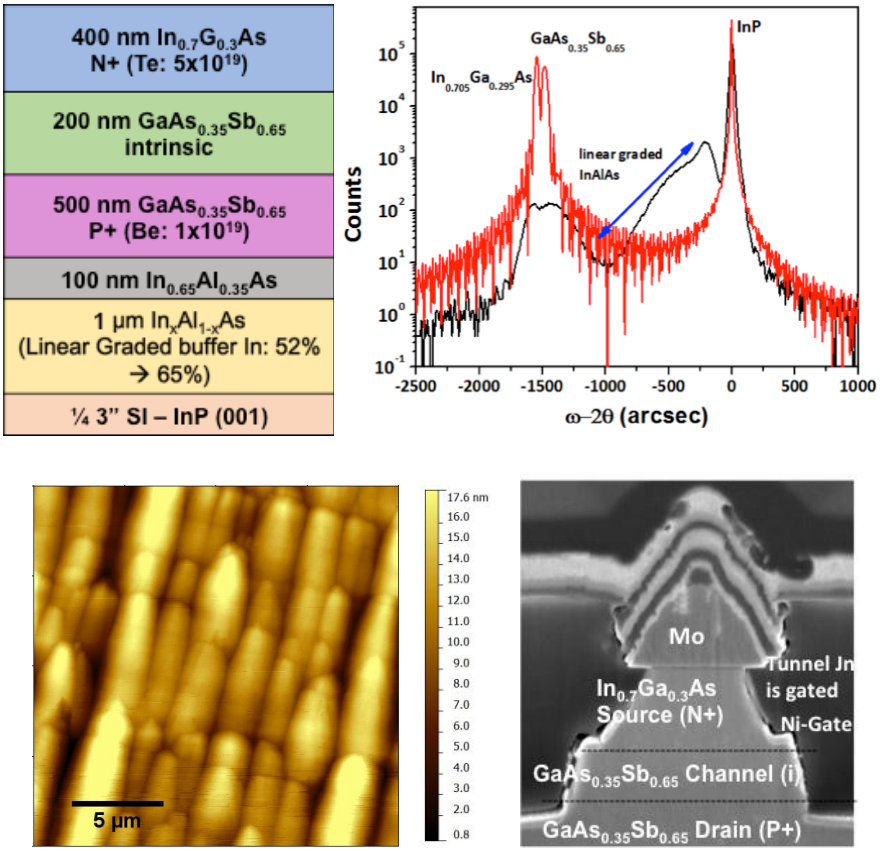

Fig. 58 Schematic for an $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ staggered gap TFET grown using MBE with XRD, AFM, and SEM metrology data.

Surface morphologies show the crosshatch pattern indicative of threading dislocations originating from the relaxation during the heteroepitaxy of lattice-mismatched layers in 2D growth mode (Fig. 58). TFET structures were fabricated at Penn State University using Molybdenum for the top and bottom S/D contacts and sidewall-gate using

ALD grown-Al_2O_3 high-k and Ni gate metal for a vertical *p*-TFET structure as shown in the cross-sectional SEM image. Transfer characteristics of these TFETs will yield important values such as ON-state and OFF-state current since the TFET is a gated reverse-biased Esaki diode, as well as subthreshold swing.

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