INVESTIGATION OF THIN FILM COBALT SILICIDE FORMATION ON THERMAL OXIDE BARRIER LAYERS

THESIS

Presented to the Graduate Council
of Texas State University
in Partial Fulfillment
of the Requirements

For the Degree

Master of SCIENCE

by

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San Marcos, Texas
August 2004

DEDICATION

I would like to dedicate this work to my husband, David Larison, who always stood by me and supported me throughout the years. I will never forget all of the love, patience, and single parent nights that he endured. I will also never forget how understanding, loving, and patient my boys, Tristen and Klay, were. They are the best kids a mom could ask for.

Another part of this dedication must go to my family, especially my parents Dan and Brenda Merkel, who always believed in me. I will always be thankful for being blessed with so many loving people in my life.

Most of all I am thankful to God for every exhausting, inspirational, and unforgettable breath that enabled me to achieve my goals.

Every breath is a gift
Breathe it
Live it
Love it
Thank God for it

ACKNOWLEDGEMENTS

I would like to thank the Texas State University physics professors for always taking the time to answer all of my endless questions. The continuous support I received from the physics faculty throughout the years is greatly appreciated. I would also like to thank Dr. Carlos Gutierrez for his guidance and knowledge that helped me to attain this goal. A special note of gratitude must be given to the people at International SEMATECH for the support, resources, and access to fabrication facilities that made the completion of my research possible. I must also thank the people at J.J Pickle Research campus at UT Austin for the use of their clean room facilities.

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1. INTRODUCTION

1.1. Motivation

The semiconductor roadmap continually guides the semiconductor industry to downsize devices that operate faster and consume less power. The evolution of device reduction has lead to the current development of silicide contacts on top of the polycrystalline silicon gate. Complementary metal oxide (CMOS) devices currently utilized self-aligned silicide (SALICIDE) process to reduce sheet resistance and RC delay, where R is metal wire resistance and C is the interlevel dielectric capacitance. Literature reports a sheet resistivity range from 30-60 Ω/sq for the poly-silicon gate material itself [1]. The addition of a silicide cap has reduced the gate resistance by a factor of 5-20 [2,3]. Co silicide formed on top of the poly-silicon gate is currently implemented into production at the 130nm mode [4]. The further scaling of this silicide/poly-silicon gate material to the 65nm mode is not advantageous due to the interconnect resistance at the gate level. Fully silicided films are excellent candidates for replacing the current silicide/poly-silicon layered gate material in CMOS devices. Silicides have been investigated for several years in support of integrated circuit applications, i.e. silicidation of source/drain and gate materials. For this particular study cobalt has been selected due to its good self-aligning and electrical properties. Cobalt mono- and di-silicides were investigated in detail for their potentiality as a candidate for low resistivity gates with a silicide thickness of 600Å

or less. The majority of research pertaining to Cobalt silicides has been focused on silicidation formed on an infinite source of silicon. The Co di-silicide nucleation phase has repeatedly been investigated due to its low resistivity and its excellent lattice match with Silicon. However, the thin film $CoSi_2$ formation has illustrated severe agglomeration and poor thermal stability. After $CoSi_2$ formed, the higher temperature anneals and/or process steps lead to further silicon consumption, which created a higher resistivity value. To meet the challenges of future CMOS technologies a silicon oxide barrier layer was implemented to form a fully silicided film. Furthermore, the silicon oxide barrier layer was utilized to examine the evolution of cobalt silicide phase formation and develop a thermally stable silicide layer with low sheet resistance.

1.2. Process

Several designs of experiments (DOE) were executed, each a further extension of the previous results obtained. The design of experiment is defined by International SEMATECH to be the "initial planning of engineering experiments in order to minimize cost, reduce experimental errors, and ensure statistical validity of the results". Each DOE included a 100Å thermal oxide isolation layer deposited on the Si substrate to control the amount of silicon consumed during the silicidation process. Various cobalt thickness, 100-250Å, were deposited on a 300-350Å poly-silicon (poly-Si) or amorphous silicon (AMSI) layer and annealed twice at temperatures varying from 350°C - 800°C. The final DOE included a Si implantation step after the 1st anneal. International SEMATECH provided the silicon wafers, deposited the film layers, processed the first anneal and implanted the wafers on all samples investigated. The Second anneal was completed at UT Austin. All the x-ray diffraction analysis scans were performed at Texas State

University. Sheet resistivity measurements and secondary ion beam microscopy analysis were performed at International SEMATECH.

1.3. Goals

The objective of this work was to optimize a cobalt silicide growth that illustrates electrical and crystalline properties, which can replace the basic poly-Si MOS gate, but meet the requirements of future Ultra Large Scale Integrated Circuit (ULSI) technology. These requirements include a decrease in sheet resistivity, narrower linewidths, faster performance, and less power consumption. To obtain a better fundamental understanding of silicides and their phenomena a portion of this thesis is dedicated to the background theory and reports on the properties of metal semiconductor contacts, workfunctions, diffusion, and nucleation of new phases. In chapter 3 a summary of work done by others is given. In chapter 4 the employed instrumentation and analysis methods are discussed. In chapter 5 the data measured on the cobalt silicide samples is presented.

2. SILICIDES

2.1. Periodic Table

Figure 2.1 illustrates all of the silicide elements in the periodic table. Over half of the elements listed react with silicon and forms one and/or multiple silicide phases. However, the silicides from group IVA to group VIII, which are outlined below, have our main focus.

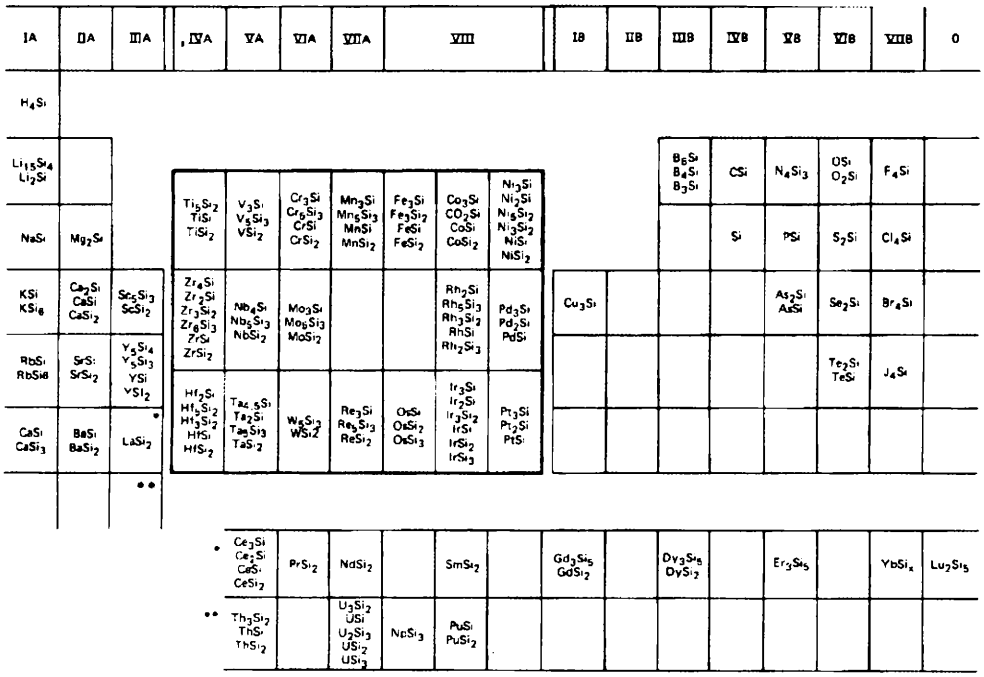

Figure 2.1 - Silicides of elements in the periodic table [5].

Three categories of Silicide include refractory metal silicides, near-noble metal silicides and rare earth metal silicides. The beneficial attributes of each are as follows

Refractory – high thermal stability

Near-noble – low chemical reactivity

Rare earth – optical properties

Silicides in general have a low sheet resistivity; they can be used as stable contacts, and self-passivate in an oxygen rich environment. [5] In CMOS, silicides are utilized for source/drain and gate applications. Cobalt silicides are near-noble metal silicides.

2.2. Schottky Barrier

The Schottky barrier height is the potential barrier for electron flow created by a metal deposited on a semiconductor material. This barrier occurs due to the difference between the work functions of the metal, ϕ_m, and the semiconductor, ϕ_s. When a metal and a semiconductor are brought in contact with each other, their Fermi levels equalize and create a potential charge barrier. Equalization occurs due to the charge transfer between the metal and the semiconductor material. The interacting behavior of the metal/semiconductor structure can be determined by the work function comparison. For example in an n-type semiconductor if $\phi_m > \phi_s$ the contact is rectifying or if $\phi_m < \phi_s$ the contact is ohmic. Since the Schottky barrier height ϕ_B controls the contact properties, a calculation of the barrier height must include the effects of the semiconductor surface states.

The current density J in terms of applied voltage V across a Schottky barrier is given by the expression below:

$$J = A^{*}T^{2}[\exp(-q\phi_B / kT)][\exp(qV / nkT) - 1]$$

$A^{*} \rightarrow Richardson's\ constant$

$T \rightarrow temperature\ in\ Kelvin$

$q \rightarrow electronic\ charge$ Equation 2.1 [1]

$\phi_B \rightarrow Schottky\ barrier\ height$

$k \rightarrow Boltzmann's\ constant$

$n \rightarrow diode\ ideality\ factor$

The value of n and ϕ_B can be determined from the I-V or J-V graph of a forward biased Schottky junction. By plotting ln (J) or ln (I) versus V, N can be determined from the slope and ϕ_B from the intersection with the ln (I) axis [1].

The four different factors that control the barrier height are listed below:

1. The work function of metal, ϕ_m
2. The crystalline structure at the metal-Si interface.
3. The ability of metal atoms that can diffuse past the interface into Si to create traps for electrons or holes. Leading to number 4.
4. The alteration of the electronic properties and the outermost electronic configuration of the metal atoms.

The electrical evaluation of the silicide contact depends on the formation of the Schottky barrier. Table 2.1 illustrates the various Schottky barrier heights of silicides on n-type silicon. In general the silicon-rich silicides have a lower barrier height than the metal-rich silicides. This is the result of the n-type semiconductor work function being less than the metal work function creating the rectifying behavior.

Disilicides	ϕ_B (eV)	Monosilicides	ϕ_B (eV)	Other silicides	ϕ_B (eV)
$CoSi_2$	0.64	CoSi	0.68	Co_2Si	NA
NiSi2	0.7	NiSi	0.7	Ni_2Si	0.7
$TiSi_2$	0.6	PtSi	0.87	Pt_2Si	0.78
$MoSi_2$	0.55	MnSi	0.76	Ir_2Si_3	0.85

Table 2.1- Schottky barrier heights of silicides on n-type silicon [1].

Several researchers have examined the correlation between ϕ_B and other physical and /or chemical properties of the silicide formation. In figure 2.2, Murarka correlated ϕ_B with metal properties by plotting the silicide barrier heights as a function of the metal's location in the periodic table. It was observed that all of the elements listed in periods 4, 5, and 6 all have d-electrons in their outermost orbitals and the value of ϕ_B increases with the number of d-electrons in the metal. The function of the transmission metal d-

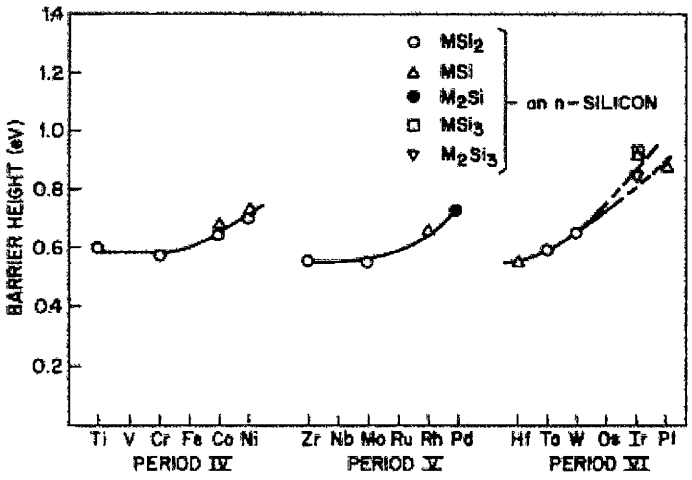

Figure 2.2 – Schottky barrier height as a function of their position of the metal in their periods in the periodic table of elements [5].

electrons during the interaction between the metal d-electrons and the silicon (sp)-electrons in the phase formation sequence was a possible consideration for this

occurrence. Other researchers have illustrated a strong correlation between ϕ_B and the semiconductor heat of formation, ΔH [5]. The higher the heat of formation equates to a higher ionicity. At the metal-semiconductor interface the covalent semiconductor react more readily with the metal, which leads to a decrease in ϕ_B. On the other hand, an ionic semiconductor has a higher heat of formation that facilitates a decrease in the metal reaction. Even though several assessments have been made, the main idea of reducing the barrier height to reduce contact resistance still remains.

2.3. Diffusion

The predominant diffusing species is an important characteristic of the metal-silicide formation. The interaction between the metal-silicide films is critical to understanding the inter-metallic formation. Since cobalt is a near-noble metal, it is the dominant diffuser at temperature range of 200-600°C. At low temperature anneals the phonon energies are not high enough to break the silicon bonds. Interstitial diffusion of the metal atoms causes the silicon bonds to weaken which leads the Si atoms to break

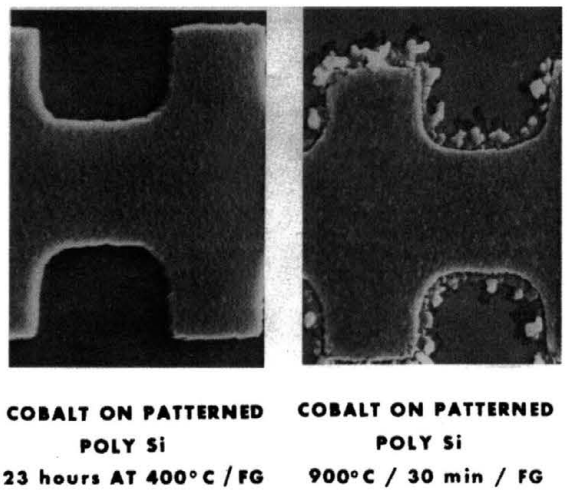

Figure 2.3 – SEM images of cobalt film over patterned poly-silicon and annealed at (a) 400°C for 23h and (b) at 900°C for 30min, in forming gas [1].

away. The Si atoms then diffuse into the vacant metal sites. At high temperatures, above 800°C, the silicon becomes the dominant diffuser since the phonon energy is now

sufficient enough to break the covalent Si bonds. The Si diffuses to the high melting metal film and Si diffusion is enhanced by large concentrations of grain boundaries, structural and point defects in the metal film. This is illustrated in figure 2.3, where the cobalt is deposited on a patterned poly-silicon film layered onto an oxide. The SEM micrograph films illustrate that the Co is the dominant diffusing species at 400°C on the left and Silicon is the dominant diffuser at 900°C on the right. Outside the edge of the patterned poly-silicon, the out-diffusion of the silicon from beneath the cobalt film is observed. Silicon diffusion into the metal is enhanced by structural defects, grain boundaries, and point defects. The coblat silicide phases and their crystalline structures are listed in the table below.

			Lattice Parameters (Å)			Density
Silicide	Structure	Type	a	b	c	g/cm^3
Co_2Si	Othorhombic	$PbCl_2$	4 918	3 737	7.109	7.46
Co_2Si_3	Tetragonal		5 234(3)		8 543(5)	5 736
CoSi	Cubic	FeSi	4.4426			6 582
$CoSi_2$	Cubic	CaF_2	5 365			4.95

Table 2.2 – Cobalt silicide phases

2.4. Diffusion Kinetics

Initially, prior to diffusion, the Si/metal layers are deposited separately and lie in a non-equilibrium state. As heat is applied, the kinetic limitations are decreased whereby diffusion occurs. The energy of the system will naturally decrease in the diffusion process. The free energy of a system as the composition changes is illustrated in figure 2.4. Where M represents the metal compound and Si is the silicon compound. The phases nucleate and multiply when the optimal parameters are employed. To understand

the nucleation process, important aspect of the classical nucleation theory must be examined.

2.5. Nucleation

Nucleation is defined as an initial process of new phase formation. When two solids come into contact with each other, for instance metal **M** and silicon **S**, they interact to become a new phase **MS**. Then a matrix evolves and the system goes from two phases with one interface to three phases with two interfaces, i.e. **M/MS** and **MS/S**. During this process the surface energy increases. In many cases involving metal silicides, several phases can exist at one time. The kinetics of CoSi formation is deemed complex due to superposition of nucleation and diffusion effects [7]. However, in the formation of $CoSi_2$ on amorphous silicon, nucleation ceases to be the rate-controlling mechanism [7]. The rapid heating of samples to high temperatures surpasses the slow nucleation stage in $CoSi_2$ formation. At high temperatures the kinetics of silicide formation becomes diffusion controlled where the driving force for reaction is increased and the nucleation effect is eliminated.

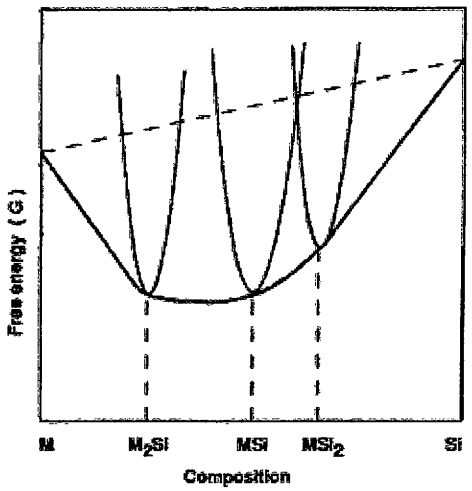

Figure 2.4 - Free energy vs. composition diagram for an M-Si diffusion couple and its inter-metallic compounds [6].

Due to the sequence of cobalt silicide phases, it appears that the phases are controlled by some critical temperature. At the high temperatures and thus high diffusion rates, the reaction expands itself throughout the thickness of the film. The initial phase forms from the metal and silicon layer followed by additional phases that form from the metal layer, silicon layer and other existing phases. Nucleation of a certain phase is generally

characterized by some factor, i.e., abruptness of formation, defects or surface roughness, and a high temperature of reaction where diffusion is not a rate controlling mechanism [7]. The exclusion of diffusion definitely applies to thin films. In general with thicker films the samples nucleation occurs first and is preceded by diffusion-controlled growth. After the initial silicide has formed, the nucleation from an additional phase may result. The initial phase reacts with the remaining silicon and forms another phase that is silicon rich. In all nucleation reactions, the outcome of silicide formation is controlled by the competition between the decrease in free energy and the opposing increase in surface energy.

2.6. Classical Theory of Nucleation

F. M. d' Heurle extensively researched the nucleation phenomenon of phase formation in reference 7. Only some of the aspects of classical nucleation theory are discussed. To understand the nucleation in basic terms, it is easiest to start with the equilibrium between two phases of a specified substance at the melting or evaporation point. A schematic of free energies of the two phases plotted as a function of temperature in figure 2.5 [7]. At the equilibrium point, Tc, the difference in free energy, ΔG, is equal to zero. The relationship is illustrated in equation

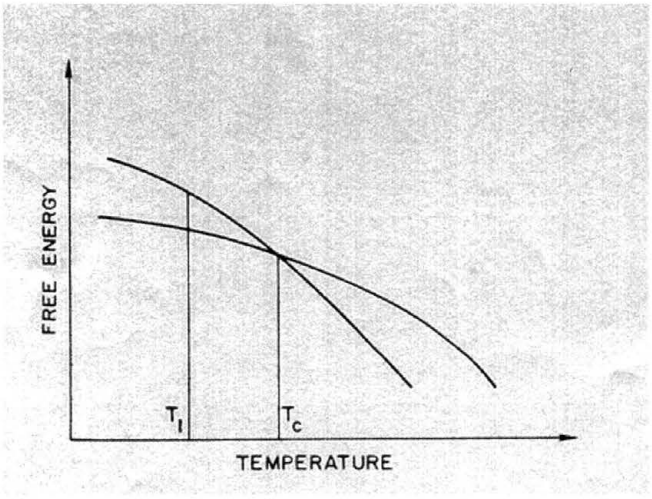

Figure 2.5 – Schematic representation of the free energies of two phases of a single component about a transition temperature [7].

2.2, where the entropy change, ΔS, is the difference in the two slopes in figure 2.5 [7] and where, ΔH, is the enthalpy change of the transition, the heat of melting, or evaporation.

$$\Delta G = \Delta H - T\Delta S$$
$$\Delta S = \Delta H / T_c \quad \text{(Equation 2.2 and Equation 2.3 [7])}$$

At the transition temperature, ΔG is zero, and a driving force does not exist. For any temperature T_1 away from the transition temperature, the transition from one phase to the other is driven by a free-energy change, ΔG_1, whose magnitude is specified by the interval between the two curves in figure 2.5[7] at T_1. If T_1 and T_c are relatively close, the driving force is given by

$$\Delta G_1 = \Delta S(T_1 - T_c) \quad \text{(Equation 2.4 [7])}$$

This decrease in free-energy (equation 2.4) is opposed by an increase of specific surface energy σ. If ΔG_1 is calculated per unit volume, a nucleus of average radius r will have a free energy given by the following equation at T_1.

$$\Delta G = br^2\sigma - ar^3\Delta G_1 \quad \text{(Equation 2.5 [7])}$$

The a and b terms are geometrical factors taking account of the fact that the nucleus is spherical. Hence the coefficient b represents an average of different surface energy values. Figure 2.6[7] illustrates the free energy of a nucleus as a function of its radius r. As shown in figure 2.6 the free energy will be maximized for nuclei with a certain critical thickness size r*. Nuclei larger than r* will be stable and grow while nuclei smaller that r* will be unstable. The free-energy

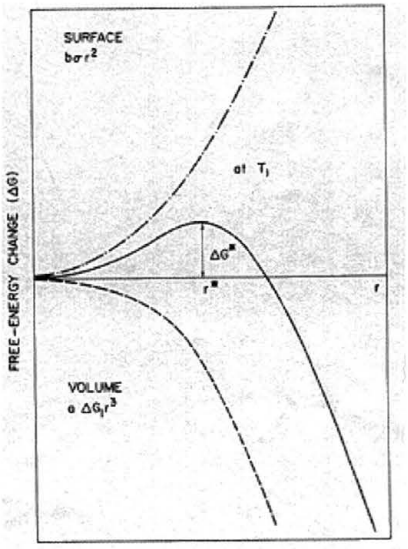

Figure 2.6 – The free energy of a nucleus as a function of its radius, sowing the surface contribution (positive), the volume contribution (negative), and their sum [7].

change ΔG is at a maximum value that corresponds to the critical size radius r* of the nucleus (equation 2.6).

$$r^* = {2b\sigma}/{3a\Delta G_1} \quad \text{(Equation 2.6 [7])}$$

The nuclei smaller than r* exists in an equilibrium distribution and the nuclei larger than r* grow. The free energy of the critical nuclei at any temperature is as follows:

$$\Delta G^* = {4b^3\sigma^3 T_c^2}/{27a^2\Delta H^2 (T - T_c)^2} \quad \text{(Equation 2.7 [7])}$$

Furthermore, the rate of nucleation ρ* is proportional to the concentration of critical nuclei and the rate at which they materialize.

$$\rho^* = K \exp(-\Delta G^* / kT) \exp(-Q / kT) \quad \text{(Equation 2.8 [7])}$$

The exp(-Q/kT) is the diffusion term, Q is the activation energy, and K is the proportionality factor K. Under the energetic conditions that occur during nucleation, it is still estimated that the number of nuclei of critical size will be less by an estimated factor of 2 than the number predicted by thermodynamic equilibrium. This is due to the fact that as the nucleation of the new phase occurs the amount of critical nuclei is continuously being depleted. Furthermore the Zeldovitch factor, which is the correction to the equilibrium equation for nucleation, is typically of order 0.01. This factor measures the probability that the fluctuations in nuclei size, even above the critical size limit, will dissolve if their free energy stays within the kT of ΔG*. Due to the inverse proportionality of ΔG* to T^2, the nucleation rate varies with the diffusion term, exp(-Q/kT) [7]. Calculations involving silicides is not done with sufficient precision, since the free energy is not known [6]. Several nucleation models have been theorized, but they do not match well with experimental observation.

3. RECENT STUDIES

3.1. Cobalt Silicide Formation

The phase formation and sequence of Cobalt silicide film growth is widely discussed in literature. The majority of the cobalt silicide studies consist of a cobalt layer deposited on a Si substrate. Other researchers deposit poly-silicon or amorphous silicon layers on top of bare silicon wafers to aid in the silicidation process. This infinite source of silicon allows for the formation of a cobalt disilicide film.

It has been observed that the crystal phase formation of the silicide layer is dependent of temperature. Several studies illustrate the sequence of phase formation by x-ray diffraction analysis. Through x-ray diffraction

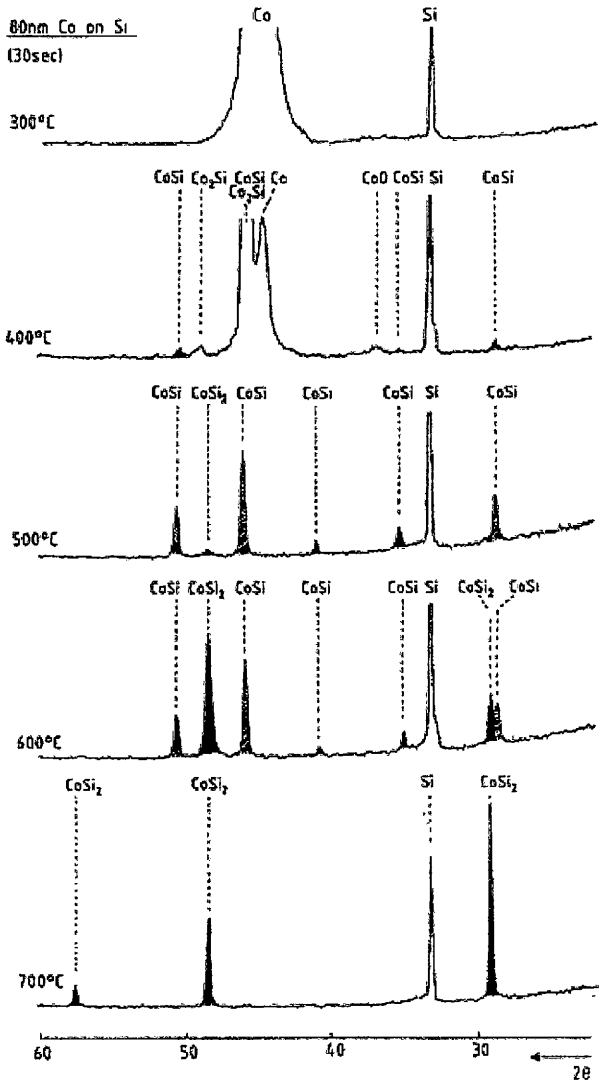

Figure 3.1 – X-ray spectra of 80nm Co on Si after RTP at various temperatures for 30s [6]

spectra, K. Maex shows the sequential formation of cobalt silicides of 800Å cobalt on a silicon substrate that was heated from 300°C to 700°C (Fig. 3.1). The cobalt disilicide phase has the most optimal electrical properties due to its low electrical resistivity. $CoSi_2$ formed by the self-aligned silicide (SALICIDE) process has proven to improve the electrical contact to the gate and junctions due to low resistivity and linewidth independent phase transformation [8]. However, thin films illustrate severe agglomeration and poor thermal stability. It has been reported that anneals, 10 to 30 minutes, greater than 950°C lead to an increase in grain size on wafers with silicidation formation on crystalline silicon. The larger grain size creates a rougher film surface and increases sheet resistance [9]. The high Si consumption during the silicidation process and succeeding high temperature processing steps lead to the thermal instability and high sheet resistivity of the CoSi2. Howell *et al.* also discovered that cobalt silicides formed with the thin polycrystalline Si films had an increase in resistivity after 700°C [9]. A greater degree of agglomeration occurs due to anneal temperatures greater that 700°C, because the textured silicon film enhances the agglomeration effect. In another study where an amorphous Si layer is sputtered sequentially after the cobalt layer, the CoSi2 film became unstable after exposure to 700°C for 60s [10].

The sheet resistance can be correlated to the phase transformations. Each time the silicide reaches a metastable phase the sheet resistance is lowered. The sheet resistivities reported for three of the cobalt silicide phases include Co2Si ≈ 70μΩ cm, CoSi = 100-150μΩ cm, and CoSi2 = 14-17μΩ cm [6].

The downside of Co silicidation is it sensitivity to impurities and preparation of the Si surface. Impurities, mainly 0_2 and H_20, lead to interfacial roughness, higher leakage currents and inhibit cobalt silicidation phase formation, especially the disilicide phase. The interfacial roughness develops differently at each stage of phase formation. The type of formation, diffusion of atoms or reaction process occurring during the phase change, impacts the morphology of the silicide layer. Cabral *et al.* discovered an initial microstructure formed before silicidation began; the Co layer generated abnormal grain growth, which produced considerable lateral non-uniformity [11]. Reports of large interface roughness between the $CoSi_2$/Si (001) layers was attributed to the formation of Si {111} facets, acting as nucleation sites of misoriented CoSi2 grains. The Si{111} facets are easily formed at the initial stage of the silicide reaction [12]. According to Lavoie *et al.*, the different roughness types that develop in each sequential phase formation, adversely affect the subsequent phase formation [3]. An increased amount of roughness occurs due to higher temperature anneals (i.e. 2^{nd} anneal) [3].

Researchers have experimented with several ways to prevent the abnormal grain growth and/or alter the agglomeration of Co silicide films to reduce the final silicide roughness. The use of Ti interlayers, Ti capping layers, oxide-mediated epitaxy (OME) layers and Ti capped OME layers are among the various experimental techniques to avoid abnormal grain growth.

3.2. Titanium Capping and Bilayer

The Titanium interlayer and capping layer have been incorporated into Cobalt silicide research for several years. The Ti interlayer acts as a reaction barrier layer between

the cobalt and Si film. The Ti capping layer functions as a barrier to suppress the cobalt oxidation produced by the oxygen ambient. Several experiments have included the use of both Titanium barriers. It was reported that the Ti capping process reduces any SiO_2 that would be present or would form during the silicidation process [13]. The SiO_2 originates from the trace amounts of O_2 and/or moisture present at the silicidation process. The oxygen atoms can originate from the pre-cobalt deposition process where the hydrogen dangling bonds at the silicon surface have not been passivated and/or the remaining hydrogen has not been removed from the silicon surface prior to the metal deposition process. In an investigation by Kang et al., the Ti interfacial barrier layer was reported to reduce the interfacial roughness of $CoSi_2$/Si substrate (001) by 7Å due to the retardation of the direct contact between the Co and Si substrate [12]. In figure 3.2, the reaction of the Co overlayer and Si substrate is shown to be suppressed by the Ti diffusion barrier until an epitaxial $CoSi_2$ (001) phase nucleated at 660°C. The formation of an epitaxial silicide layer with a coherent interface enabled energetically more favorable conditions to maintain the smoother Si (001) interface [12]. However, the Ti interlayer has also been found to exhibit lateral encroachment and void defects that are generated under the oxide edge. These defects lead to deterioration of the gate and shallow junction. The void

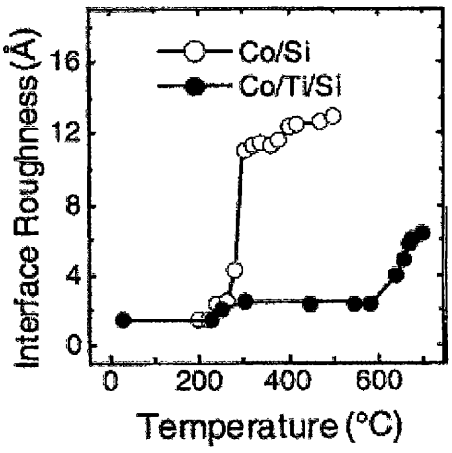

Figure 3.2 - The evolutions of interface roughness of the Co/Si(001) (open circles) and the Co/Ti/Si(001) (filled circle) systems as a function of annealing temperature.

formation is due to the initial Ti-Si reaction [14]. The use of a Ti capping layer has several advantages. The surface diffusion of silicon is reduced and the oxygen ambient contamination during anneal is prevented. Maex et al. illustrated the electrical performance and robustness of the Ti capping process, for sub 0.18 dimensions [13]. Capped Ti films have exhibited a dependence on anneal temperatures. A decrease in anneal temperature leads to a decrease in $CoSi_2$ film thickness, which indicates a large amount of unreacted Co or Ti-Co. The sample annealed at temperatures higher than 600°C increase the sheet resistance value by 25%. This high resistivity is attributed to chemical poisoning by the Ti incorporated during the 1st anneal [12].

3.3. Oxygen Mediated Epitaxy

The oxide-mediated epitaxy (OME) utilizes the Shiraki process to form a protective oxide layer on the Si substrate. The Shiraki process is a 5-8Å passivative oxide layer that is chemically deposited on the silicon substrate [15]. A thin layer, 10-30Å, of cobalt is deposited on the oxide layer and annealed. A single crystalline $CoSi_2$ layer is formed beneath the intact oxide layer [14]. The oxide layer provides a reaction barrier to the Co/Si interface, but is thin enough to allow the formation of a 400-500Å epitaxial $CoSi_2$ layer. However, the formation of the epitaxial $CoSi_2$ layer is dependent on the Co film thickness, which limits the $CoSi_2$ layer to around 110Å in one deposition sequence [14]. The OME process is still sensitive to the oxidation of the Co films. If the cobalt is still exposed to the oxygen ambient, then the epitaxial $CoSi_2$ film exhibits poor quality. M. W. Kleinshind *et al.* performed OME experiments with an insitu anneal to prevent the poor epitaxial quality. However,

insitu deposition and anneal are processes considered to be unsuitable for ultra large-scale integration ULSI applications [16].

The addition of a Titanium cap is also experimentally performed to enhance the OME process by enabling an exsitu anneal process and reducing the oxidation of the cobalt film by ambient oxygen absorption. The Ti capping layer thickness is a large factor in the crystalline structure formed in the $CoSi_2$ phase. For Ti films less than 50Å, the oxidation is non-uniform, with a rough Ti oxide surface morphology. This very rough surface enables the Co film to oxidize and the resulting $CoSi_2$ film was polycrystalline in nature. Ti capping layers thicker than 100Å resulted in a uniform oxide layer, blocking the oxygen atoms and allowing the growth of epitaxial CoSi2. The Ti also functioned as a continuous barrier by transforming the $Si0_2$ interlayer into a $Co_xTi_yO_z$ diffusion membrane [17]. The thickness of the epitaxial $CoSi_2$ layer still remains limited to 110Å in one deposition sequence [14].

3.4. Cobalt Interaction with Thermal Oxide

Thermal oxide was chosen for the research performed, as the barrier layer since cobalt does not react readily with SiO_2. Previous experiments of cobalt deposited on SiO_2 substrates, reported that the Co film did not become discontinuous and agglomerate on the SiO_2 until the temperature reached 736°C [11]. The agglomeration, forming cobalt islands, resulted in a decomposition of the SiO_2 catalyst by the cobalt film. Even though agglomeration occurred on the SiO_2 substrate at this temperature, the Co-SiO_2 interaction was due to the direct contact of Co with the SiO_2 layer. It has also been reported in that the cobalt does not reduce the thermal oxide during the self-aligned silicide (SALICIDE) process [18]. The cobalt

will react with the Silicon layer first before it is able to encounter and react with the thermal oxide.

4. INSTRUMENTATION AND TECHNIQUES

4.1. Design of Experiment Matrix

Initially the designs of experiment (DOE) were based on a density concentration ratio to determine the correct Co:Si ratio to obtain a CoSi and/or CoSi2 film. Table 4.1

Amorphous Silicon								
Film	Thickness Å	Number of atoms	Co:Si 300Å Si	Silicide Phases	Crystalline Formation	Co:Si 350Å Si	Silicide Phases	Crystalline Formation
Cobalt	100	9.10E+16	3:5	NA	amorphous	1:2	$CoSi/CoSi_2$	poly
	150	1.36E+17	1:1	CoSi	mono	4:5	NA	NA
	200	1.82E+17	11:9	CoSi	mono	1:1	NA	NA
	250	2.27E+17	3:2	CoSi	mono	4:3	NA	NA
	300	2.73E+17	11:6	CoSi	mono	11:7	NA	NA
Poly-Crystalline Silicon								
Film	Thickness Å	Number of atoms	Co:Si 300Å Si	Silicide Phases	Crystalline Formation	Co:Si 350Å Si	Silicide Phases	Crystalline Formation
Cobalt	100	9.10E+16	3:5	NA	NA	1:2	$CoSi/CoSi_2$	poly & mono
	150	1.36E+17	1:1	NA	NA	4:5	CoSi	mono
	200	1.82E+17	11:9	CoSi	mono	1:1	CoSi	mono
	250	2.27E+17	3:2	CoSi	mono	4:3	NA	NA
	300	2.73E+17	11:6	CoSi	mono	11:7	NA	NA

Table 4.1 – Calculated number of atoms per cm^2 area and Co:Si ratios of various cobalt thickness deposited on top of 300Å and 350Å of AMSI and PolySi films.

illustrates a calculated number of atoms per cm^2 area for the different cobalt and silicon thicknesses used in the various experiments. The calculated number of atoms per cm^2 for a 300Å and 350Å silicon thick film is 1.48E+17 atoms/cm^2 and 1.72E+17 atoms/cm^2 respectively. The Co:Si atomic ratios for the 300Å and 350Å silicon deposition are listed. The table also lists the silicide phases and crystalline structures that formed as a result of

the Co:Si ratios. The experiments performed included four DOE matrices. Each Matrix is illustrated in the following tables. All experiments utilized a 100Å thermal oxide barrier layer and a cobalt deposition temperature of 350°C. The samples were exposed to oxygen ambient before and after both anneal steps. The dimension of each wafer listed in the matrices is 200mm. The matrices describing the subsequent process steps do not include the 2nd anneal step. After the wafers were processed through a 1st anneal and chemical cobalt strip, they were cleaved into 3cm square samples. The samples were then processed through a 2nd anneal in a rapid thermal process (RTP) tool at a separate location. The basic motivation behind the experiments and the parameters of the second anneal are explained in each DOE.

4.1.1. 1st DOE – Lot # 3092614

Wafer #	1	2	3	4	5	6	7	8	9	10	11	12		14	15	16	17	18	19	20	21	22	23	24	25
50A HF RCA 1&2	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x
100A Thermal Oxide	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x
300A Amorphous Si	x	x	x	x	x	x	x	x	x	x	x	x													
300A Poly-Si														x	x	x	x	x	x	x	x	x	x	x	x
50A HF only	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x
100A Cobalt	x	x	x	x										x	x	x	x								
150A Cobalt					x	x	x	x										x	x	x	x				
200A Cobalt									x	x	x	x										x	x	x	x
Co Si RTA, 650, 60sec,N2	x				x				x					x				x				x			
Co Si RTA, 700, 60sec,N2		x				x				x					x				x				x		
Co Si RTA, 750, 60sec,N2			x				x				x					x				x				x	
Co Si RTA, 800, 60sec,N2				x				x				x					x				x				x
Co Strip	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x

Table 4.2 – 1st Design of Experiment

Table 4.2 illustrates the design of experiment for all process steps completed on lot #3092614. The initial cobalt silicide investigation examined the crystalline phase formation of the cobalt silicidation process. The first twelve wafers are

processed with amorphous silicon and the remaining twelve wafers with poly-crystalline silicon. Different Co thicknesses were deposited onto the silicon to observe the resultant phase(s) and crystalline nature of the cobalt silicide films. A two step annealing process was carried out utilizing various temperatures. The cobalt silicide phase sequence on an infinite source of silicon is highly dependent on the application of a two step anneal process. The mono-silicide is formed in the initial anneal step, the remaining cobalt is etched, and the second anneal step forms di-silicide forms[4]. A portion of this experiment is to determine the effects of different first and second anneal temperatures of the Co silicidation process that forms on top of an oxide barrier layer. Due to subsequent high temperature process steps in IC manufacturing, it is also important to determine the thermal stability of silicidation formation. Each wafer in lot #3092614 was processed through a second anneal step carried out by cleaving each wafer into four sections and annealing at process temperatures of 650°C, 700°C, 750°C, and 800°C.

4.1.2. 2nd DOE – Lot # 3092615

Wafer #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
50A HF RCA 1&2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
100A Thermal Oxide	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
300A Amorphous Si	x	x	x	x	x	x							x	x	x	x				
300A Poly-Si							x	x	x	x	x	x					x	x	x	x
50A HF only	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
200A Cobalt	x	x					x	x												
250A Cobalt			x	x					x	x			x	x			x	x		
300A Cobalt					x	x					x	x			x	x			x	x
Co Si RTA, 450, 60sec,N2	x		x		x		x		x		x									
Co Si RTA, 550, 60sec,N2		x		x		x		x		x		x								
Co Si RTA, 650, 60sec,N2													x		x		x		x	
Co Si RTA, 750, 60sec,N2														x		x		x		x
Co Strip - 300A	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Table 4.3 – 2nd Design of Experiment

Table 4.3 illustrates the design of experiment matrix for lot # 3092615. With this particular lot the influence of a thicker cobalt film and lower annealing temperatures was investigated. The main objective was to alter the crystalline phase formation and sheet resistivity with the thicker cobalt film deposition of 250Å and 300Å. The 200Å cobalt film, which illustrated the largest cobalt silicide monocrystalline formation was also annealed at lower temperatures to correlate anneal temperatures and silicide phase formation. Ten of the wafers were processed with amorphous silicon and the remaining ten with polycrystalline silicon. Additionally every wafer in lot #3092615 was processed through a second anneal step at another location. Four sections of each wafer listed, 1-10, were cleaved and annealed at process temperatures of 450°C, 550°C, 650°C, and 750°C.

4.1.3. 3rd DOE – Lot #3092616

Wafer #	1	2	3	4	5	6	7	8	9	10
50A HF RCA 1&2	x	x	x	x	x	x	x	x	x	x
100A Thermal Oxide	x	x	x	x	x	x	x	x	x	x
350A Amorphous Si	x	x			x	x	x			
350A Poly-Si			x	x				x	x	x
50A HF only	x	x	x	x	x	x	x	x	x	x
100A Cobalt	x	x	x	x	x	x	x	x	x	x
Co dep. - 350C/no anneal	x		x							
Co dep. - 250C/no anneal		x		x						
Co Si RTA, 350, 60sec,N1					x			x		
Co Si RTA, 450, 60sec,N2						x			x	
Co Si RTA, 550, 60sec,N2							x			x
Co Strip - 300A					x	x	x	x	x	x

Table 4.4 – 3rd Design of Experiment

Table 4.4 shows the process steps for the third design of experiment for lot # 3092616. Since the lowest sheet resistivity values were attained with a Co:Si ratio of 1:3.5 respectively the objective of the 3rd DOE was to investigate this

phenomenon further. The first four wafers processed investigated the initial silicide formation due to the cobalt deposition step. Cobalt deposition of 100Å on underlying amorphous and polycrystalline silicon films were both examined. The six remaining wafers were processed with 100Å of cobalt on three AMSI and three PolySi films, both 350Å thick. Since the 1st DOE used a high temperature 1st anneal, the first anneal temperatures of this DOE were set lower at 350°C, 450°C, and 550°C. In the second anneal step, three sections of each wafer listed, 19-24, were cleaved and annealed at three different process temperatures of 600°C, 700°C, and 800°C.

4.1.4. 4th DOE – Lot #3092616C

Wafer #	19	20	21	22	23	24
50A HF RCA 1&2	x	x	x	x	x	x
100A Thermal Oxide	x	x	x	x	x	x
300-350A Poly-Si	x	x	x	x	x	x
50A HF only	x	x	x	x	x	x
100A Cobalt	x	x	x	x	x	x
Co Si RTA, 550, 60sec,N2	x	x	x			
Co Si RTA, 650, 60sec,N2				x	x	x
Co Strip - 300A	x	x	x	x	x	x
IMP05-Si, 1E15 at 200eV	x			x		
IMP05-Si, 1E15 at 300eV		x			x	
IMP05-Si, 1E15 at 400eV			x			x

Table 4.5 – 4th Design of Experiment

The main objective of this DOE was to transform the initially formed CoSi/$CoSi_2$ mixture into a fully cobalt disilicide phase. To achieve this transformation a Si ion implantation was utilized after the 1st anneal and cobalt etch step. From the previous experiments the process parameters of CoSi/$CoSi_2$ mixture formed with the lowest sheet resistivity was chosen for implantation. The first anneal

temperatures of 550°C and 650°C were applied to six polycrystalline silicon wafers, 350Å thick. The deposited cobalt film thickness remained 100Å. Each set of AMSI and PolySi wafers were implanted at low energies, 200eV, 300eV, and 400eV, with a Si dose of $1x10^{15}$ ions/cm^2. The ion dose is much less than the number of silicon calculated at 1.72E+17 atoms/cm^2 for a 350Å silicon thick film. Therefore, rather than incorporating more Si atoms into the cobalt silicide film, it is more likely that the ionization will alter the crystalline structure of the film to allow further migration of the atoms during the second anneal. After Si ion implantation, each wafer was cleaved into three sections and annealed at three process temperatures of 600°C, 700°C, and 800°C.

4.2. CoSi Deposition Process

Lightly boron doped silicon substrates are utilized in all of the samples. A 100Å thermal oxide, which provided a stopping layer for the silicidation process, was deposited by furnace. The design of experiment was set up to process the Co silicide wafers as presented in the following steps.

To ensure a clean interface between deposited layers, several cleans were performed throughout the separate deposition and anneal process steps. The initial clean was a pre-thermal oxidation deposition etch with the following chemistry:

Title: SPM, HF 50A, RCA
Chemicals: H2SO4:H2O2 (10:1)
HF (15:1)
SC1 = NH4OH:H2O2:H2O (0.5:1:5)
SC2 = HCl:H2O2:H2O (0.6:1:5)

Next the thermal oxide was grown on the Si substrate in a vertical gate oxide furnace as follows:

100 Gate- OxTemp 900 C
Oxidation time:15:28
O2 sccm:9980 sccm
DCE sccm: 123 sccm
Anneal Time:34:58
N2: 10 SLM

The poly-Si or AMSI layers were deposited by a vertical hotwall thermal reactor that utilized low pressure chemical vapor deposition (CVD). The deposition process is listed as follows:

300A AMSI @ 530C
Deposition time: 20:36
SiH4 top of tube:100 sccm
SiH4 bottom of tube: 110 sccm
380 milli-Torr process control
300A Poly @ 600C
Deposition time: 7:40 (recipe still not maximized)
SiH4 top of tube:100 sccm
SiH4 bottom of tube: 100 sccm
110 milli-Torr process control

A pre-metal clean was performed to remove any native oxide prior to metal deposition. The HF clean is known to passivate the Si surface, which leaves an oxide free interface between the deposited metal and the furnace grown silicon. The short queue time ensures that the Si surface remains oxygen free prior to cobalt deposition.

HF/50A - 50A thermal oxide etch with HF only and rinse/dry.
With a time queue of 15 minutes between clean and Co dep.

Cobalt was then deposited with a Varian M2000/8 Sputtering System, with a cobalt layer thickness ranging from 100-300Å. Sputtering is usually the preferred deposition process due to its controllability. The dangling hydrogen bonds were removed by a five minute pre-heat at 300°C. The deposition process is listed as follows:

Chamber A4-Heater Temp 300 C
Heater + Dev= 100C

Heater - Dev=100 C
Base Pressure= 5e-2 Torr
Ar flow= 55
Ar +/- dev=5.0
Dep power= 6
Pre heat=5
Ramp time= 50.0
Min Pressure=0/Max pressure=20

After Co deposition the 1st anneal, 450°C-800°C temperature range ,is processed in a rapid thermal anneal (RTA) tool for 60 seconds. The RTA tool utilized a ramp rate of 60°C/s and an N_2 inert gas flow that purged at 20 litters per minute for 3 seconds. The low temperature anneal of 350°C was annealed in the Varian sputtering Tool for 60 seconds. The excess cobalt was striped of with a wet etch with the following chemistry.

Wet etch= H3PO4 (2):H202 (3):H2O (4) @ 80C for 300 seconds.

Finally, pieces were cleaved off of each wafer to perform the subsequent second anneal with temperatures ranging from 450°C to 800°C for 60 seconds. An AG Associates Heatpulse Model 610 rapid thermal annealer (RTP), with a ramp rate of 40°C/s, was utilized for all second anneals. RTP processing is an effective means of annealing the sample while only subjecting the sample to a short term thermal process .Prior to anneal the RTP chamber is purged with an N_2 inert atmosphere for 5 minutes. The heat source utilized in the AG Associates tool was tungsten halogen lamps that emitted radiant light to anneal the samples for 60 seconds. This type of anneal allowed rapid and uniform heating and cooling of the sample. Inert N_2 atmosphere also flowed through the chamber post-anneal to aid in the process of cooling the sample. The tool specifications were as follows

ANNEAL @ 450C-800C
Preheat = 300C
Purge time: 05:00min

Ramp time: 40C/s
Deposition time: 00:60s
N2 flow: 5 sccm
Cool: 05:00min

The ion implantation process that was implemented in the 4th DOE after the first anneals. Energetic silicon ions were used to implant the polycrystalline cobalt silicide layer to increase the amount of silicon available to the silicidation process. During the implantation process ions move through the film and transfer energy by collisions with the target nuclei and Coulombic interaction with the electrons of the target film. These interactions lead to a continual loss of energy until the ions stop. Low acceleration energies were used due to the thin (@ 400Å) silicided layer. The Si implant process consisted of the following parameters:

All implants are in 100% Ar ambient.
Tilt and twist angle were set to zero due to the low energy of the Si implantation
Three different Si implant splits:

1. 2KeV->200eV 1E15 ions/cm^2
2. 2KeV->300eV 1E15 ions/cm^2
3. 2KeV->400eV 1E15 ions/cm^2

4.3. Analysis Tools

Bede D1 XRD analysis tool at Texas State University characterized the different peaks that corresponded to the Co silicide phases and the crystalline structure of the silicided layer. High angle x-ray diffraction (HAXRD) and parallel beam x-ray diffraction (PBXRD) were the two types of x-ray analysis utilized for this verification. Sheet resistivity data was obtained with a Prometrix Omnimap RS55/tc tool at International SEMATECH. Cross-section and plan-view Scanning electron microscope (SEM) analysis was performed at International SEMATECH.

4.3.1. High Angle X-Ray Diffraction (HAXRD)

The configuration of the Bede D1 tool is illustrated in figure 4.1. The Bede D1

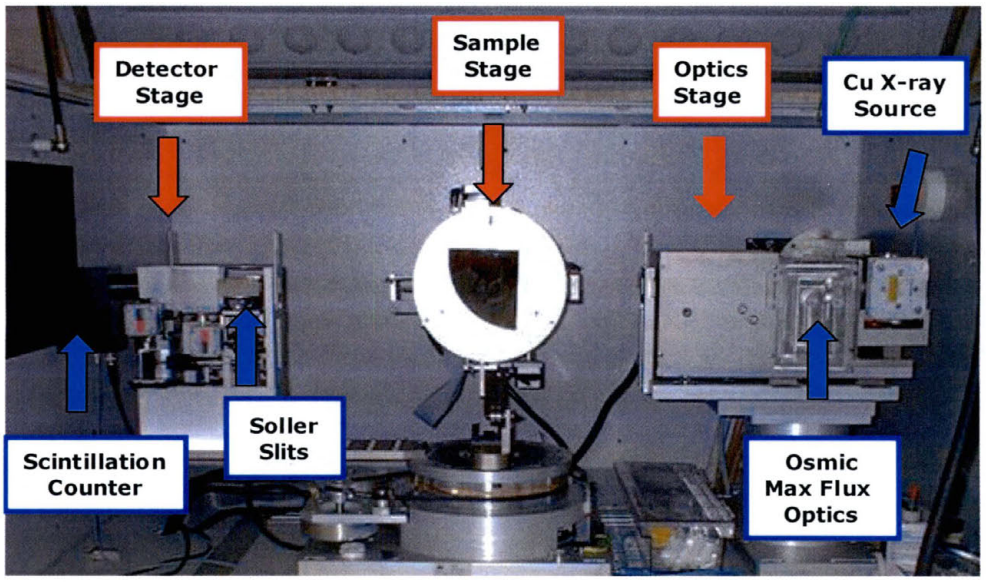

Figure 4.1 – Bede-D1 hardware configuration.

utilizes a sealed off filament x-ray tube that generates copper radiation. For HAXRD scans the incident beam was filtered through an Osmic Max-Flux®optics attachment. This attachment utilizes multilayer x-ray optics, which act as x-ray mirrors to increase the x-ray beam intensity. The Osmic Max-Flux® also has a nickel-carbon layer that absorbs the copper k-beta components of the copper sealed tube radiation source. More detailed information about the Osmic Max-Flux® is presented in Shannon Fritz thesis [19]. The beam proceeds through a 1mm vertical slit, penetrates the sample, passes through a 1mm and a 2mm vertical slit, and enters the detector. The detector is a scintillation counter that converts x-ray photons into optical photons via a scintillator and the optical pulse is amplified by a photomultiplier. An omega offset of –2 degrees was implemented to reduce the intensity of the silicon (004) substrate peak. The Spellman power supply source was set to 40mA and 40kV for all scans.

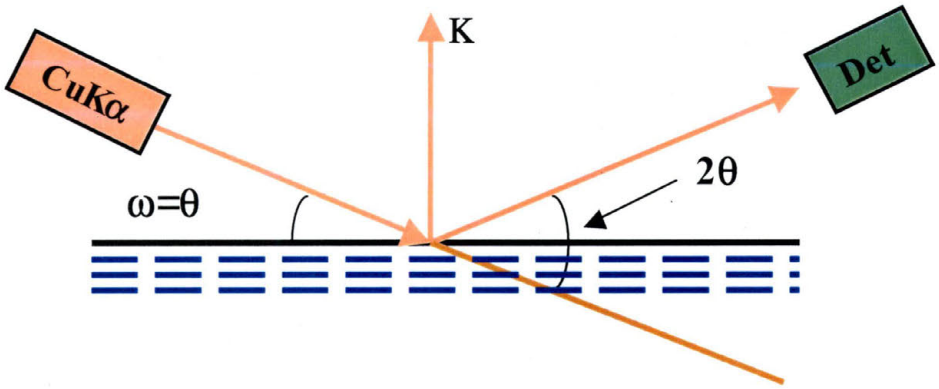

Figure 4.2 – Powder diffraction θ/2θ measurement.

HAXRD was initially utilized to determine the crystalline peaks associated with the Co silicide phases. Figure 4.2 illustrates the HAXRD experimental setup where incident beam penetrates the wafer with omega-2theta moving simultaneously. The 2Theta range of 15° – 60°, was determined from the ICDD software files of Co, Si, Co_2Si_3, Co_2Si, CoSi, and $CoSi_2$ expected peaks with intensities greater than 50%.The diffracted beam is a collection of scattered rays that mutually reinforce each other after penetrating the wafers surface. Figure 4.3 illustrates diffraction of x-rays by a crystal. Diffraction only occurs when the scattered rays produce constructive interference from the planes of atoms in the sample. The diffracted beam creates an angle θ_R of reflection that is equal to the angle θ_I of incidence. The essential criteria that must be met for diffraction to occur is satisfied by Braggs Law.

$$n\lambda=2d(\sin\theta) \quad \text{(Equation 4.1)}$$

This formula created by W.L. Bragg states that the scattered rays 1 and 2 will be in phase when the path difference is equal to the whole number *n* (order of reflectance) of wavelengths λ. The wavelength λ_{Cu} for the copper source is 0.1540 nm for Cu Kα1, 0.1544 nm for Cu Kα2 and 0.1392 nm for Cu Kβ. The lattice spacing of adjacent parallel planes of atoms is d and θ is the angle of diffraction.

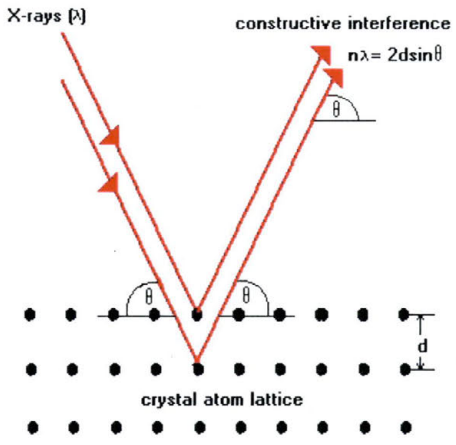

Figure 4.3 – Bragg diffraction of a crystal lattice.

4.3.2. Parallel Beam X-Ray Diffraction (PBXRD)

Samples that did not indicate any monocrystalline formation were analyzed with parallel beam x-ray diffraction to determine if the films were either

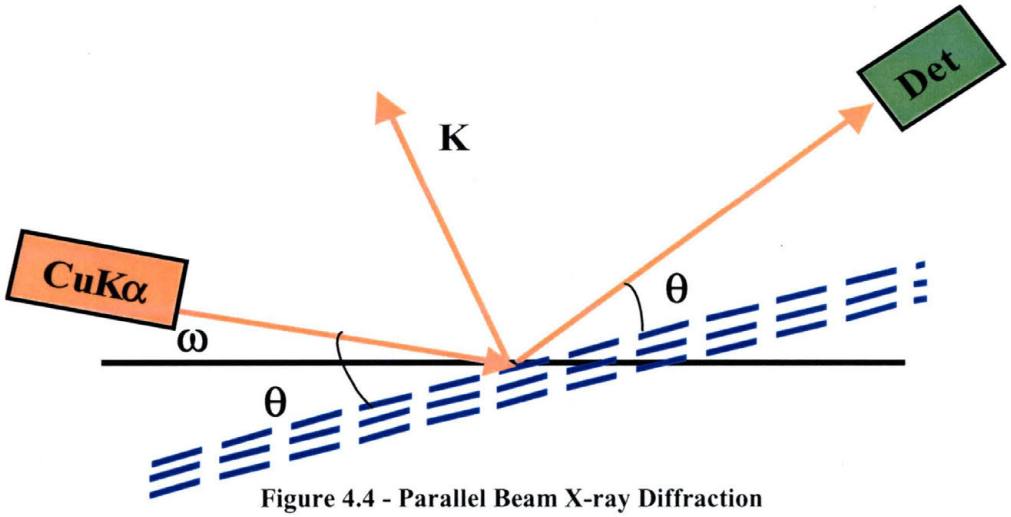

Figure 4.4 - Parallel Beam X-ray Diffraction

polycrystalline or amorphous. This allows the diffraction of x-rays off atomic planes that are not parallel to the substrate. In PBXRD analysis the scattering

vector (K) is no longer always perpendicular to the wafers surface. The PBXRD experimental setup is observed in figure 4.4, where 2Theta moves through a specified range and omega is held at a constant value (typically $0.2° < \omega < 5°$). The grazing incidence geometry makes this technique more sensitive to very thin random polycrystalline films. In the PBXRD configuration the beam proceeded through a 1mm vertical slit, penetrated the sample, passed through a 5mm vertical slit, passed through soller slits, then a 2mm vertical slit, and enters the detector. Soller slits, consisting of a series plates set parallel to each other, were used to collimate the scattered beam. The soller slits are placed before the detector to allow a wide cross-section of the beam to enter the parallel plates and condition the scattered angles of the diffracted beam. The geometry of the scan places the incident x-ray beam at an angle of grazing incidence with the sample, usually between 0.2° and 1°(sometimes up to 5° for thicker films). This small angle of incidence allowed for an enhanced signal from the sample surface. A series of scans was performed at different angles to determine the critical angle θ_C, where x-rays are totally reflected from the wafers surface, and angles above θ_C, which allowed for a degree of depth profiling.

4.3.3. Four Point Probe

Each sample was measured with a Prometrix four-point probe tool to evaluate the electrical properties of the silicide films. In the

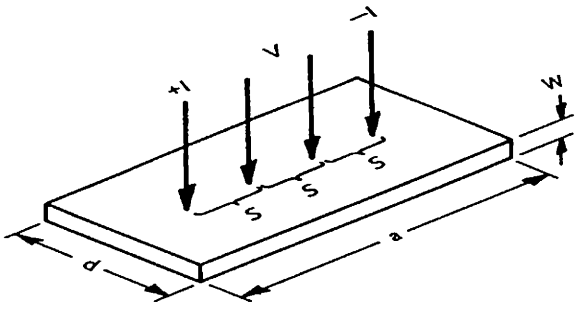

Figure 4.5 – Four-point probe measurement configuration

experiments, four probes were arranged in-line and in contact with the sample. Each sample was approximately 3cm square. The samples were measured at room temperature with a Tungsten carbide probe designed for metal films. The probe radius was 1.6mil, with 100gm of loading, and a spacing of 1mm. A constant current source of 2.35mA was applied to the two outer probes and a sensing voltage across the inner probes. The measurement of resistivity was obtained from the voltage drop across the two inner probes and the applied current. A square wave was used to apply a voltage. The relationship was defined as R = V/I. Figure 4.5 illustrates the probe configuration.

4.3.4. Scanning Electron Microscopy (SEM)

Scanning electron microscopy has the capability to produce an image that is higher in magnification, resolution, and field depth than any optical microscope. The morphology data obtained is created by beam source of electrons that are accelerated to the sample surface of energies from 500eV to 40KeV. Various physical phenomena occur when the electrons bombard the surface, the emission of electrons and x-rays are the most significant for SEM analysis. The cross-section SEM analysis was completed on a Hitachi-4700 field emission SEM. The samples were prepped with a Buffered Oxide etch to smooth the cleaved edge of the wafers to be analyzed. Both samples were capped with TEOS (Tetra Ethyl Ortho Silicate) to aid in the thickness measurement of the layers formed. Silver paint, a conductive adhesive that provides a conductive path for electrons to travel, is used to attach the sample pieces to a Si strip. The samples are also sputter coated with Platinum to makes the whole sample (the sample piece plus

the Si strip) conductive. The platinum provides a nice uniform conductive coat that makes it easier to obtain an image. The key function of this analysis was to obtain film thickness and the morphology of the films and their interfacial formation. One sample was polished to obtain a clearer view of the grain formation.

The second set of SEM images were plan-view views of the silicide film obtained by a Phillips FEL XC-30. The wafers were coated with platinum to prevent charging. The main purpose of the plan-view view of the silicide process was to determine the surface morphology and how it related to the sheet resistivity measurements.

5. DATA ANALYSIS

Each design of experiment included high angle x-ray diffraction analysis. Parallel beam x-ray analysis was performed to identify the crystalline nature of the films if mono-crystalline formation was not initially evident. The x-ray diffraction patterns of the cobalt silicide films were identified from the JCPDS-International Center for Diffraction Data files. The cobalt silicide JCPDS files are listed in appendix A. The 2Theta range was 15 - 60° to obtain the corresponding XRD pattern that would yield the most intense peaks of the cobalt, cobalt silicide, and cobalt oxide films. All XRD scan were offset by 2 degrees to prevent the silicon substrate peaks from dwarfing the silicide peaks. If the 1st anneal did not indicate a Co_2Si_3 film, the 2Theta range was reduced to 25 - 60°. The Co_2Si_3 is not a well established phase, but was more likely to occur at a lower temperature. Since the formation of silicide on a barrier oxide layer has not been extensively researched, the possibility of Co_2Si_3 phase formation was not ruled out. None of the x-ray diffraction analysis contained characteristic peaks of either the Co_2Si_3 phase or the cobalt oxide phase. The silicide films containing a mixture of cobalt mono- and di-silicide contained intensity peaks associated with CoSi (110) at 28.5° and $CoSi_2$ (111) at 28.8°. In several of the XRD scans the peak shift of this 2Theta position from 28.5° to 28.8° occurs illustrating the occurrence of a phase transformation from CoSi to $CoSi_2$. For electrical characterization, sheet resistivity (Rs) data was obtained for all

films samples. The scanning electron microscopy was performed on a few select samples.

5.1. 1st Design of Experiment

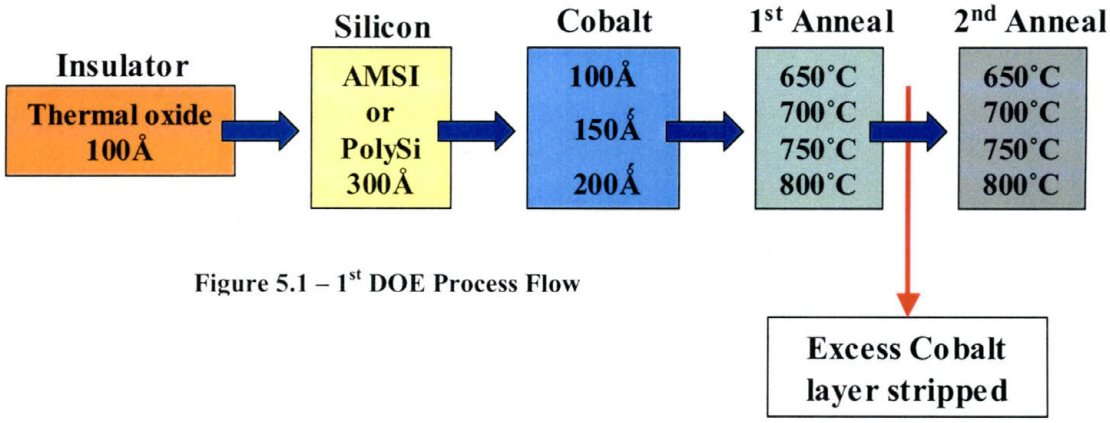

Figure 5.1 – 1st DOE Process Flow

Lot# 3092614

The first design of experiment (DOE) was processed sequentially as depicted in the above figure 4.1. The AMSI was 300Å and PolySi layer thickness varied around 350Å. The thickness of the Si layers was measured optically by a Thermawave tool provided by SEMATECH and the Poly-Si layer formed thicker than expected. The thicker film growth was attributed to a new process flow that was executed for the thin furnace grown poly-silicon layer. The above cobalt layers are deposited on AMSI or PolySi and annealed at the temperatures listed. Figure 5.2 illustrates the sheet resistivity data for Co silicide after the first anneal. The duration of the 1st anneal was 60s and the temperature range included 650°C, 700°C, 750°C, and 800°C. These data points are grouped for each Co thickness for AMSI and Poly-Si layers. The sheet resisitivity ranged between 15Ω/sq to 70 Ω/sq. As illustrated there is miminal differences between the annealing

temperatures with in each group. However, each individual group does differ, especially the low sheet resistivity of the Poly-Si layer with a Co thickness of 100Å.

After the 1st anneal the wafers are cleaved into pieces and annealed at each of the subsequent temperatures in the second anneal step.

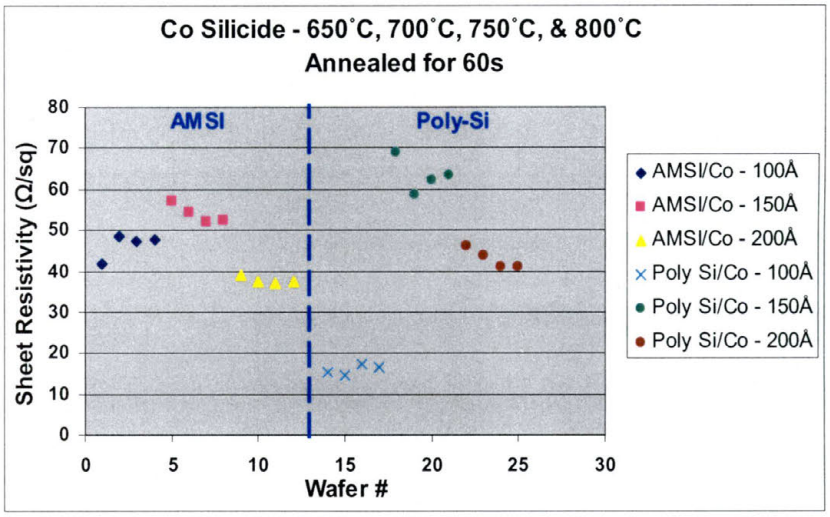

Figure 5.2 – Sheet Resistivity Comparison of Lot# 3092614.

Wafers scribed 1 - 12 were deposited with amorphous silicon and wafers scribed 14 – 25 were deposited with poly-silicon. Evaluation of the splits is described as follows:

Amorphous Silicon wafers #1 - #12

5.1.1. Wafer #1-4 (Cobalt - 100Å)

Wafer #	1st Anneal	2nd Anneals			
1	650°C	650°C	700°C	750°C	800°C
2	700°C	650°C	700°C	750°C	800°C
3	750°C	650°C	700°C	750°C	800°C
4	800°C	650°C	700°C	750°C	800°C

Table 5.1 – Wafer #1-4 anneal matrix

The High Angle X-ray Diffraction (HAXRD) scans (appendix B, figure B.1 – B.4) do not indicate any strong evidence of a crystalline structure for the first anneal or any subsequent second anneal temperatures. The graphs consist of a 1st anneal scan (purple) which is at the bottom of the graph and 2nd anneals that are sequentially placed with increasing temperature, beginning with the second scan

(dark blue) from the bottom. There is only a slight trend of CoSi peaks observed around 28.6° (110) and 46.1° (210). Further investigation required analyzing these films with Parallel Beam X-ray Diffraction (PBXRD) to determine if the samples were amorphous or poly-crystalline in nature. For grazing incidence analysis, the angle of incidence varied, the omega values were = 0.35°, 0.50°, 0.65° (appendix B, figure B.5). The diffraction scans indicated a poly-crystalline silicide formation. The CoSi peaks are observed at 28.6° (110), 46° (210), and 50.5° (211). Due to the high sheet resistivity values obtained from the 1st and 2nd anneals, additional PBXRD scans were only performed on wafer # 1 to characterize the second anneal. The angle of incidence was set to omega = 0.50, to obtain peaks from the poly-crystalline CoSi film layer. Figure B.6 in appendix B, illustrates the poly-crystalline formation that occurred PBXRD scans. The XRD pattern indicates a slight mixture of $CoSi_2$ into the CoSi film. Weak peaks at 2Theta at 28.7° and 48.4° are characteristic of the $CoSi_2$ phase.

The sheet resistivity (Rs) measurements of this wafer set ranged between 40 – 50 Ω/sq after the 1st anneal and an overall trend of increased Rs after all 2nd anneals (appendix B, figure B.7). Due to the high Rs values and the weak formation of poly-crystalline CoSi-$CoSi_2$ phase mixture, these samples do not illustrate any beneficial electrical properties that could be applied to thin silicided gates.

5.1.2. Wafer #5-8 (Cobalt - 150Å)

Wafer #	1st Anneal	2nd Anneals			
5	650°C	650°C	700°C	750°C	800°C
6	700°C	650°C	700°C	750°C	800°C
7	750°C	650°C	700°C	750°C	800°C
8	800°C	650°C	700°C	750°C	800°C

Table 5.2 – Wafer #5-8 anneal matrix

The HAXRD analyses of the first anneal illustrated an intense peak of about 300cps on all four samples (appendix B, figure B.8-B.11). The only dominant peak formed at 45.7°, which corresponds to the CoSi (210) plane. It appears that the CoSi layer has formed with a preferential grain growth at the expense of all the other expected planes listed in the JCPDS file. After the second anneal, the CoSi (210) plane continues to be the predominant crystalline plane to align with the substrate. The peak increases by 100 – 200 cps per sample on all second anneals. The Rs data of the first anneal of all four wafers ranged from 47 - 57 Ω/sq (figure B.12). After the second anneal, as the CoSi (210) plane continues to form, the Rs values only varied around ±5 Ω/sq compared to the first anneal. There is no indication that any particular 2nd anneal temperature corresponded to an increase in the formation of the CoSi (210) plane, but the most intense peaks of each wafer group correspond to the lowest Rs data. In comparison to the previous set of wafers with the 100Å cobalt layer (Co:AMSI ratio of 3:5), the Rs data of the crystalline CoSi layer (Co:AMSI ratio of 1:1) is only about 5 Ω/sq lower. Therefore, the crystalline formation of CoSi (210) plane did not substantially optimize the electrical properties of the Co silicide film.

5.1.3. Wafer #9-12 (Cobalt - 200Å)

Wafer #	1st Anneal	2nd Anneals			
9	650°C	650°C	700°C	750°C	800°C
10	700°C	650°C	700°C	750°C	800°C
11	750°C	650°C	700°C	750°C	800°C
12	800°C	650°C	700°C	750°C	800°C

Table 5.3 – Wafer #9-12 anneal matrix

The HAXRD illustrates the CoSi (210) atomic layer repeatedly dominated the crystal structure (figure B.13-B.16). Due to the additional 50Å of cobalt, the intensity of the peak after the 1st anneal was between 400 to 500 cps. After the 2nd anneal the CoSi (210) peak still dominated and its intensity increased from around 650 to 850 cps. Even though the peaks varied with intensity, a strong correlation of CoSi (210) peak formation cannot be attributed to one single 2nd anneal temperature. This is also evident in the sheet resistivity measurements where all of the 1st and 2nd anneal Rs data remained around 35 Ω/sq with minimal variation (figure B.17). The additional 50Å increased the formation of the CoSi (210) plane and reduced the Rs value compared to the cobalt layer of 150Å in the previous set of wafers. The Rs values were still however within the polySi range of 30-60 Ω/sq and are not optimal materials for replacing the PolySi gate.

Poly Silicon wafers #14 - #25

5.1.4. Wafers # 14-17 (Cobalt - 100Å)

Wafer #	1st Anneal	2nd Anneals			
14	650°C	650°C	700°C	750°C	800°C
15	700°C	650°C	700°C	750°C	800°C
16	750°C	650°C	700°C	750°C	800°C
17	800°C	650°C	700°C	750°C	800°C

Table 5.4 – Wafer #14-17 anneal matrix

The HAXRD analysis is only indicative of either a weak CoSi (120) peak at $2\theta = 46°$ of or a $CoSi_2$ (111) peak at $2\theta = 29°$ (figure B.18-B.21). The graphs consist of a 1st anneal scan (dark blue) which is at the bottom of the graph and 2nd anneals that are sequentially placed with increasing temperature, beginning with the second scan (red) up from the bottom. Both 1st and 2nd anneals temperatures had minimal effect on the intensity of this 2Theta-Omega peak at 29°. There is no strong evidence of any crystalline structure aligning parallel to the silicon substrate. To further determine the crystalline order, PBXRD analysis was performed. PBXRD scans determined if the layers were polycrystalline or amorphous in nature. Wafer #14 was initially evaluated at several omega values (figure B.22) between 0.25° and 1° to determine the critical angle any polycrystalline film may have formed on the substrate. For a more dense film, a larger critical angle is observed. The 0.25° omega angle was barely penetrating the surface of the sample, but slightly larger angles of incidence were able to detect a combination of CoSi and $CoSi_2$ peaks. The peaks observed correspond to the following phases: 29° → CoSi (110) and /or $CoSi_2$ (111), 46° → CoSi (210), 48° → $CoSi_2$ (220), and 50.5° → CoSi (211).

The additional scans done to characterize this group of wafers included PBXRD analysis with the omega angle set to 0.35° and 0.70° to obtain data from the surface layers and data from the planes of silicided layers (figure B.23-B.30). The Rs data was remarkably low, ranging from 15-25 Ω/sq (figure B.31). It is also noteable that the Rs data values only vary slightly from the 1st to 2nd anneals. The Rs data indicated no instability due to an increase in temperature.

The increase in instability has previously been observed for Cobalt silicided layers that are formed on a infinite supply of silicon [1]. The formation of $CoSi_2$ along with CoSi is possibly due to a limited amount of silicon which did

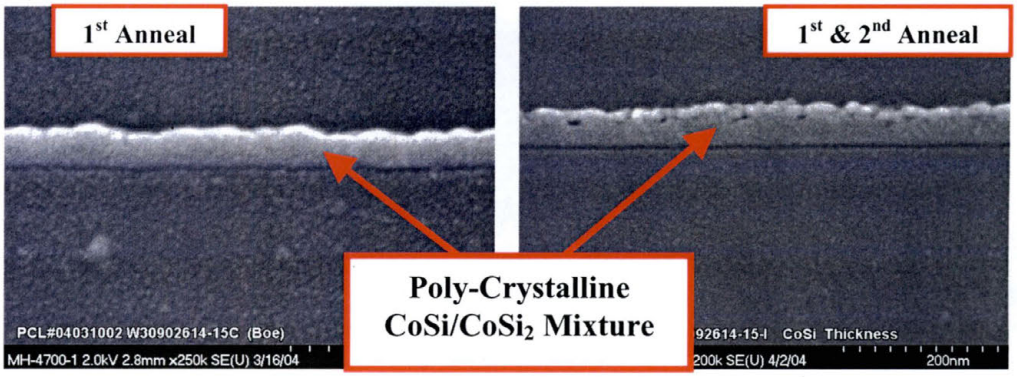

Figure 5.3 – SEM images of (a) 60s 1st anneal at 700° and (b) Subsequent 2nd 60s anneal at 650°.

not allow a complete transformation into a $CoSi_2$ phase. Figure 5.3 illustrates a cross-section SEM pictures of the poly-crystalline $CoSi/CoSi_2$ mixture for the first and second anneal steps. Sample #15 had the lowest Rs values and was therefore choosen for cross-section SEM imagine. Tetraethyl ortho-silicate (TEOS) was deposited on top of the silicide and a buffered oxide etch was applied to obtain a sharp picture of the silicide film. The dark line underneath the silicide was the thermal oxide barrier layer. The silicide thickness after a 60s, 700°C first anneal was 400-450Å thick. After a 60s, 650°C second anneal the film had an increased amount of agglomeration and the $CoSi/CoSi_2$ mixture increased to 400-500Å thick. Even though the sheet resistivity decreased, the surface roughness increased. The second anneal image appears to have an augmented grain boundary formation.

5.1.5. Wafers # 18-21 (Cobalt - 150Å)

Wafer #	1st Anneal	2nd Anneals			
18	650°C	650°C	700°C	750°C	800°C
19	700°C	650°C	700°C	750°C	800°C
20	750°C	650°C	700°C	750°C	800°C
21	800°C	650°C	700°C	750°C	800°C

Table 5.5 – Wafer #18-21 anneal matrix

The HAXRD analysis indicates a CoSi (210) crystalline layer present with the most intense peak at $2\theta = 45.8°$ observed in all scans (figure B.32-B.35). The graphs consist of a 1st anneal scan (dark blue) which is at the bottom of the graph and 2nd anneals that are sequentially placed with increasing temperature, beginning with the second scan (red) up from the bottom. The CoSi (110) peak is evident in wafer #20 and #21 at $2\theta = 28.5°$ and the CoSi (211) peak in wafer #21 at $2\theta = 50.5°$. The added 50Å of cobalt produced a stronger CoSi alignment to the (210) peak and prevented the formation of the $CoSi/CoSi_2$ phase mixture. The intensity of the 45.8° peak was initially 50cps for all the 1st anneals and remained around 60cps for all 2nd anneals. The only impact temperature had on the different peak formations of the CoSi layer was the 1st anneal. All subsequent anneals only slightly increased the monocrystalline growth. The sheet resistivity data illustrates values that ranged from 58 to 67Ω/sq for all 1st anneal wafers (figure B.36). For the second anneal values there was an overall trend of Rs decreasing, ranging from 50 to 60Ω/sq, with the 700°C second anneal having the largest impact on lowering the Rs data values. Since the Rs increases at the 800°C second anneal step, it indicates that the silicide was in a metastable phase and the higher temperature has initiated the transformation into the next phase, i.e.

$CoSi_2$. Due to the limited amount of silicon, the phase transformation cannot continue. The XRD data and Rs values for this set of wafers were not indicative of any silicide films that could be potential candidates for gate applications.

5.1.6. Wafers # 22-25 (Cobalt - 200Å)

Wafer #	1st Anneal	2nd Anneals			
22	650°C	650°C	700°C	750°C	800°C
23	700°C	650°C	700°C	750°C	800°C
24	750°C	650°C	700°C	750°C	800°C
25	800°C	650°C	700°C	750°C	800°C

Table 5.6 – Wafer #22-25 anneal matrix

The HAXRD analysis illustrated a dominant CoSi (210) peak at 45.7° (figure B.37-B.40). There were some slight indications of a (211) CoSi peak, as illustrated in the x-ray diffraction graphs. The peak height varied at most 50 cps between 1st and 2nd anneals, therefore the second anneal had little affect on the progression of the CoSi growth. This was also evident in the Rs data where the values only range from 36 to 44Ω/sq (figure B.41). The small range of values between the 1st and 2nd anneal step illustrated that the CoSi layer was more stable than the previous set of wafers. This was due to the extra 50A of cobalt that allows more 1:1 Co: Si bonds. There is even less excess Si to enable a metastable state that would allow the possible formation of the disilicide phase.

5.2. 2nd Design of Experiment

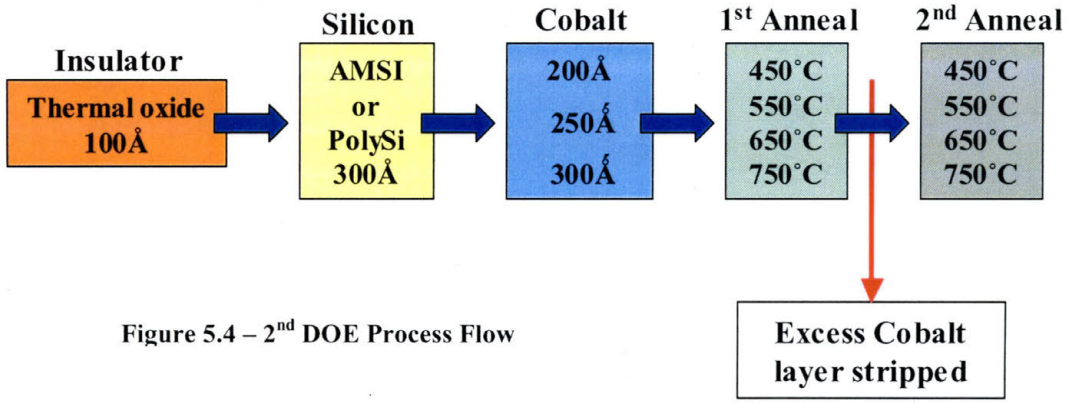

Figure 5.4 – 2nd DOE Process Flow

Lot# 3092615

The previous formation of the CoSi films with the dominant (210) peak lead to a further investigation of the thicker cobalt films and a temperature range expansion to include lower 1st and 2nd anneal temperatures. Since cobalt is the dominant diffuser in the initial stages of silicidation, mainly observed in the first anneal, a thicker cobalt layer was deposited. The cobalt was increased to 250Å and 300Å to possibly form a thin cobalt interfacial layer between the silicide and thermal oxide. An interfacial layer would provide a good contact between the silicide and SiO_2 films. A thicker cobalt film was also implemented to alter the crystalline formation that formed in the previous lot. The lower temperature range was included to determine if the phase sequence of cobalt silicide formation was directly correlated to the initial anneal temperature. A metastable CoSi-$CoSi_2$ phase mixture formed at higher temperatures might have prohibited the $CoSi_2$ phase formation in the subsequent anneal step. Both 300Å AMSI and 300Å PolySi were implemented into this DOE. The thickness of the PolySi film was verified by optical measurements performed by the Thermawave tool.

Amorphous Silicon Films

5.2.1. Wafer #1-2 (Cobalt - 200Å)

Wafer #	1st Anneal	2nd Anneals			
1	450°C	450°C	550°C	650°C	750°C
2	550°C	450°C	550°C	650°C	750°C

Table 5.7 – Wafer #1-2 anneal matrix

In the previous lot# 3092614, wafers 9 – 12 had the same film stack, but higher 1st and 2nd anneal temperatures. In figures B.42-B.43, HAXRD scans illustrated that the lower 450°C and 550°C 1st anneals did not have a different affect on the subsequent silicidation formation during the second anneal process. The silicide film continued to generate the CoSi (210) dominant peak. The peaks of these films appear more intense, but the background intensity started at 100 cps higher than the previous wafers in lot# 3092614. Moreover, the sheet resistivity values ranged similarly, around 35 Ω/sq, as the previous wafer set in the first design of experiment (figure B.44).

5.2.2. Wafer #3, 4, 13, & 14 (Cobalt - 250Å)

Wafer #	1st Anneal	2nd Anneals			
3	450°C	450°C	550°C	650°C	750°C
4	550°C	450°C	550°C	650°C	750°C
13	650°C	450°C	550°C	650°C	750°C
14	750°C	450°C	550°C	650°C	750°C

Table 5.8 – Wafer #3, 4, 13, & 14 anneal matrix

HAXRD scans in figure B.44-B.48 illustrated the outcome of a thicker 250 Å cobalt layer. Wafer #3, 450°C first anneal, presented the highest CoSi (210) peak, which remained stable after the second anneal process. The 550°C 1st anneal, wafer #4, illustrated a CoSi (210) peak about 200cps lower than #3 and gained

intensity after the second anneal step. The CoSi (210) peak for wafer #13, 650°C 1st anneal, was initially 400cps less than #3, but the monocrystalline formation increased to match the intensity of wafer #3 by the 750°C second anneal. Wafer #14 began with a CoSi (210) peak intensity of 1379 cps, similar to #13, but the second anneal temperatures did not further the mono-crystalline growth. The higher sheet resistivity data generated from the 1st and 2nd anneals of wafer #14 corresponded to the lower peak intensities in the HAXRD scans (figure B.49). The Rs values, 30 Ω/sq, were likely a result of the fast agglomeration that has previously been documented for thin film cobalt silicidation greater than 700°C [7]. For wafers 3, 4, and 13, the thicker Co layer increased the CoSi (210) layer and decreased the Rs to around 25 Ω/sq for all other 1st and 2nd anneal temperatures.

5.2.3. Wafer #5, 6, 15, & 16 (Cobalt - 300Å)

Wafer #	1st Anneal	2nd Anneals			
5	450°C	450°C	550°C	650°C	750°C
6	550°C	450°C	550°C	650°C	750°C
15	650°C	450°C	550°C	650°C	750°C
16	750°C	450°C	550°C	650°C	750°C

Table 5.9 – Wafer# 5, 6, 15, & 16 anneal matrix

The HAXRD analysis in figures B.50-B.53 illustrated a decrease in peak intensity due to the additional 50Å of cobalt. Wafers 5 and 6 began with a CoSi (210) peak intensity of around 1200cps and the intensity only varied by 100cps in the preceding second anneal steps. Wafers 15 and 16 initially formed CoSi (210) peaks with intensities of about 1200cps and varied by 100cps in the second anneal process. The sheet resistivity data showed a similar trend as compared to the

250Å Co film thickness (figure B.54). However the 750°C 1st anneal of the 300Å Co film had a larger jump in data to an Rs value around 35 Ω/sq. The higher sheet resistance values were attributed to the fast agglomeration of the thin silicide film formation.

Poly-Silicon Films

5.2.4. Wafer #7-8 (Cobalt - 200Å)

Wafer #	1st Anneal	2nd Anneals			
7	450°C	450°C	550°C	650°C	750°C
8	550°C	450°C	550°C	650°C	750°C

Table 5.10 - Wafer# 7 & 8 anneal matrix

These wafers were also annealed at a lower temperature to potentially alter the silicide phase formation. Again, the HAXRD data (figure B.55-B.56) initially appears greater than wafers #22 – 25 in lot# 3092614 (figure B.37-B.40), but this is also due to the increase in background intensity of 100cps. The second anneal temperatures had a minimal effect on the crystalline CoSi formation, which only produced ≈50Å gain in intensity. The sheet resistance values for the 1st anneal values (figure B.57) were about 5 Ω/sq less for the 450°C and 550°C anneal temperatures compared to the Rs data (figure B.41) obtained from wafers #22-25 in lot# 3092614. Comparing the second anneal values between the 6 sets of data, the values only differ by about 3 Ω/sq.

5.2.5. Wafer #9, 10, 17, & 18 (Cobalt - 250Å)

Wafer #	1st Anneal	2nd Anneals			
9	450°C	450°C	550°C	650°C	750°C
10	550°C	450°C	550°C	650°C	750°C
17	650°C	450°C	550°C	650°C	750°C
18	750°C	450°C	550°C	650°C	750°C

Table 5.11 - Wafer# 9, 10, 17, & 18 anneal matrix

HAXRD scans illustrated the resultant CoSi (210) peaks of the 250Å thick cobalt layer to reach an intensity around 500cps for the initial anneal process step (figure B.58-B.61). Each subsequent anneal only varied with a peak intensity of about 50cps. The PolySi layer did not produce a large increase in intensity as compared to the CoSi layers formed from AMSI films. The textured formation of the PolySi film restricted the crystalline growth of the CoSi (210) film. The added 50Å of cobalt had an effect on the Rs data (figure B.62). Similar to the AMSI-300Å/Co-250Å silicide layers, the Rs data was also reduced by 10 Ω/sq and the 750°C 1st anneal has the highest Rs data in the wafer group.

5.2.6. Wafer #11, 12, 19, & 20 (Cobalt - 300Å)

Wafer #	1st Anneal	2nd Anneals			
11	450°C	450°C	550°C	650°C	750°C
12	550°C	450°C	550°C	650°C	750°C
19	650°C	450°C	550°C	650°C	750°C
20	750°C	450°C	550°C	650°C	750°C

Table 5.12 - Wafer# 11, 12, 19, & 20 anneal matrix

The HAXRD analysis illustrated an overall decrease in intensity for the 300Å cobalt films by about 50Å(figure B.63-B.70). The 2nd anneal had a minimal effect on the peak formation with a variance less than 50Å between peak heights. The Rs data remained in the same range as the previous 250Å cobalt layer wafer set

except for the 750°C 1st anneal. In figure B.71 these values increased by about 15 Ω/sq and illustrated the same pattern as the AMSI-300Å/Co-300Å wafer set. The polycrystalline Si layer allowed more thermal instability than the amorphous Si film. It was interesting to note how the Rs data values for the AMSI and PolySi corresponded so well with each other with the 3 different cobalt thicknesses. Even though the AMSI film stack illustrated an increase in monocrystalline formation, the electrical data follows the same pattern for both AMSI and PolySi film stacks. The wafers formed from the AMSI film stack may indicate a larger

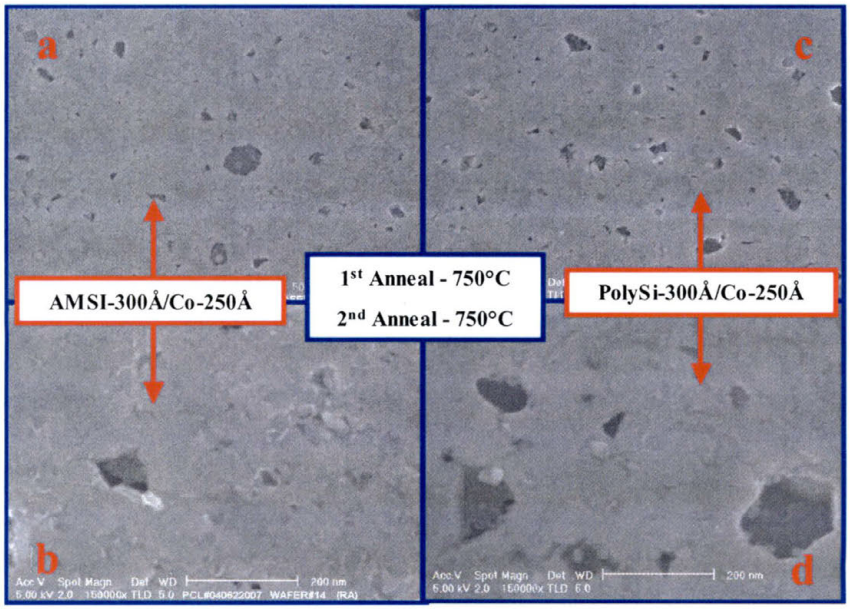

Figure 5.5 – Plan-view SEM images of AMSI-300Å/Co-250Å at a magnification of a) 50X, b) 150X , & of PolySi-300Å/Co-250Å at c) 50X, and d) 150X.

amount of crystalline formation, but the analogous Rs data suggests a similar rough surface morphology as the silicides generated from the PolySi film stack. Plan-view SEM images were performed to determine if the surface structure for the PolySi-300Å/Co-250Å and AMSI-300Å/Co-250Å were analogous, due to

their Rs data. The images in figure 5.5 illustrate the same surface morphology, i.e. defects and voids that would produce similar electrical data.

The x-ray diffraction scans did not indicate the formation of any cobalt interfacial layer between the silicide and thermal oxide films. All layers that formed were mono-crystalline in nature. The only phase present was the CoSi crystalline phase with the (210) plane aligned parallel with the Si substrate. The CoSi (210) peak remained the dominant peak in all of the HAXRD scans. The reoccurrence of the single dominant peak may indicate that the $CoSi_2$ formation is impeded by a lack of Si atoms as opposed to Co atoms. The sheet resistivity behavior of CoSi formed from the PolySi and AMSI film stack is due to the same surface roughness.

5.3. 3rd Design of Experiment

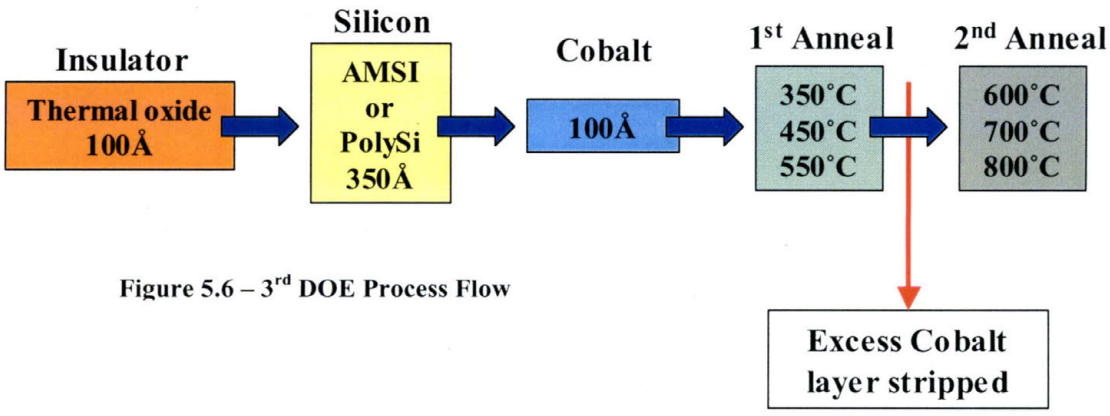

Figure 5.6 – 3rd DOE Process Flow

Lot# 3092616

The motivation behind this experiment was to determine the affect of a lower temperature 1st anneal on the silicidation process and to further investigate the affects of a thicker 350Å silicon layer. This DOE was broken up into two parts. The first part included 4 wafers deposited with 100Å cobalt on 350Å PolySi and 350Å AMSI, prior to the anneal

process, to determine the initial silicide formation due to cobalt deposition alone. Higher temperature anneals of the Co:Si ratio of 1:2 respectively was previously investigated in the 1st DOE. Therefore, the next part included six additional wafers with 100Å cobalt, processed with a low 1st anneal temperature and a high 2nd anneal temperature.

5.3.1. Wafer #1-4 (Cobalt - 100Å)

Wafer #	Si	Deposition
1	AMSI	350°C
2	AMSI	250°C
3	PolySi	350°C
4	PolySi	250°C

Table 5.13 - Wafer# 1-4 anneal matrix

HAXRD analysis was utilized to characterize any initial interactions between the furnace grown silicon and the sputtered cobalt. All of the experiments in this study were performed with a 350°C cobalt deposition temperature. However, two deposition temperatures, 250° and 350C° were employed for comparison purposes. The HAXRD graphs (figure B.68 and B.69) only indicate one dominant peak, which matches the JCDPS file (appendix A) for the Co (111) peak at $2\theta = 44.255°$. Cobalt deposition on the amorphous layer illustrates a higher peak intensity than the poly-silicon layer. This indicates that the initial interaction during cobalt deposition is less for the AMSI-Co layer stack. The AMSI-Co stack was influenced more by temperature. The shifted peak from 44.4° to 44.7° indicates more initial interaction between the AMSI and cobalt has occurred. The peak reduction and peak shift to the right, towards the CoSi (210) peak, is indicative of an increased amount of interaction between the two layers. The PolySi-Co stack was affected less by the temperature change. The pronounced

difference in the initial interaction between the silicon and deposited cobalt explains why the reactions in the anneal process differed for the AMSI-Co and PolySi-Co films.

5.3.2. Wafer #5-7 (AMSI - 350Å)

Wafer #	1st Anneal	2nd Anneals		
5	350°C	600°C	700°C	800°C
6	450°C	600°C	700°C	800°C
7	550°C	600°C	700°C	800°C

Table 5.14 - Wafer# 5-7 anneal matrix

The HAXRD and PBXRD analysis of the first anneal, in figure B.70 and B.71, indicate that the initial interface transforms into an amorphous layer. The graphs consist of a 1st anneal scan (dark blue) which is at the bottom of the graph and 2nd anneals that begin with the second scan (red) and then sequentially placed with increasing temperature. Monocrystalline formation occurred after the 700°C and 800°C second anneal temperatures were carried out. The peak at $2\theta = 28.5°$ is characteristic of the CoSi (210) peak. The subsequent first anneal temperatures, 450°C and 550°C, converted the initial Co-Si reacted layer into a poly-crystalline film, illustrated in figure B.73 and B.75. The HAXRD analysis indicates that only a small amount of the poly-crystalline silicide film was transformed into a more ordered crystalline state (figure B.72 and B.74). The peak placement is again characteristic of a CoSi-$CoSi_2$ phase mixture as seen in previous Poly-Si stacks (figure B.23- B.30, PBXRD 14-17). This is the first indication of a mono-crystalline CoSi-$CoSi_2$ mixture for the AMSI-Co film stack. The 1st anneal temperatures of 650°C formed a poly-crystalline phase mixture This mono-crystalline mixture was not evident in the HAXRD scans (figure B.1-B.4) of the

AMSI-Co film stack, annealed at a higher initial temperature, ranging from 650°C - 800°C. However the PBXRD scan in figure B.6 did indicate a CoSi-$CoSi_2$ mixture after the second anneal process step.

The sheet resistivity data of the AMSI-350Å/Co-100Å film stack (figure B.80) was less overall compared to the AMSI-300Å/Co-100Å film stack in figure B.7 (Rs of wafers 1-4). The 350°C and 450°C first anneal values were the exception. The HAXRD analysis and high Rs data associated with their films illustrated the recrystallization of the as deposited Co-Si films into an amorphous and polycrystalline films that were not supplied a sufficient heat of formation to produce a metastable cobalt silicide phase. The 350°C and 450°C anneal temperatures did not provide enough energy to form a cobalt silicide phase. The reduced sheet resistivity observed in the AMSI-350Å/Co-100Å stack was attributed to the 50Å increase in Si, which enabled an ordered crystalline silicide phase to form and /or a lower 1st temperature anneal that reduced Co film agglomeration.

5.3.3. Wafer #8-10 (Poly-Si - 350Å)

Wafer #	1st Anneal	2nd Anneals		
8	350°C	600°C	700°C	800°C
9	450°C	600°C	700°C	800°C
10	550°C	600°C	700°C	800°C

Table 5.15 - Wafer# 8-10 anneal matrix

The HAXRD analysis of the Poly-Si film stack demonstrated a high order of crystallinity than the previous AMSI-Co films (figure B.77). The graphs consist of a 1st anneal scan (dark blue) which is at the bottom of the graph and 2nd anneals that begin with the second scan (red) and then sequentially placed with increasing

temperature. The only poly-crystalline formation was observed in the 350°C first anneal shown in figure B.78. The subsequent anneals performed on wafer #8 indicate only a slight increase in crystallinity. The peak placement and height illustrate an increase in silicidation growth after the second anneal steps. It is not distinctively apparent whether or not the broadened peaks are characteristic of CoSi or a CoSi-$CoSi_2$ mixture. The 450°C and 550°C first anneal HAXRD scans illustrate a CoSi-$CoSi_2$ mixture that is more $CoSi_2$ enriched. This is evident in the formation of the $CoSi_2$ peak at 48.2° and the shift of CoSi (110) peak closer to the $CoSi_2$ (111) peak as illustrated in figure B.79 and B.80.

The sheet resistivity data continued to read higher for the 350°C first temperature anneal, which was similar to the AMSI-350Å/Co-100Å film stack. The high Rs value of 1011 Ω/sq was attributed to the small amount of crystalline order formed (figure B.76). The 450°C and 550°C Rs values are less for the 1st anneal, but the 550°C is the lowest due to the initial formation of the CoSi-$CoSi_2$ phase mixture. Wafers 8 and 9 possessed lower 2nd anneal Rs values, but there is an upward trend for each 100°C increase in temperature. Wafer 10 initially had the lowest sheet resistance, however it also trended upward with increasing temperature. The increase in Rs might be due to an increase in silicon consumption, as silicon is consumed, instability occurs until another metastable state is encountered. An increase in Rs data has previously indicated an instability resulting from a phase change and/or island formation [20]. In comparison to earlier results (figure B.31), the sheet resistivity was less stable for the samples with first low temperature anneals.

5.4. 4th Design of Experiment

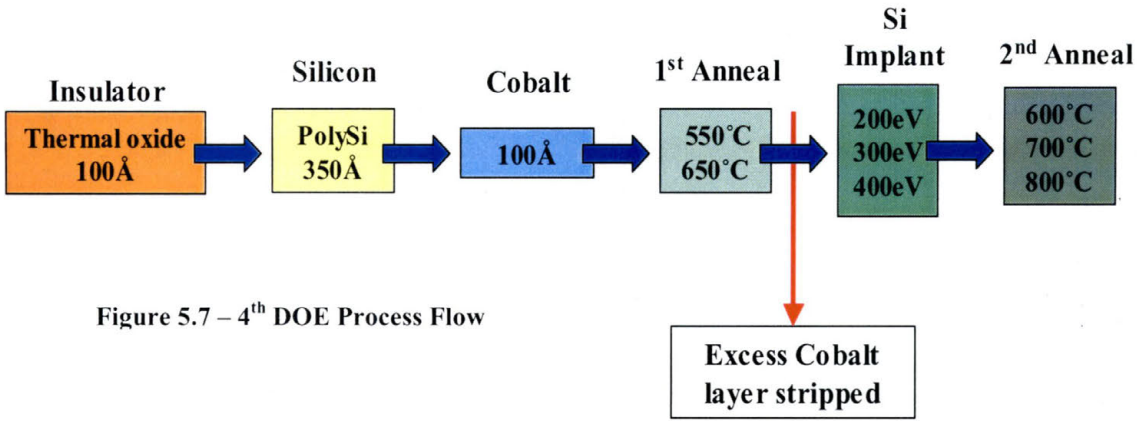

Figure 5.7 – 4th DOE Process Flow

Lot #3092616C

Since the wafers were initially forming a phase mixture of CoSi and $CoSi_2$ after the first anneal and did not complete the phase transformation of CoSi into $CoSi_2$, it was thought that the CoSi → $CoSi_2$ transition was limited by a limited supply of silicon. Therefore Si was implanted after the 1st anneal and excess cobalt metal etch step. The incorporation of Si by implantation was an attempt to supply additional Si to the phase mixture and/or introduce defects that would allow further mobilization of the Si atoms. However, due to the low Si ion implant dose of $1x10^{15}$ ions/cm^2 the additional supply of silicon was minimal. Each wafer had the same PolySi-350Å/Co-100Å film stack. The 1st anneal temperatures were 550°C and 650°C, the implants were carried out using Si with a dose of $1x10^{15}$ ions/cm^2 at 200eV, 300eV, and 400eV, and the 2nd anneal temperatures were 600°C, 700°C, and 800°C. Due to the thin 400Å silicided film, ion implantation was processed at low energies. The first anneal temperatures were limited to the 550°C and 650°C, since previous wafers processed at these temperatures attained the lowest sheet resistance values.

5.4.1. Wafer #19-21 (1st Anneal 550°C)

Wafer #	1st Anneal	Implant	2nd Anneals		
19	550°C	200eV	600°C	700°C	800°C
20	550°C	300eV	600°C	700°C	800°C
21	550°C	400eV	600°C	700°C	800°C

Table 5.16 - Wafer# 19-21 anneal matrix

The HAXRD analysis in figure B.81-B.83 included a 1st anneal, post implant, and three 2nd anneal scans. The graphs consist of a 1st anneal scan which is at the bottom (dark blue) of the graph, next an implant scan (red) and finally three 2nd anneal scans are sequentially placed with increasing temperature. Amorphization of the silicide phase mixture in the post implant scan did not occur. There was only a sight indication of crystalline order alteration. However, there was a significant difference between the crystalline formation of the implanted versus the non-implanted (figure B.79) wafers after the second anneal. The implanted wafers benefited from the Si ion bombardment by an increase in the $CoSi_2$ phase formation. The $CoSi_2$ (111) and $CoSi_2$ (220) peaks were more pronounced in the implanted wafers and the crystalline order increased with increasing temperature. The energy implant comparison (figure B.84) does not reveal a substantial difference between the implant energies, in the altering the crystalline order. Implantation was simulated by SRIM (The Stopping and Range of Ions in Matter) software, the results are in figure B.85-B.87. The maximum simulated allowed dose was $1x10^8$ ions/cm^2 and the dose of the implanted wafers was $1x10^{15}$ ions/cm^2. The simulation reproduced a silicon ion penetration depth around 50Å. Due to the dose limitation, it is possible that the ions could have penetrated up to

100Å. The simulation illustrated a large amount of backscattering, which restricted the penetration depth of the Si ions.

The sheet resistivity data of the post implant wafers did not significantly vary from the 1st anneal values (figure B.88). The Rs data still illustrated an increase in resistivity with temperature, but the overall data values were less than the non-implanted wafers (figure B.89). An additional post implant sample was annealed, at 800°C for 300s, to test the silicide phase stability. The five minute anneal resulted in a stable silicide with an Rs value of 20Ω/sq.

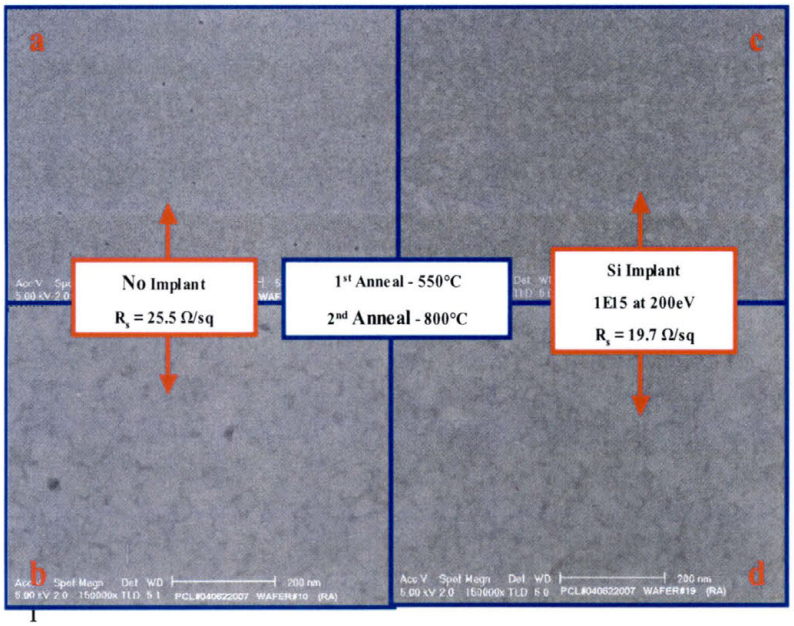

Figure 5.8 – Plan-view SEM images comparing the surface topography of non-implanted with a magnification of a) 50X & b) 150X versus implanted c) 50X & d) 150X of a PolySi-350Å/Co-100Å film stack.

1

ew SEM was performed to compare the surface topography of the implanted and non-implanted wafers. Figure 5.8 shows an improved morphology achieved by the Si implantation, which explains the lower Rs data. P. S. Lee et al. also reported the same SEM and Rs results for Ni silicide formed on BF^{+}_{2} and N^{+}_{2} implanted Poly-Si.(figure 5.9 and 5.10) illustrates the plan-view SEM analysis

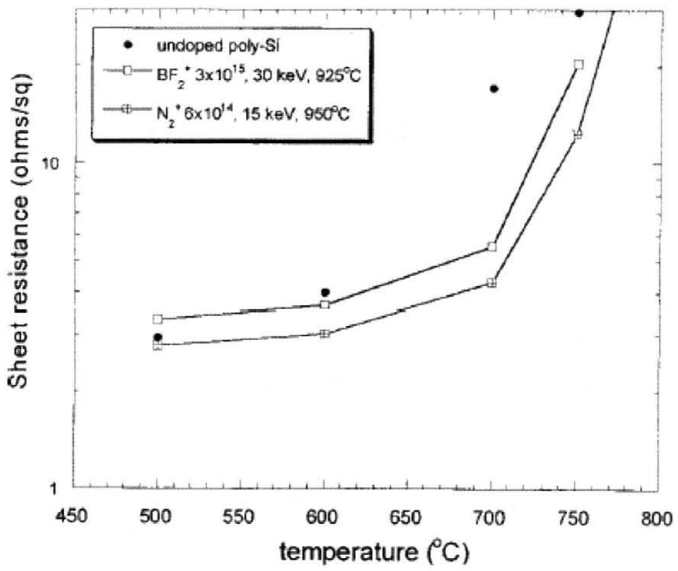

Figure 5.9 –Sheet Resistance of Ni on undoped and doped poly-Si after annealing at various temperatures [21]

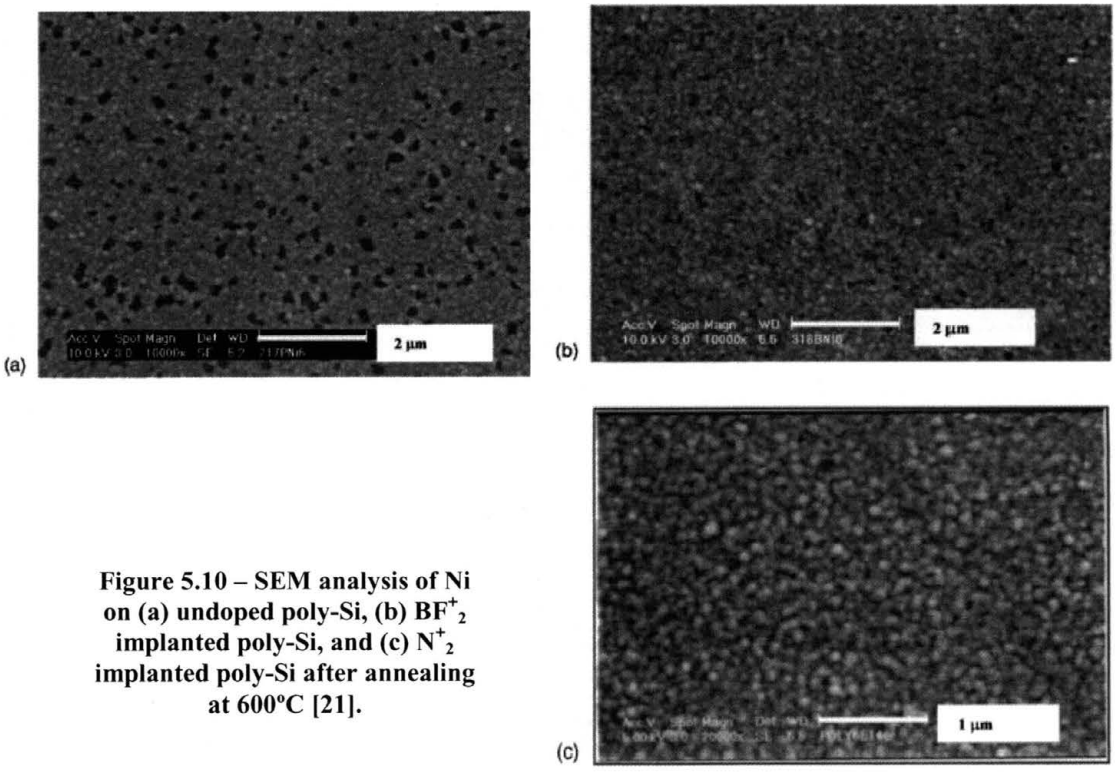

Figure 5.10 – SEM analysis of Ni on (a) undoped poly-Si, (b) BF^+_2 implanted poly-Si, and (c) N^+_2 implanted poly-Si after annealing at 600°C [21].

of both implanted and anneal samples [21]. Layer inversion is observed on the non-implanted Poly-Si samples, which is analogous to the previous results obtained in the second DOE (figure 5.5). The implanted Poly-Si films show the same improved surface morphology as the implanted cobalt silicide films. The Rs behavior of the Ni silicided Poly-Si was also lower, as compared to the non-implanted samples.

5.4.2. Wafer #22-24 (1st Anneal 650°C)

Wafer #	1st Anneal	Implant	2nd Anneals		
22	650°C	200eV	600°C	700°C	800°C
23	650°C	300eV	600°C	700°C	800°C
24	650°C	400eV	600°C	700°C	800°C

Table 5.17 - Wafer# 22-24 anneal matrix

HAXRD analysis results were similar to the previous implanted wafers. The post second anneal crystalline phase formation followed the same trend (figure B.90-B.92). The graphs consist of a 1st anneal scan (dark blue) which is at the bottom of the graph, next an implant scan (red), and finally three 2nd anneal scans are sequentially placed with increasing temperature. The implantation energy comparison shows less disordering of the crystalline structure (figure B.93). The Rs values for the 200eV and 300eV implant energies remained similar to the previous wafers set, but the 400eV Rs value set maintained values closer to the non-implanted wafers (figure B.94).

5. CONCLUSION

The ultimate goal was to form a fully $CoSi_2$ silicide film on thermal oxide that exhibits desirable electrical properties. The data obtained in my experiments characterized the phase formation of cobalt silicide layer and their electrical properties. The phase formation was identified by high angle x-ray diffraction and parallel beam x-ray diffraction and the corresponding peaks were verified with the JCPDS-International Centre for Diffraction Data Files. The initial cobalt reaction was also characterized with x-ray diffraction. The amorphous and poly-crystalline films illustrated different growth mechanisms in the cobalt deposition and silicidation process. The amorphous silicon and poly-crystalline silicon readily formed a monocrystalline CoSi on Co films thicker than 100Å. However the amorphous films formed a thicker monocrystalline layer. For the 100 Å cobalt film the 350Å poly-crystalline silicon readily formed a mono- and/or poly-Co/ $CoSi_2$ mixture with a low sheet resistivity value. The various cobalt thicknesses did not result in a cobalt interfacial layer, but as the cobalt thickness increased up to a Co:Si ratio of 3:2, the monocrystalline CoSi formation increased and the sheet resistance decreased. The electronic properties were obtained through sheet resistivity measurements and scanning electron microscope analysis corresponded the physical and electrical data. Since $CoSi_2$ phase formation was not attained, further electrical analysis to characterize the work function produced by the silicide films was not performed. Several

$CoSi_2$–CoSi film multiphase mixtures were formed, but a transformation into the $CoSi_2$ single phase was not obtained due to an insufficient amount of silicon atoms. The silicon ion implantation did not supply enough silicon to transform the $CoSi_2$–CoSi mixture into a pure $CoSi_2$ film. However, implantation did improve surface morphology and reduce sheet resistivity as compared to the non-implanted samples. An increase in implantation energy may amorphize the silicide layer further and decrease the defects throughout the silicide layer. A tri-layer of Si-Co-Si would increase the supply of Si atoms to the silicide process. Due to contamination issues, this process was currently not an option. The phase transformation to a fully $CoSi_2$ film, may have been impeded by ambient oxygen contamination. However, the XRD analysis did not indicate a cobalt oxide and/or cobalt silicate oxide in the silicide samples. Further investigation with secondary ion mass spectroscopy (SIMS) or Rutherford Backscattering (RBS) analysis may give insight into any possible cobalt oxide interfacial layers. The implementation of a titanium capping layer could reduce and/or prevent any oxidation or fast agglomeration that occurs during the 1^{st} and 2^{nd} anneal process steps. Except for samples initially annealed at a high temperature (> 700°C), the silicide formation remained very stable through subsequent anneals. The mono-crystalline CoSi phases formed from PolySi and AMSI silicon remained very stable in terms of sheet resistivity values. Implementation of this process using nickel would be beneficial, since NiSi has the lowest resistivity values of the nickel silicide process. The nickel silicidation formation could be controlled by the thermal oxide barrier and remain stable due to the limited amount of silicon atoms. Ion implantation of Ni silicide has already produced positive results.

APPENDIX A

Co
JCPDS – 15-0806
CuKα x-ray source
Cubic a = 3.545

2θ	Intensity	h	k	l
44.255	100	1	1	1
51.568	40	2	0	0
75.927	25	2	2	0

$Co_2 SiO_4$
JCPDS – 29-0508
CuKα x-ray source
Cubic a = 8.138

2θ	Intensity	h	k	l
18.889	40	1	1	1
31.086	12	2	2	0
36.619	100	3	1	1
38.318	11	2	2	2
44.546	43	4	0	0

$Co_2 Si_3$
JCPDS – 42-0827
CuKα x-ray source
Tetragonal a = 5.234(3)
c = 8.543(5) C = 1.632

2θ	Intensity	h	k	l
16.903	50	1	0	0
20.776	50	0	0	2
34.263	15	2	0	0
38.404	30	2	1	0
44.186	15	2	1	2
49.211	100	2	2	0
49.211	100	1	1	4
52.422	20	3	0	0

2θ	Intensity	h	k	l
26.914	30	1	0	1
31.026	30	2	1	0
32.533	70	1	1	1
39.491	50	2	1	1
42.401	50	3	1	0
44.141	100	0	2	1
44.832	70	2	2	0
45.305	100	3	0	1
46.034	100	1	2	1
48.650	100	0	0	2
49.211	50	3	1	1
53.546	100	3	2	0
53.886	30	1	1	2
54.935	30	4	1	0
57.557	30	1	3	0

$Co_2 Si$
JCPDS – 04-0847
CuKα x-ray source
Orthorhombic a = 7.109
b = 4.918 c = 3.737

Co Si
JCPDS – 08-0362
CuKα x-ray source
Cubic a = 4.43

2θ	Intensity	h	k	l
28.493	60	1	1	0
34.882	50	1	1	1
40.796	40	2	0	0
45.886	100	2	1	0
50.463	90	2	1	1

$Co Si_2$
JCPDS – 38-1449
CuKα x-ray source
Cubic a = 5.364

2θ	Intensity	h	k	l
28.814	90	1	1	1
33.399	2	2	0	0
47.921	100	2	2	0
56.894	23	3	1	1

APPENDIX B

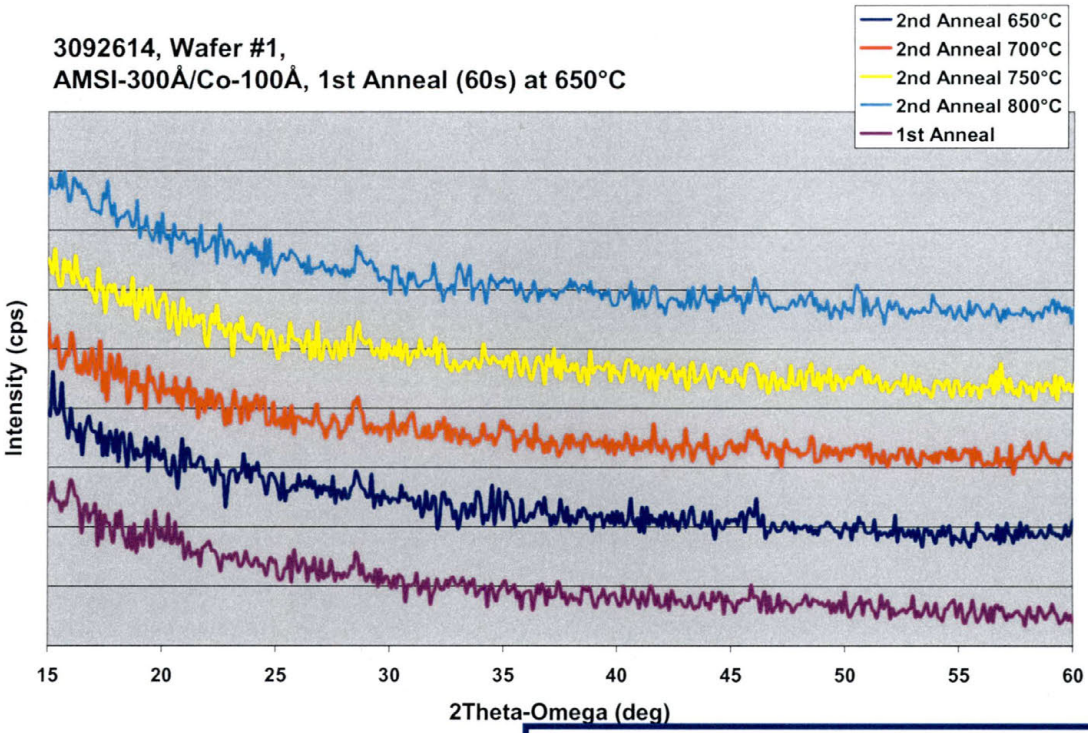

Figure B.1 - HAXRD 3092614 - Wafer# 1

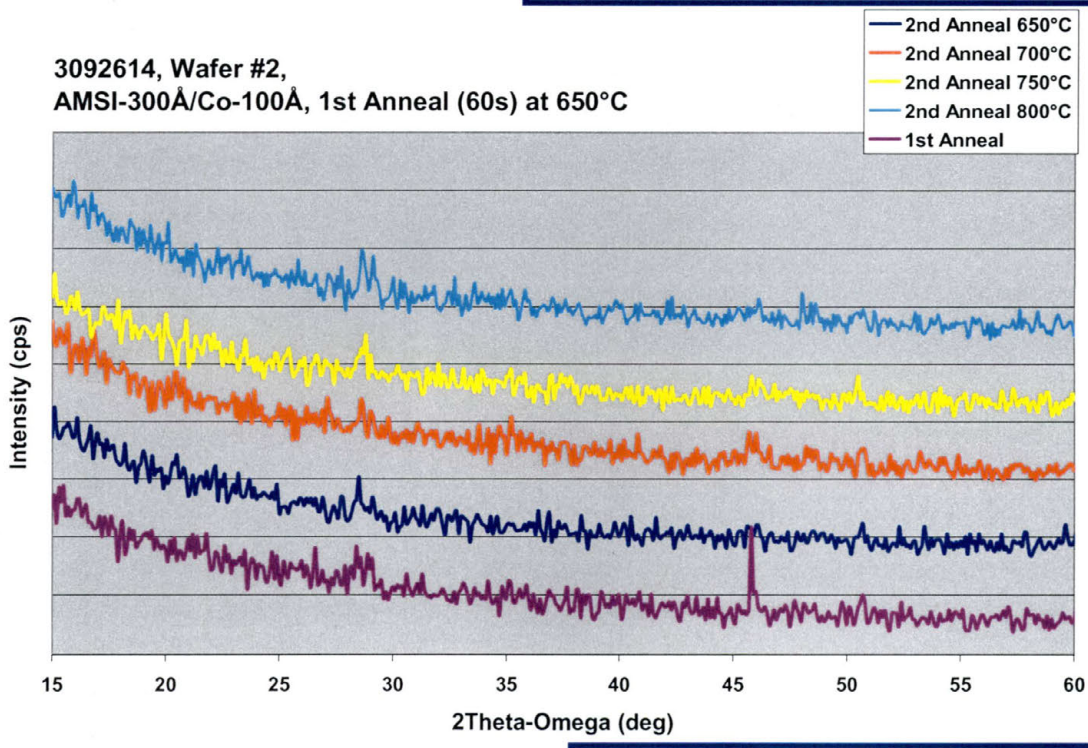

Figure B.2 - HAXRD 3092614 - Wafer# 2

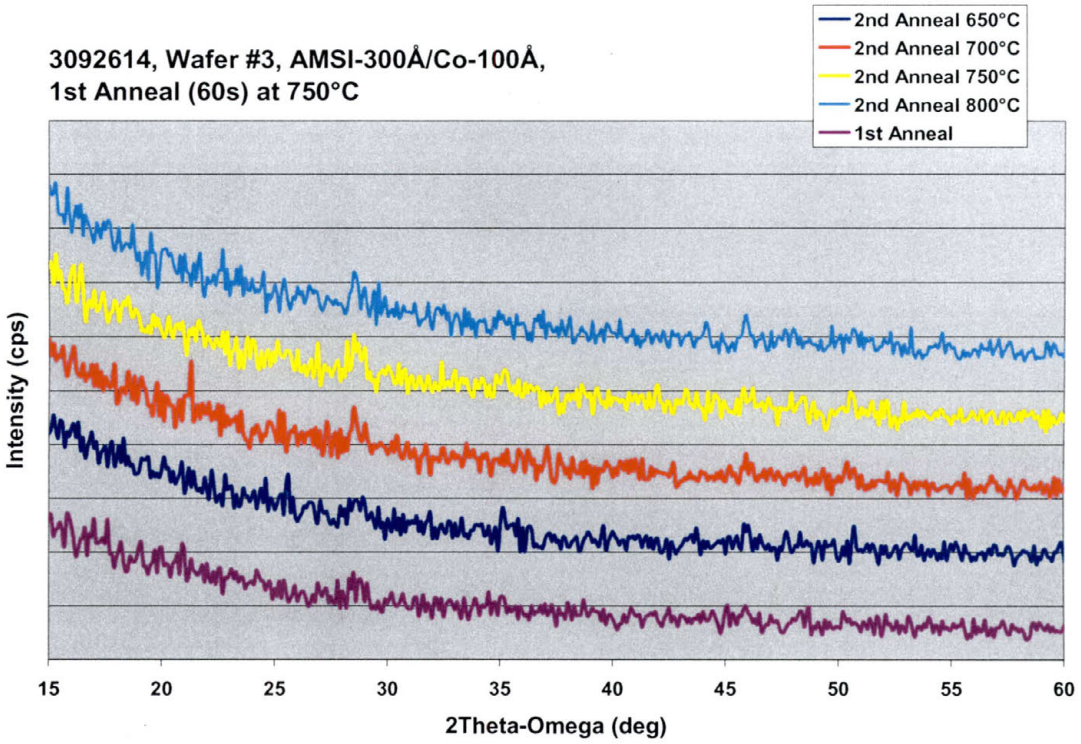

Figure B.3 - HAXRD 3092614 - Wafer# 3

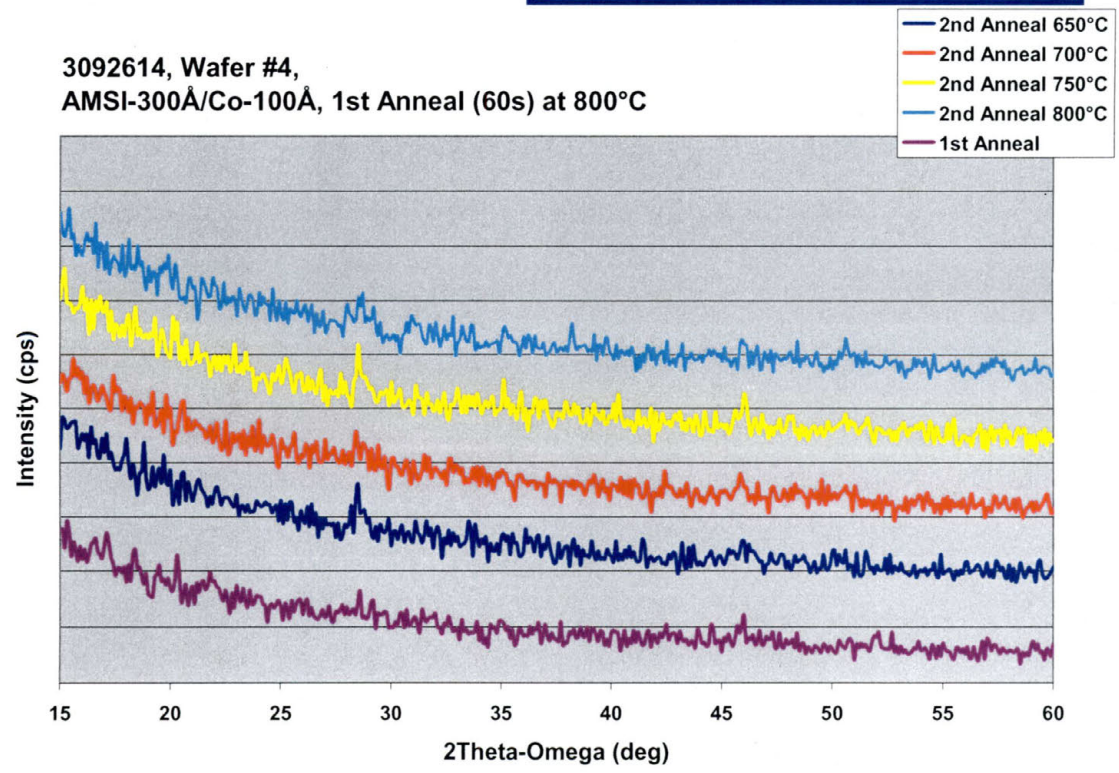

Figure B.4 - HAXRD 3092614 - Wafer# 4

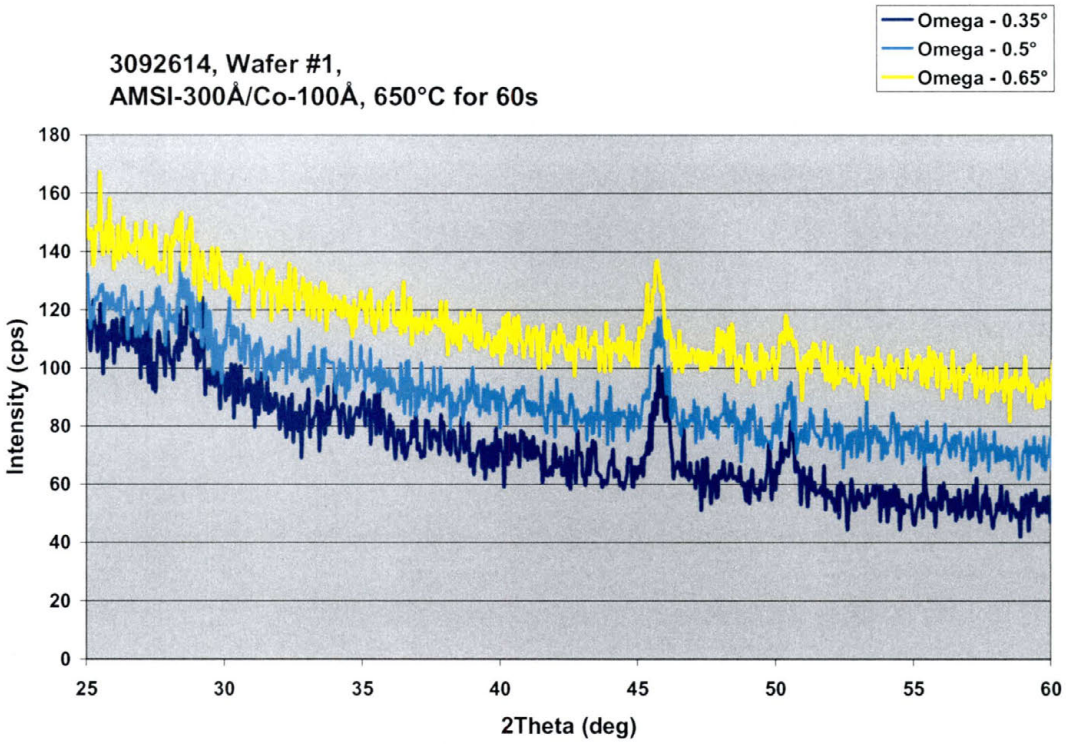

Figure B.5 - PBXRD Omega comparison 3092614 - Wafer# 1

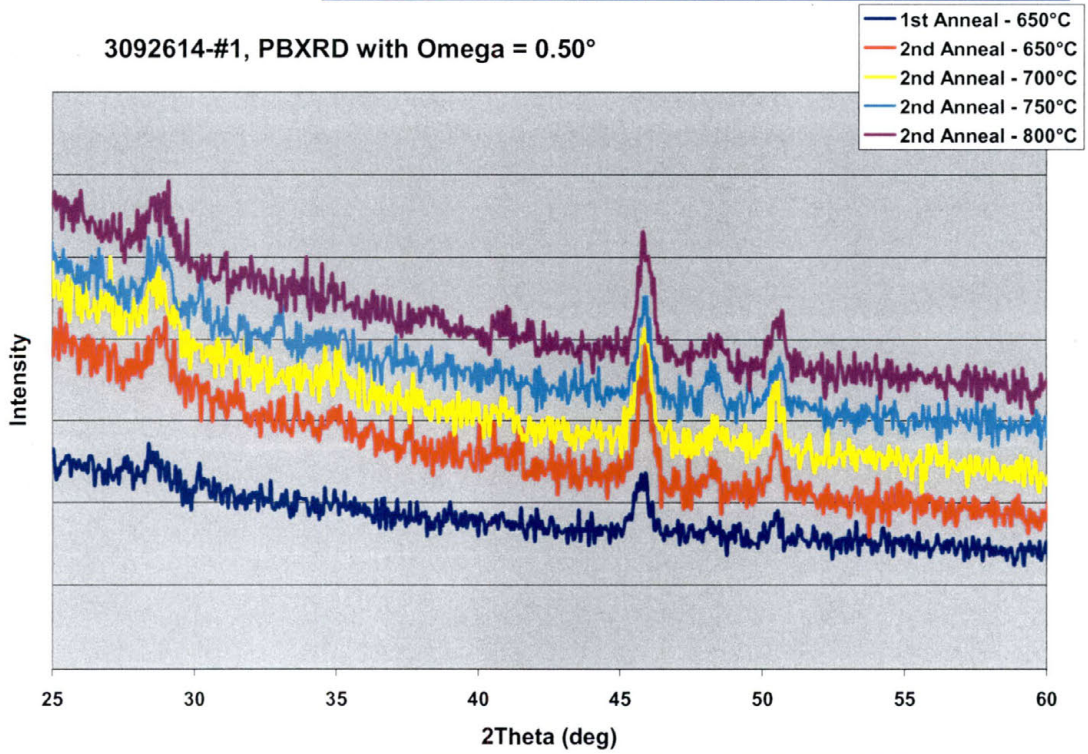

Figure B.6 – PBXRD (Omega = 0.5°) 3092614 - Wafer# 1

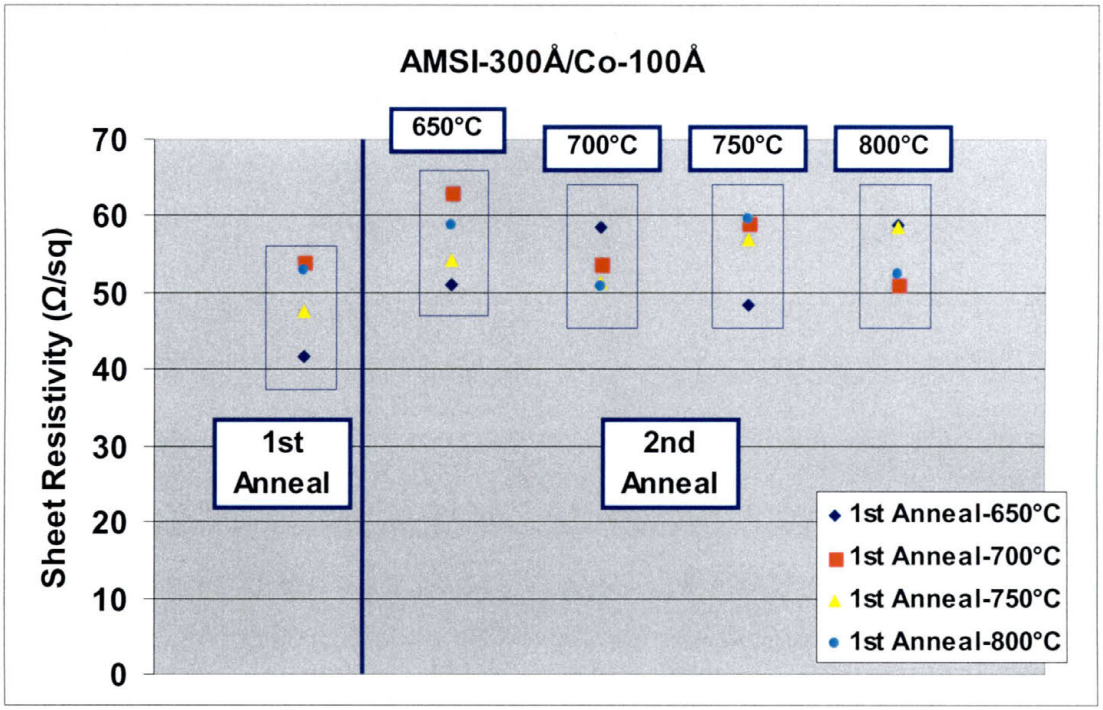

Figure B.7– Rs 3092614 - Wafer# 1-4

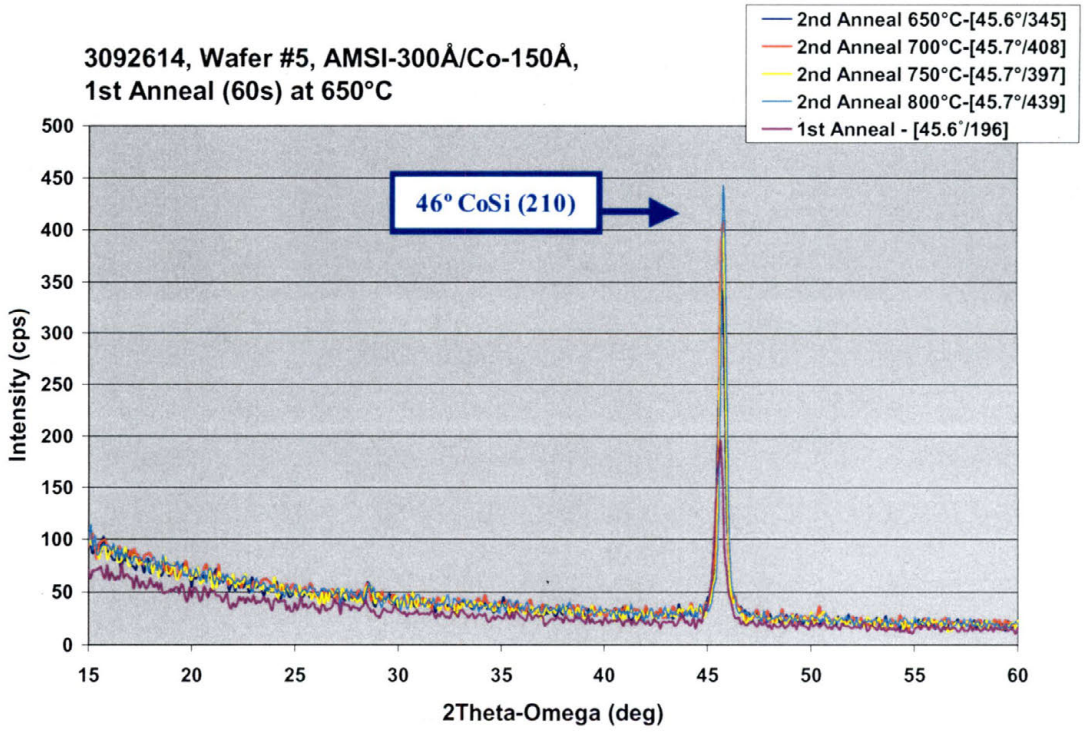

Figure B.8– HAXRD 3092614 - Wafer# 5

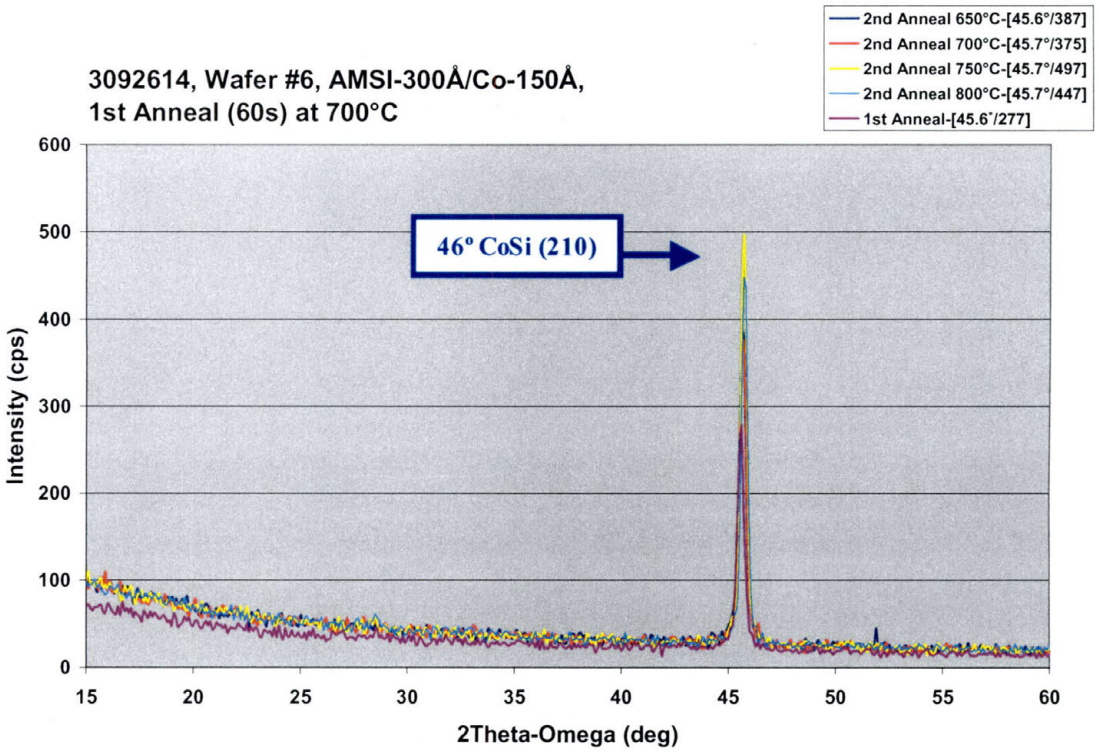

Figure B.9– HAXRD 3092614 - Wafer# 6

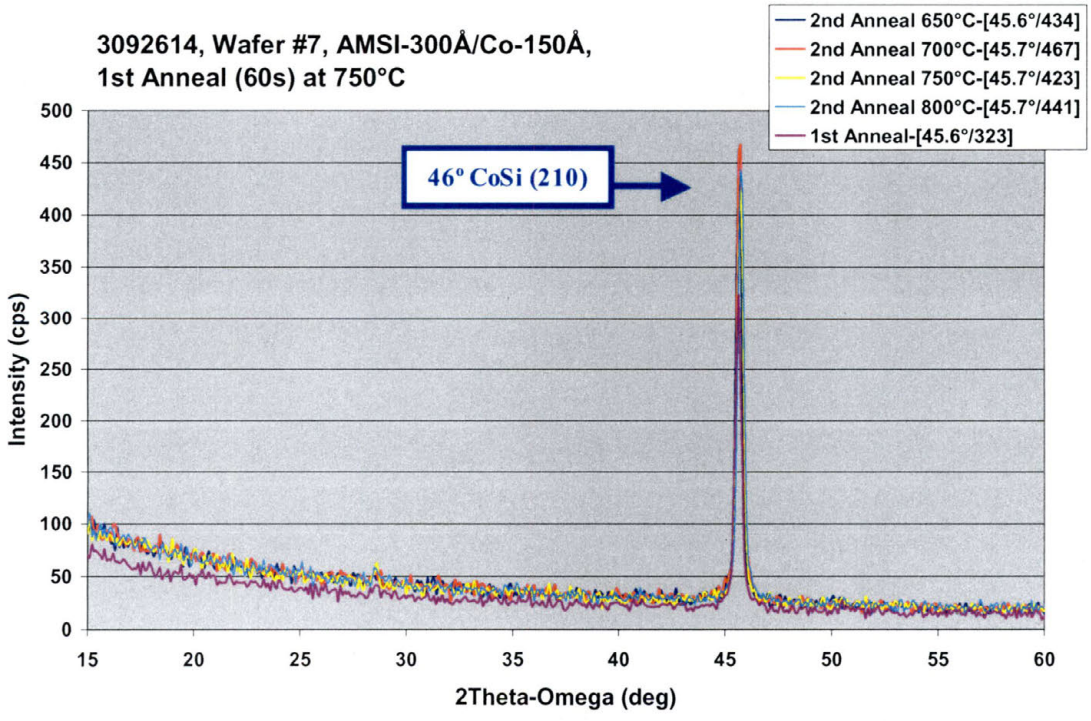

Figure B.10– HAXRD 3092614 - Wafer# 7

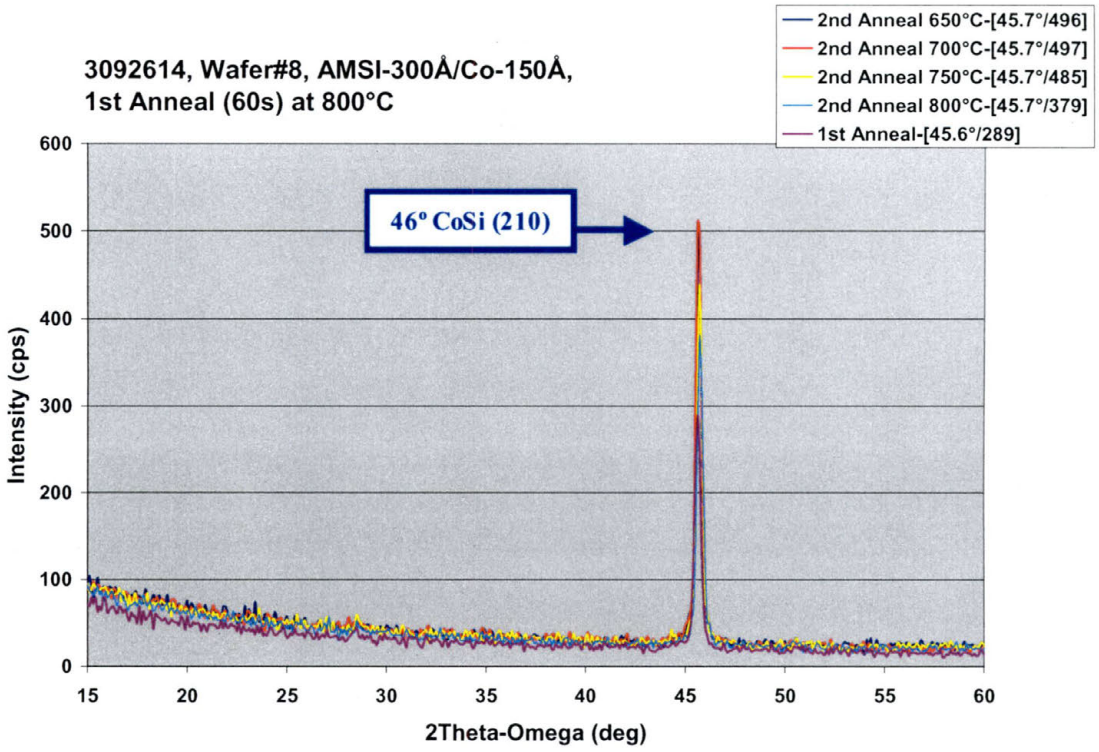

Figure B.11 – HAXRD 3092614 - Wafer# 8

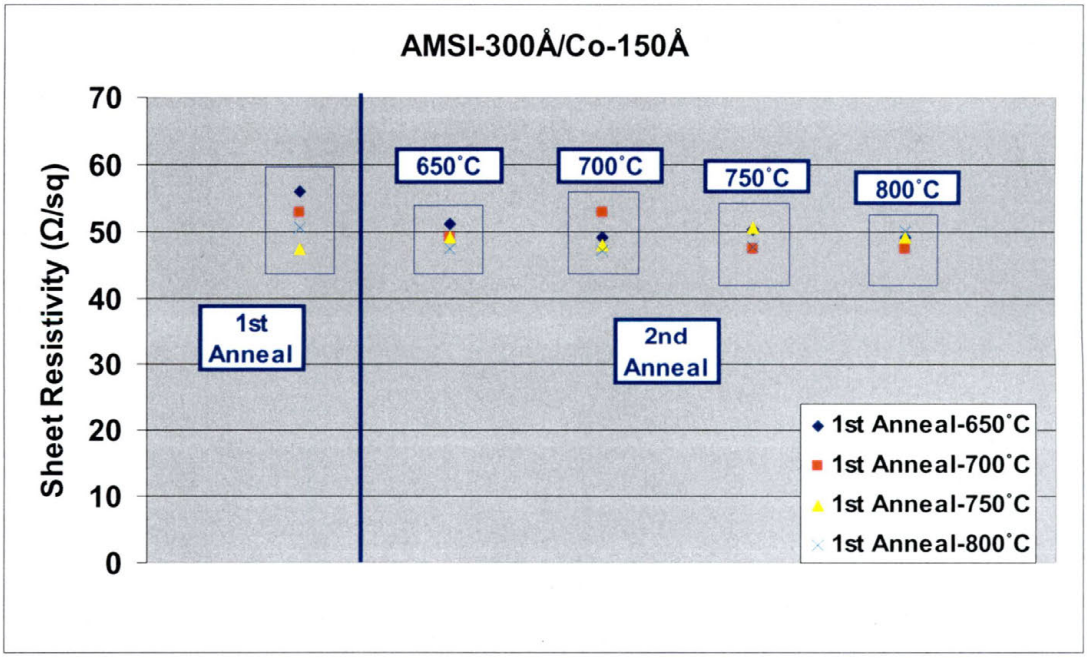

Figure B.12– Rs 3092614 - Wafer# 5-8

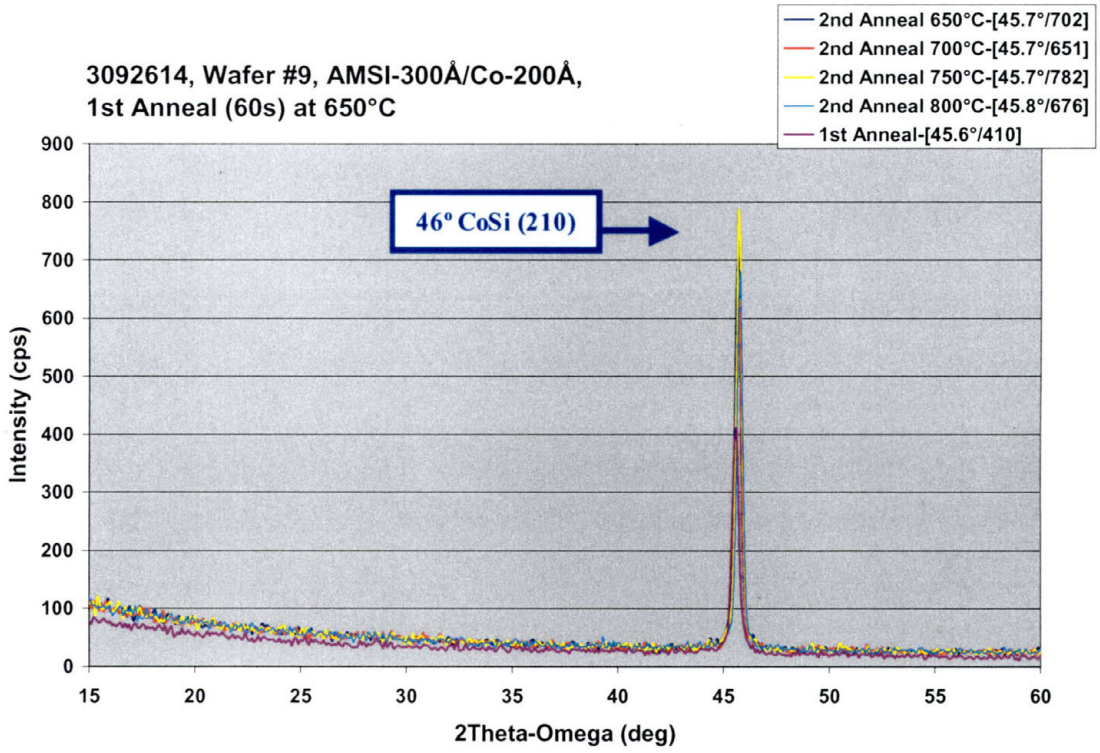

Figure B.13– HAXRD 3092614 - Wafer# 9

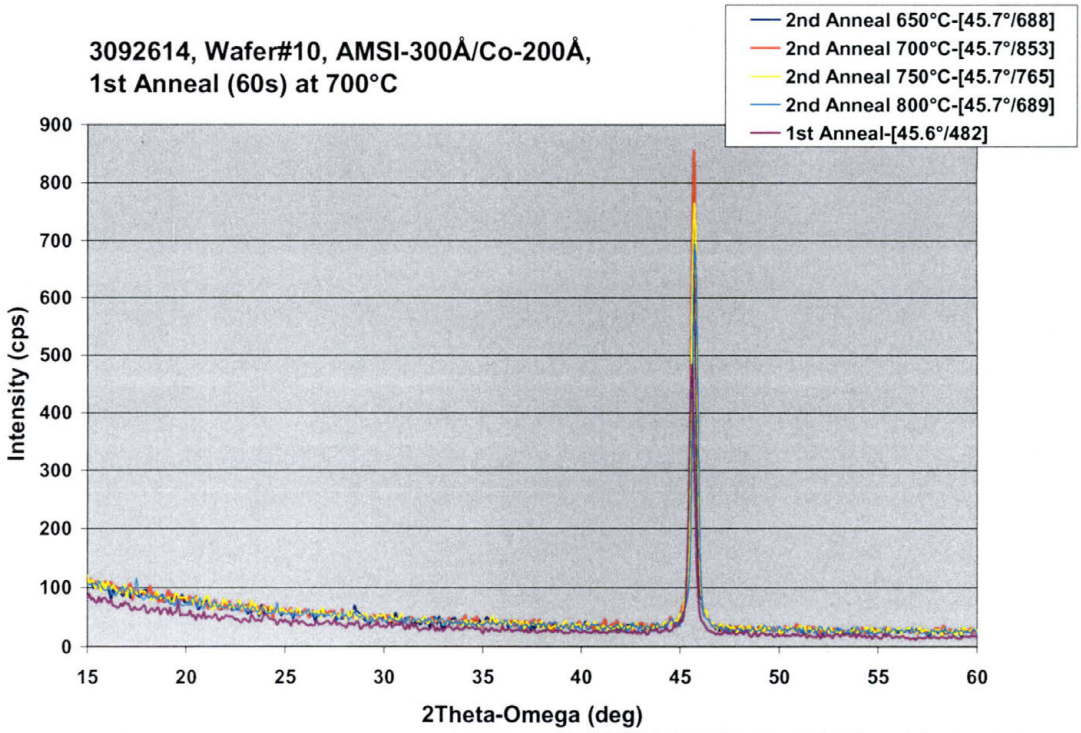

Figure B.14– HAXRD 3092614 - Wafer# 10

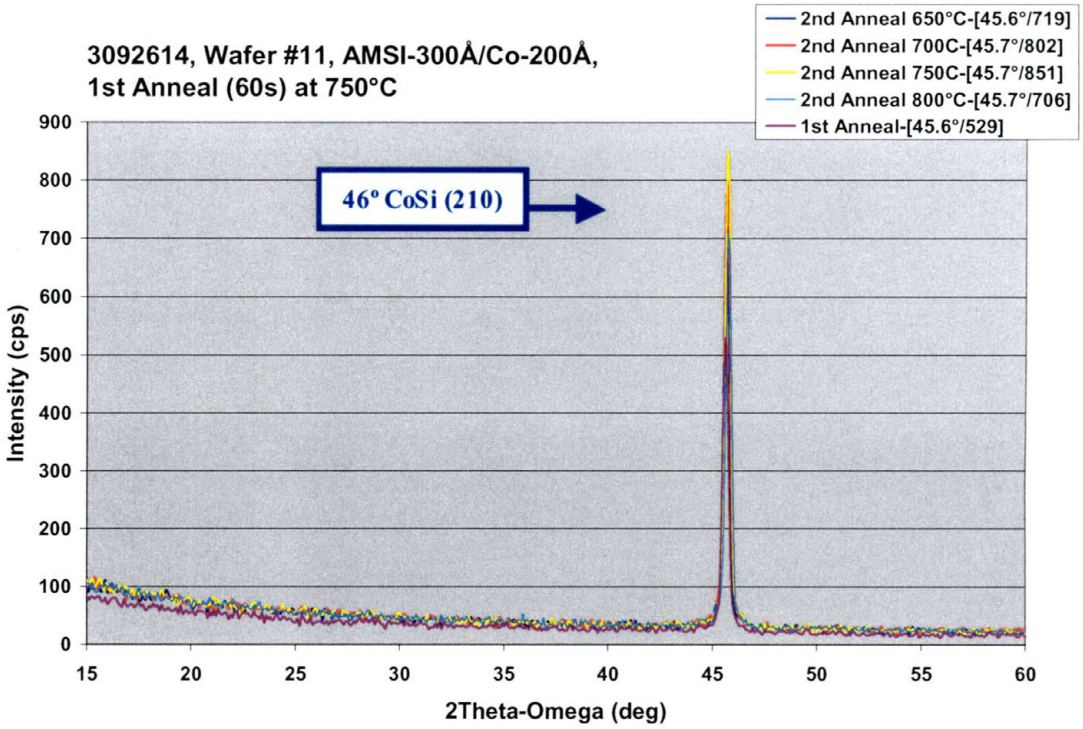

Figure B.15– HAXRD 3092614 - Wafer# 11

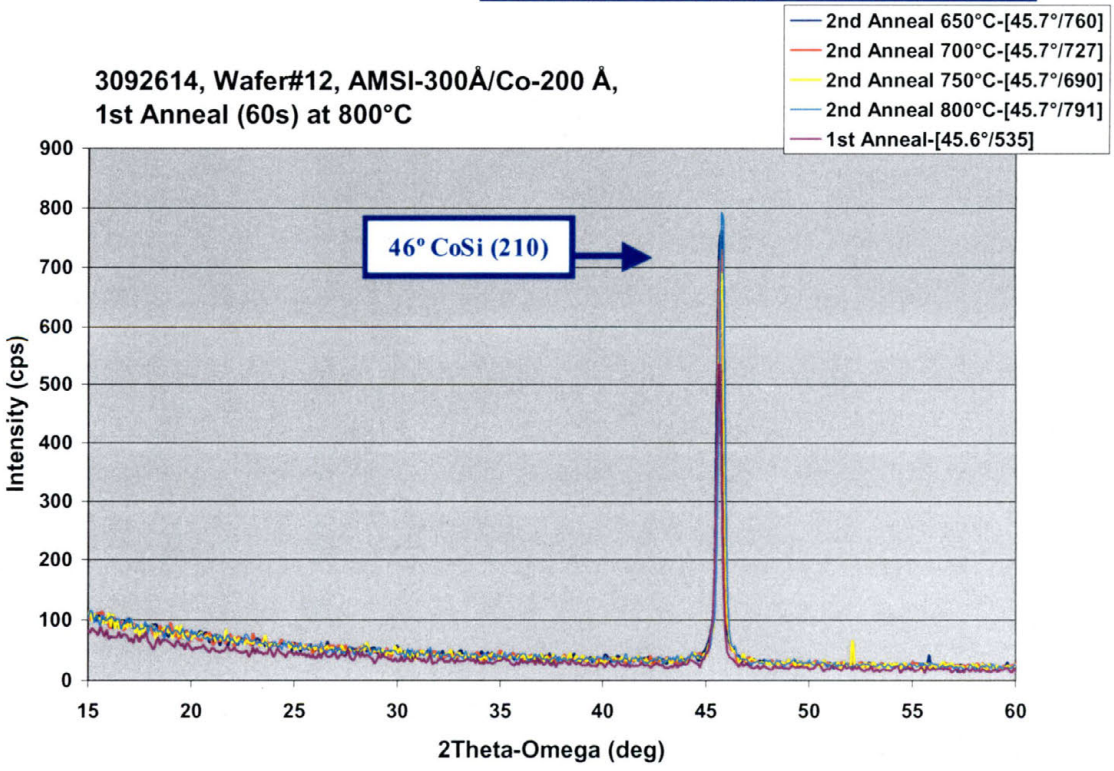

Figure B.16 – HAXRD 3092614 - Wafer# 12

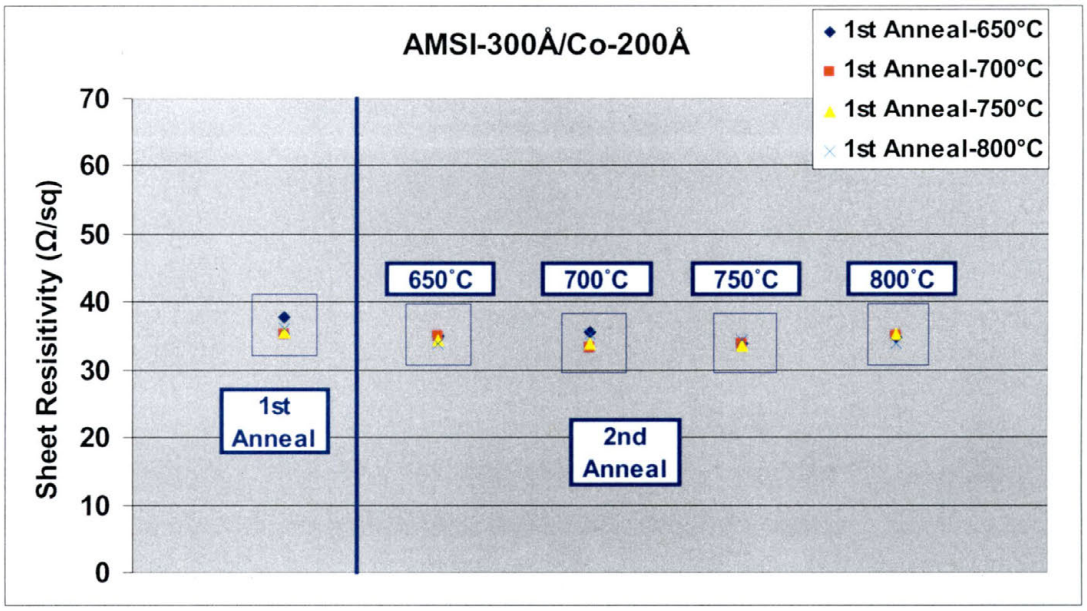

Figure B.17– Rs 3092614 - Wafer# 9-12

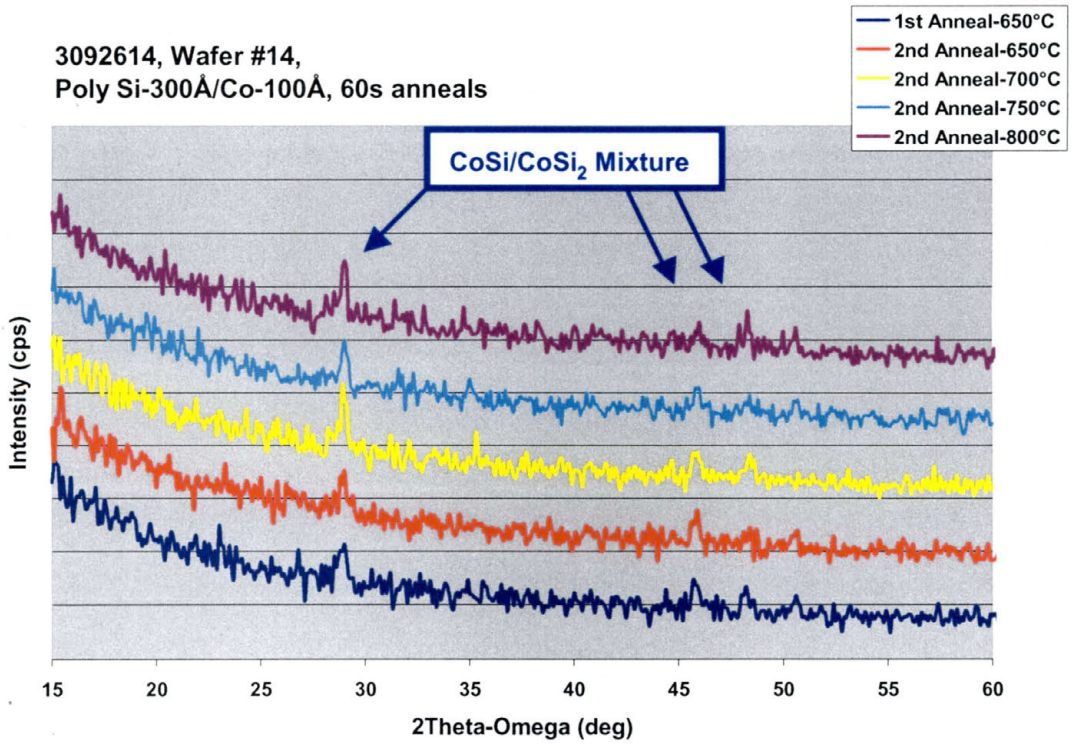

Figure B.18– HAXRD 3092614 - Wafer# 14

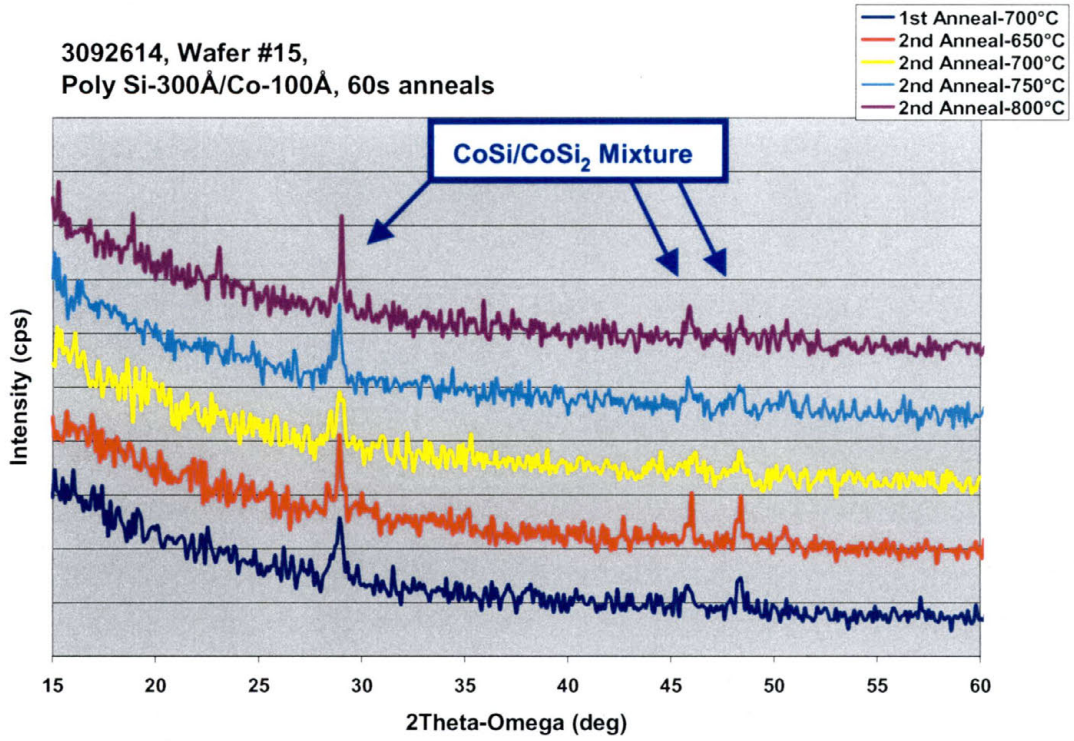

Figure B.19 – HAXRD 3092614 - Wafer# 15

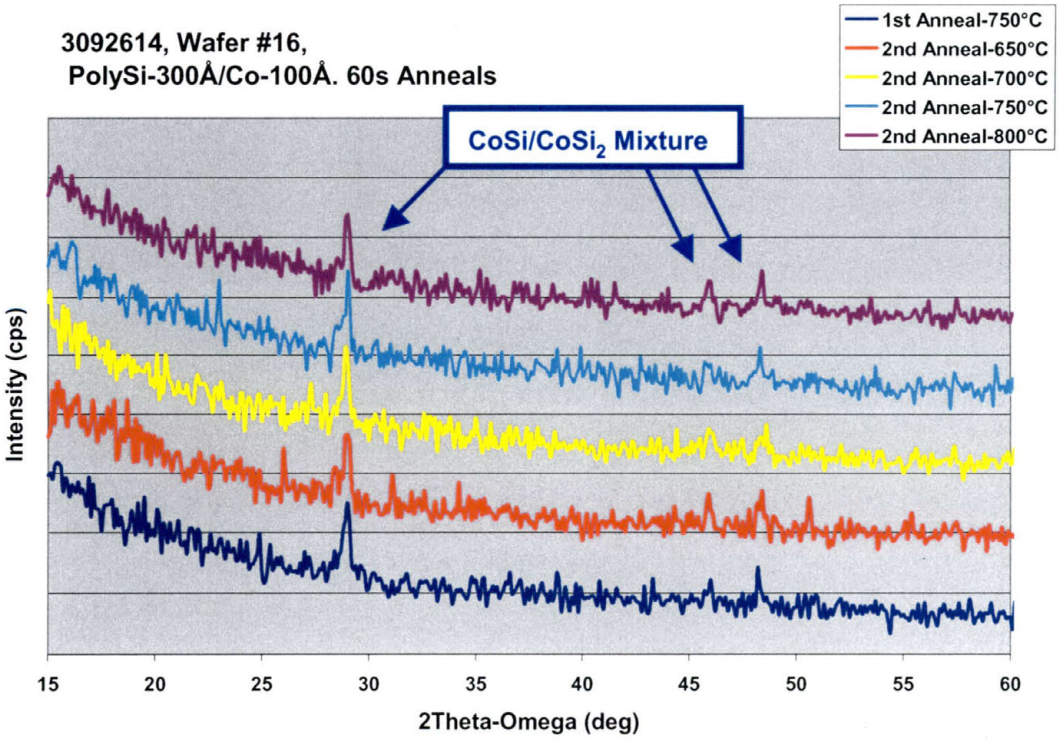

Figure B.20 – HAXRD 3092614 - Wafer# 16

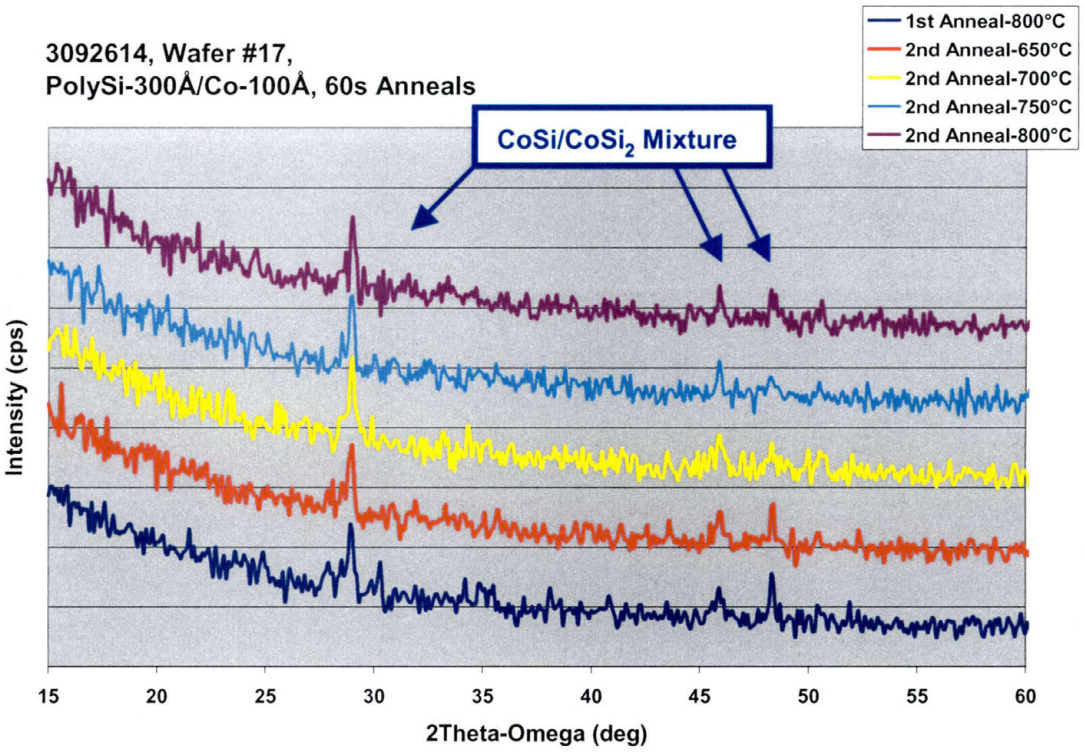

Figure B.21 – HAXRD 3092614 - Wafer# 17

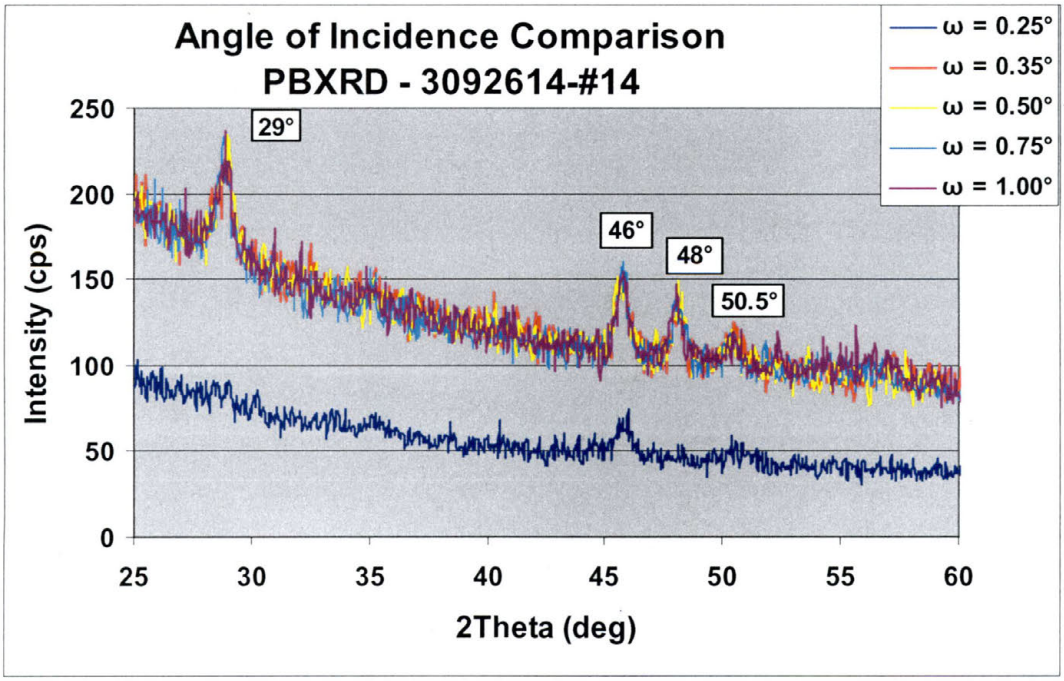

Figure B.22– PBXRD Omega comparison 3092614 - Wafer# 14

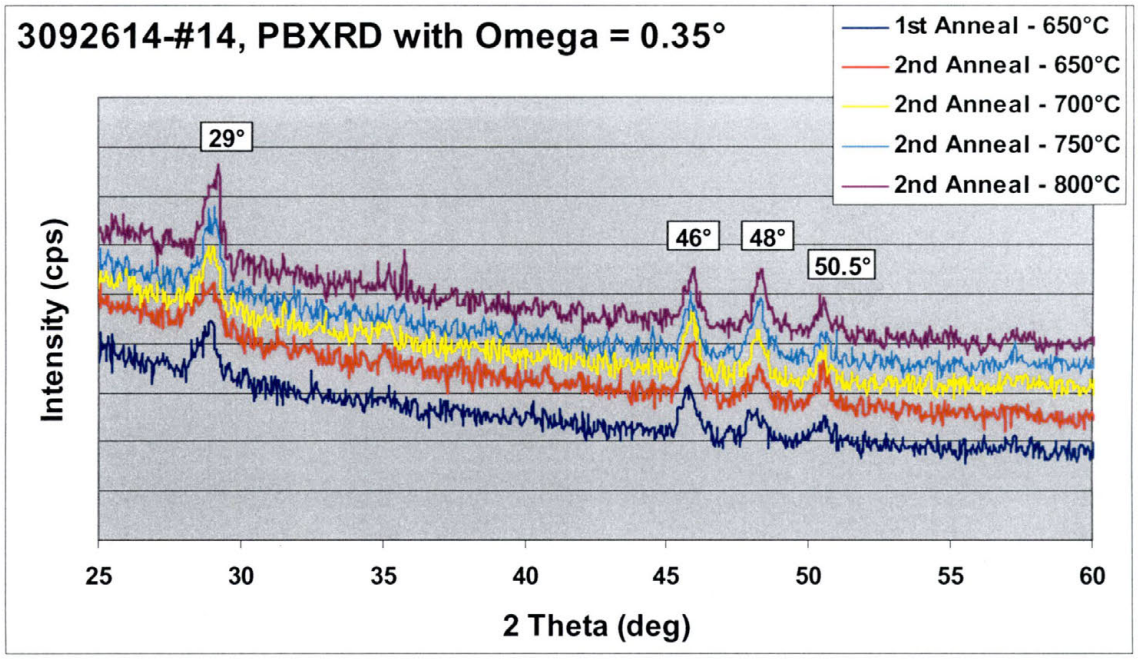

Figure B.23– PBXRD (Omega = 0.35°) 3092614 - Wafer# 14

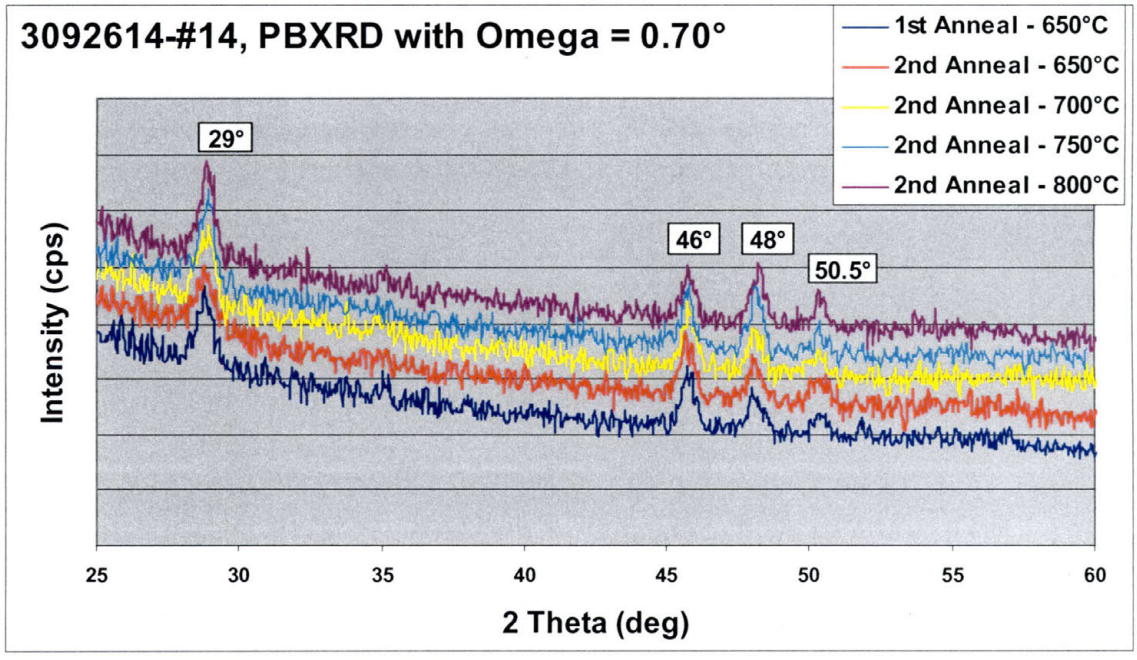

Figure B.24 – PBXRD (Omega = 0.70°) 3092614 - Wafer# 14

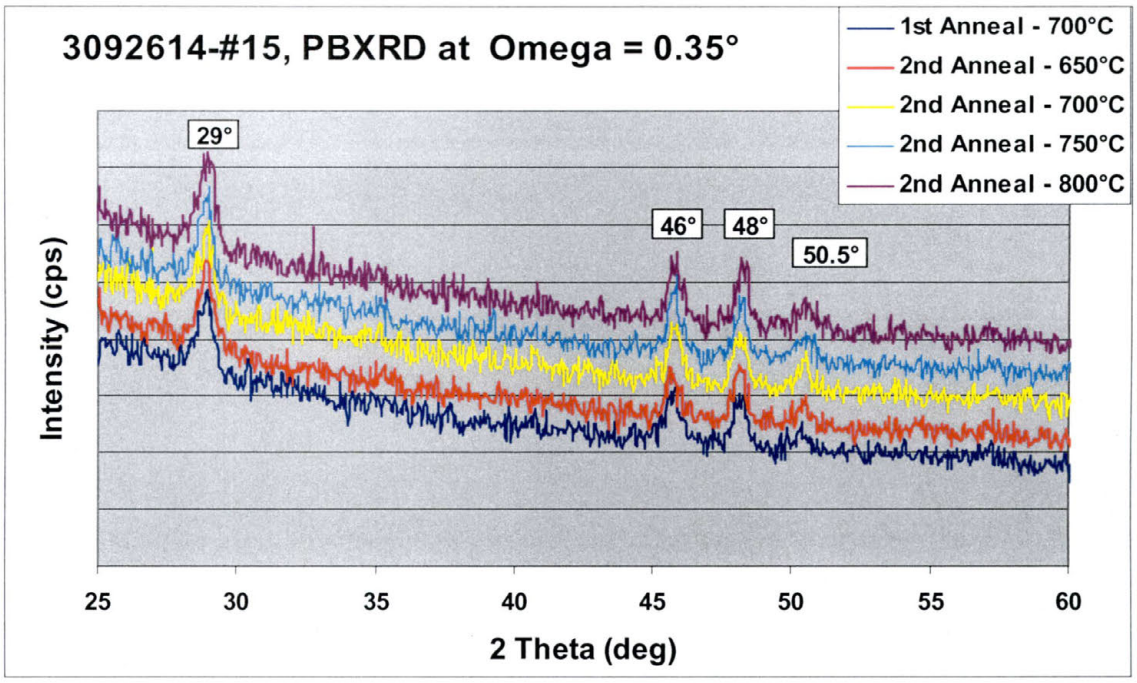

Figure B.25 – PBXRD (Omega = 0.35°) 3092614 - Wafer# 15

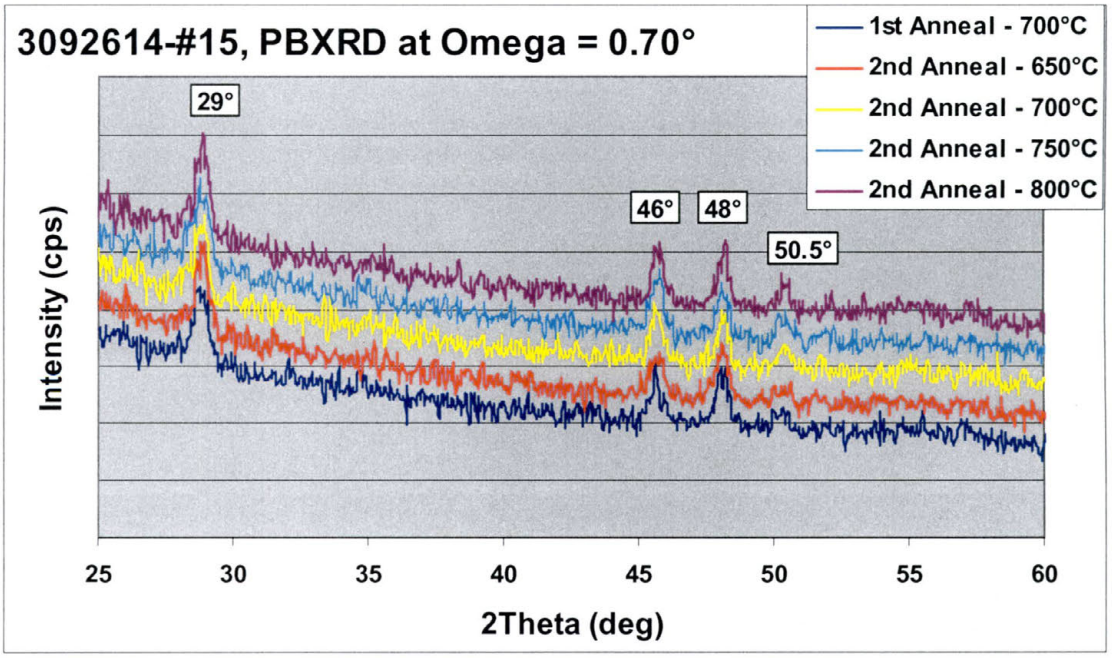

Figure B.26– PBXRD (Omega = 0.70°) 3092614 - Wafer# 15

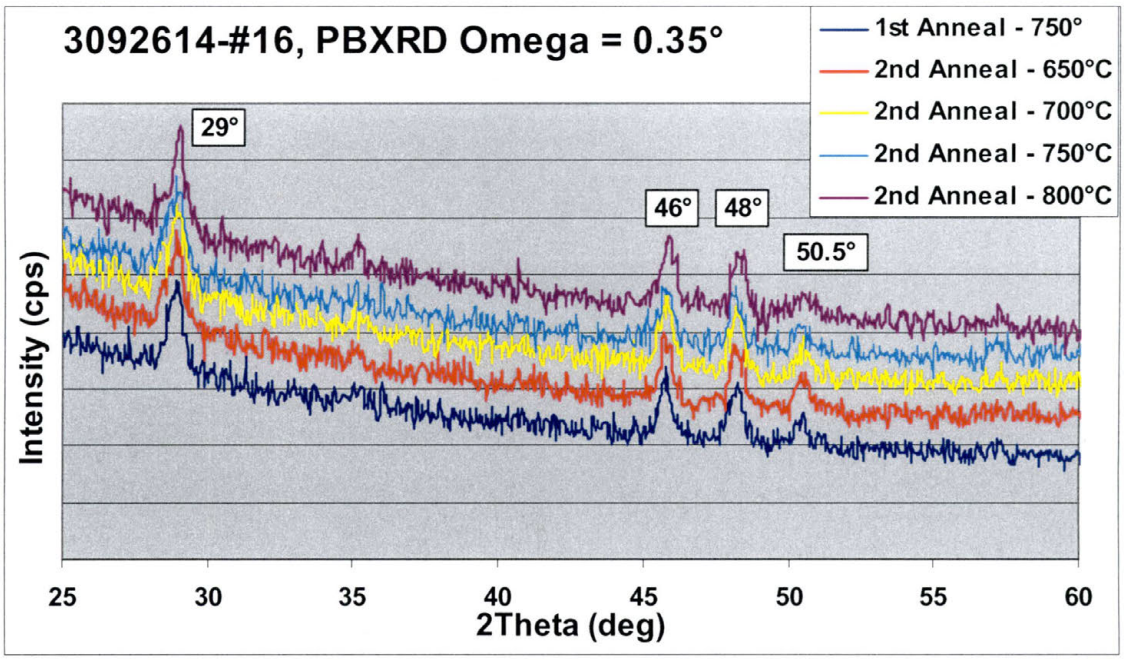

Figure B.27– PBXRD (Omega = 0.35°) 3092614 - Wafer# 16

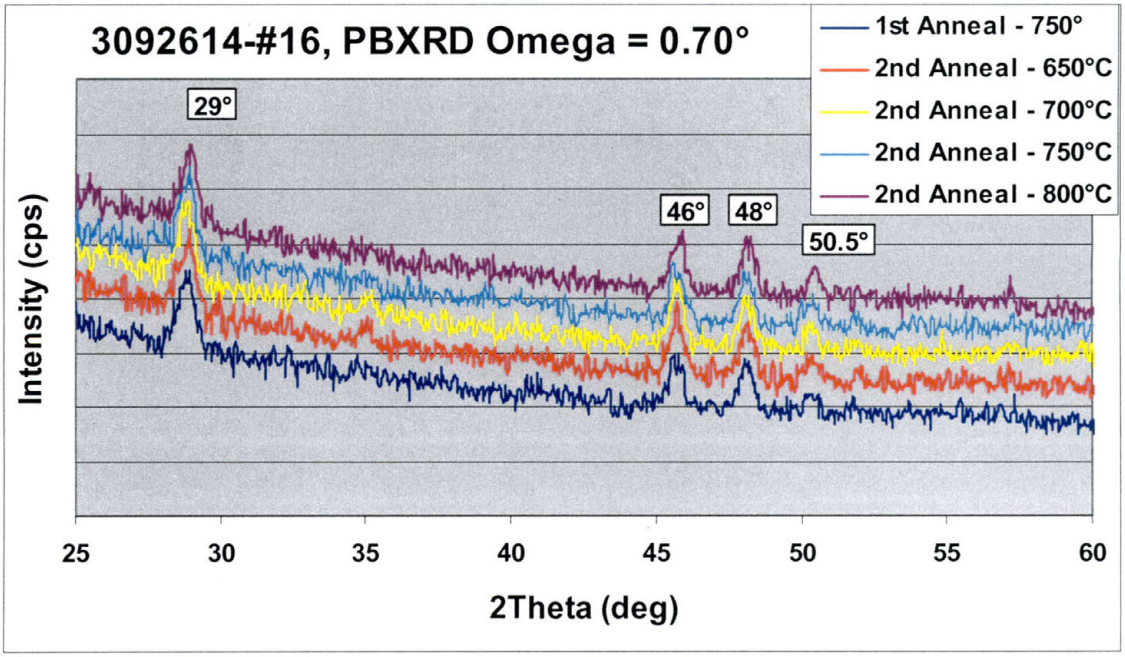

Figure B.28– PBXRD (Omega = 0.70°) 3092614 - Wafer# 16

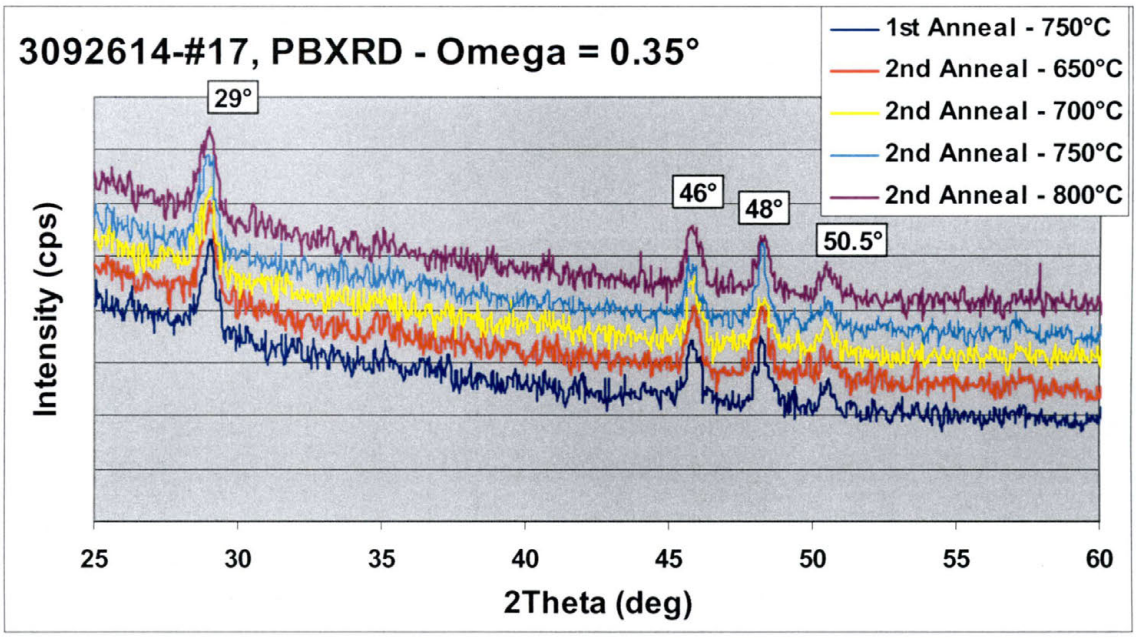

Figure B.29– PBXRD (Omega = 0.35°) 3092614 - Wafer# 17

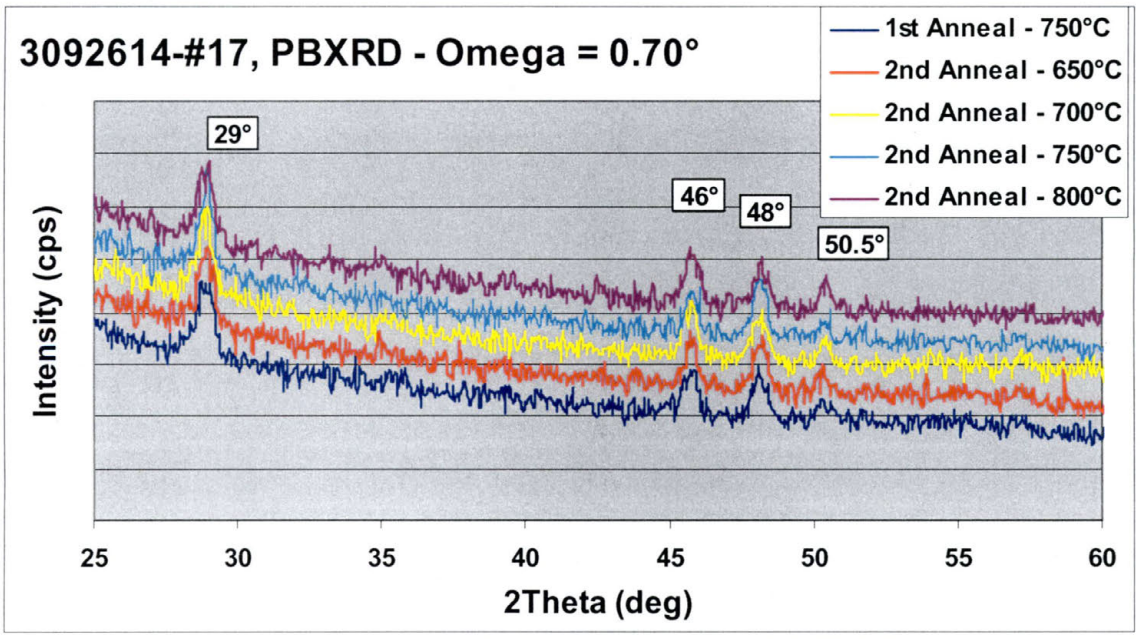

Figure B.30– PBXRD (Omega = 0.70°) 3092614 - Wafer# 17

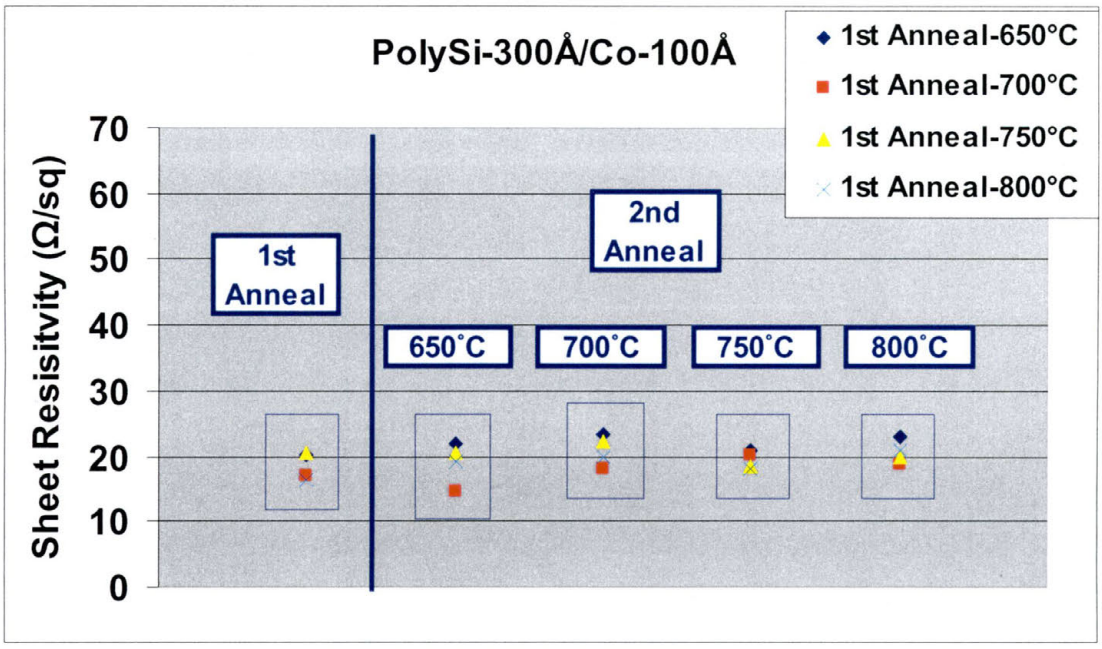

Figure B.31– Rs 3092614 - Wafer# 14-17

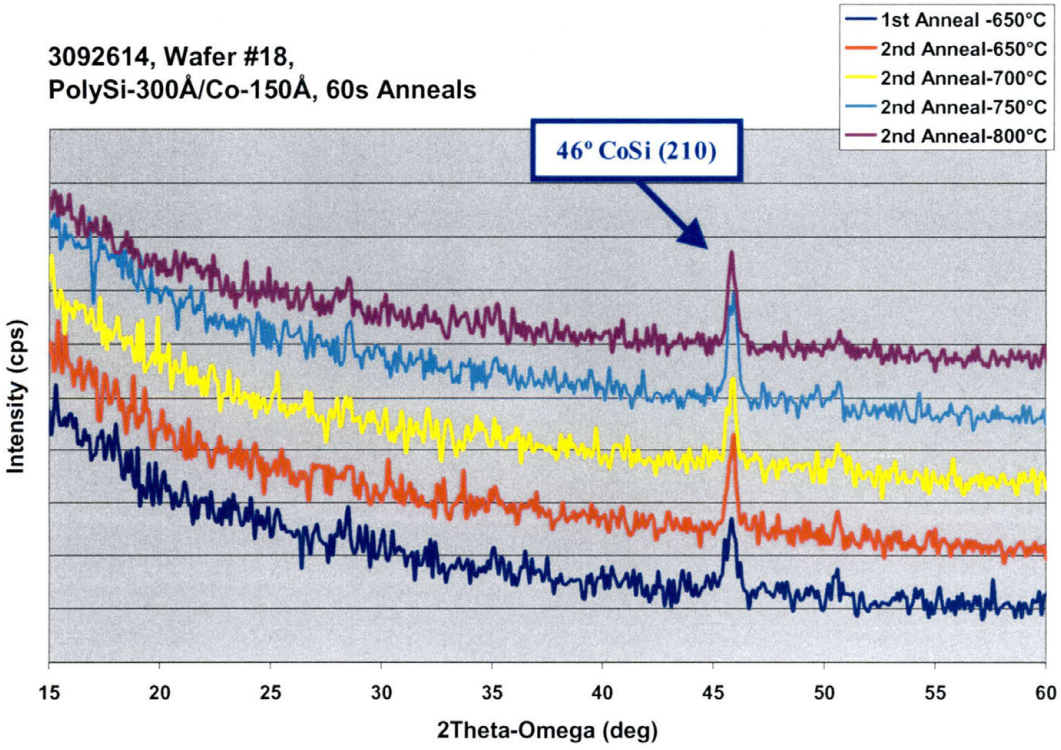

Figure B.32 - HAXRD 3092614 - Wafer# 18

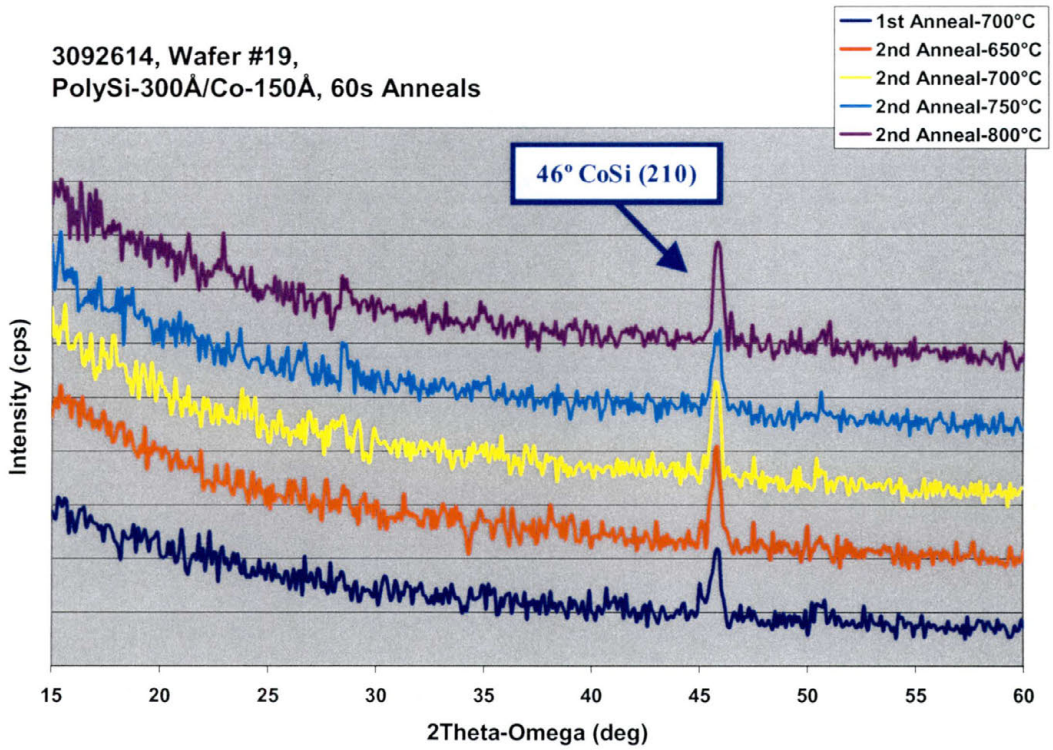

Figure B.33 - HAXRD 3092614 - Wafer# 19

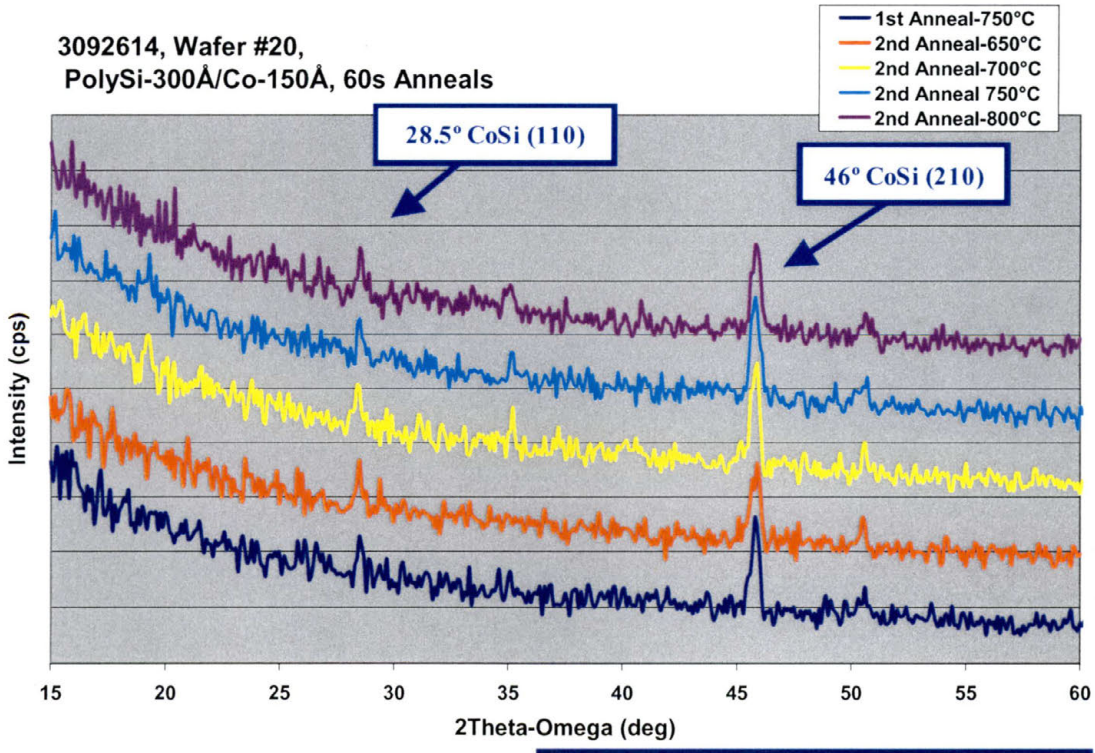

Figure B.34 - HAXRD 3092614 - Wafer# 20

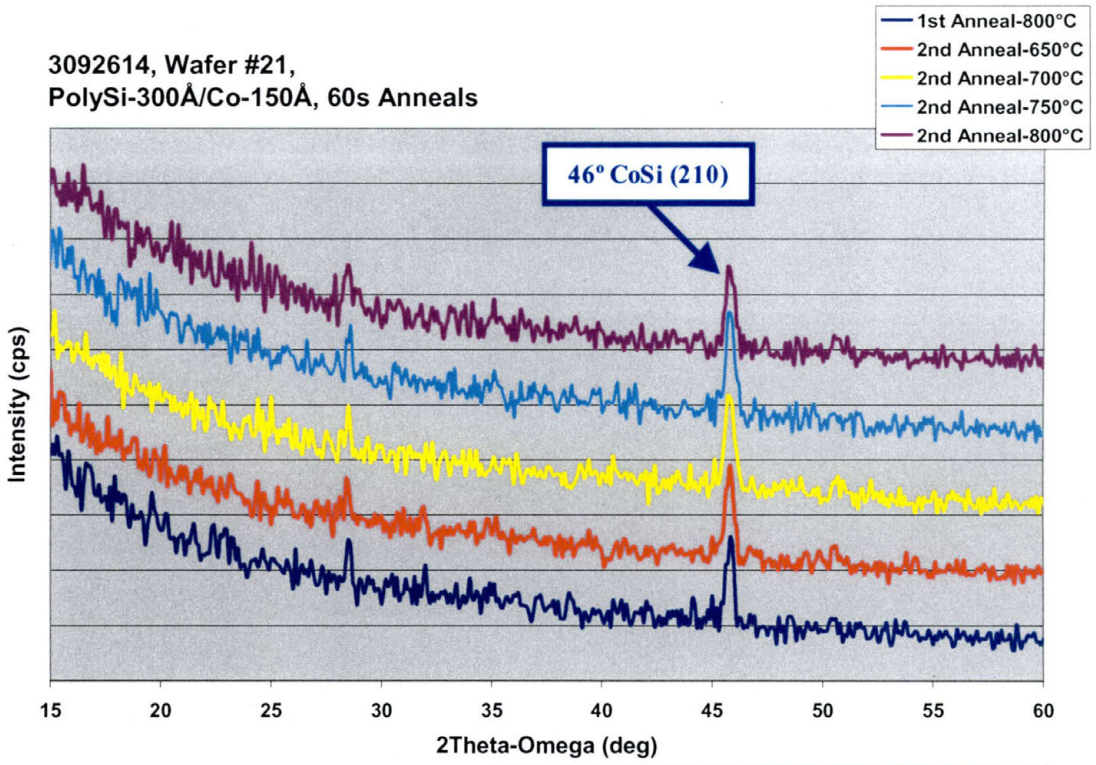

Figure B.35 - HAXRD 3092614 - Wafer# 21

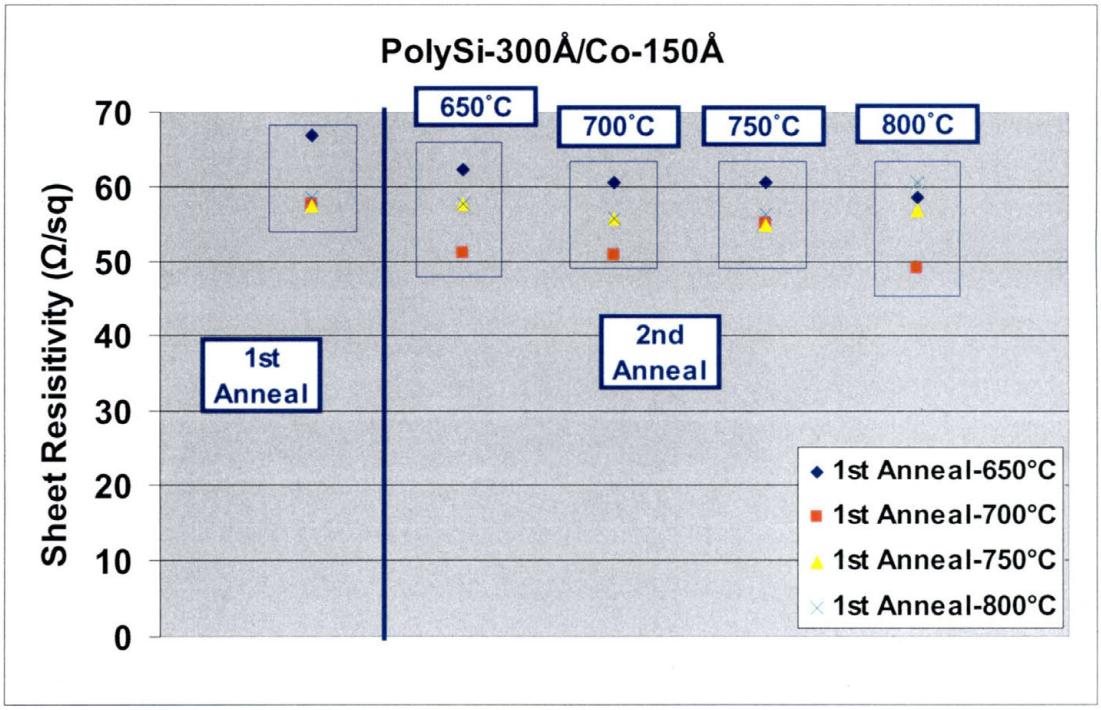

Figure B.36– Rs 3092614 - Wafer# 18-21

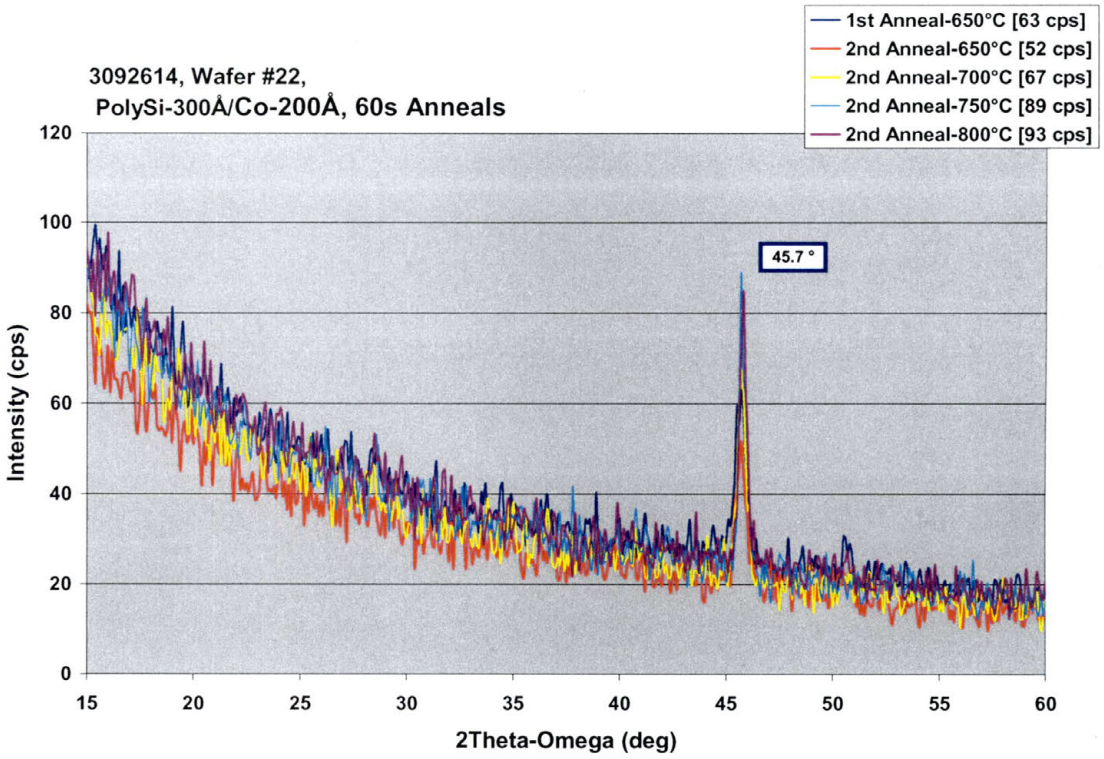

Figure B.37 - HAXRD 3092614 - Wafer# 22

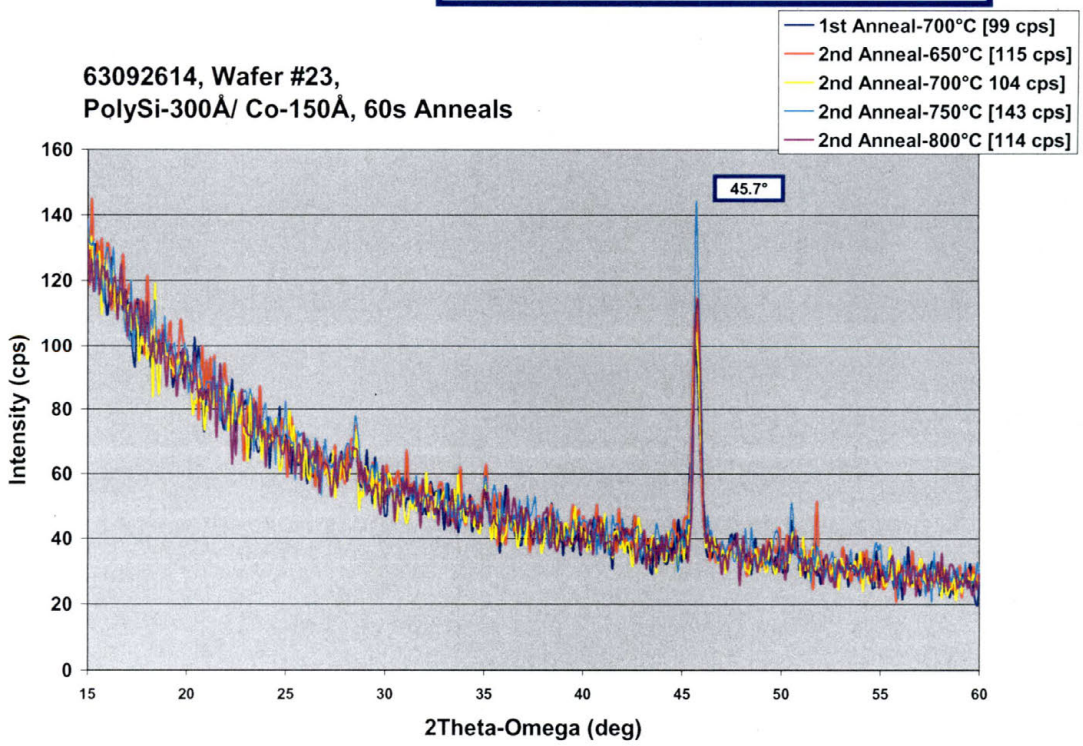

Figure B.38 - HAXRD 3092614 - Wafer# 23

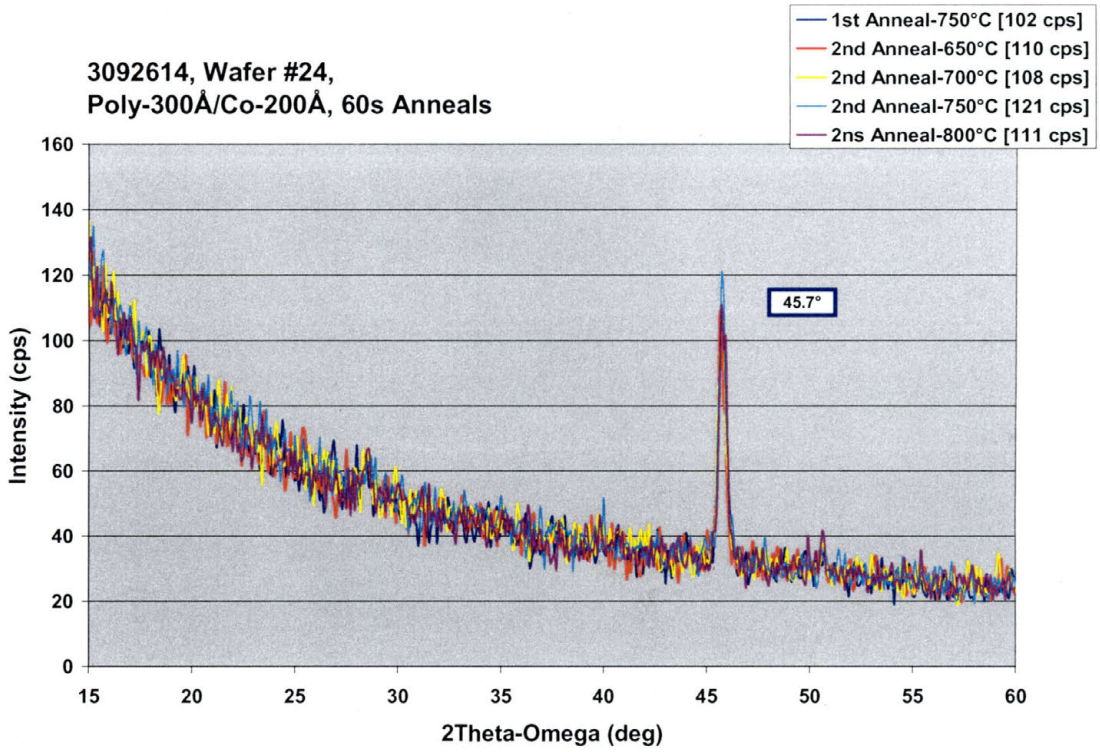

Figure B.39 - HAXRD 3092614 - Wafer# 24

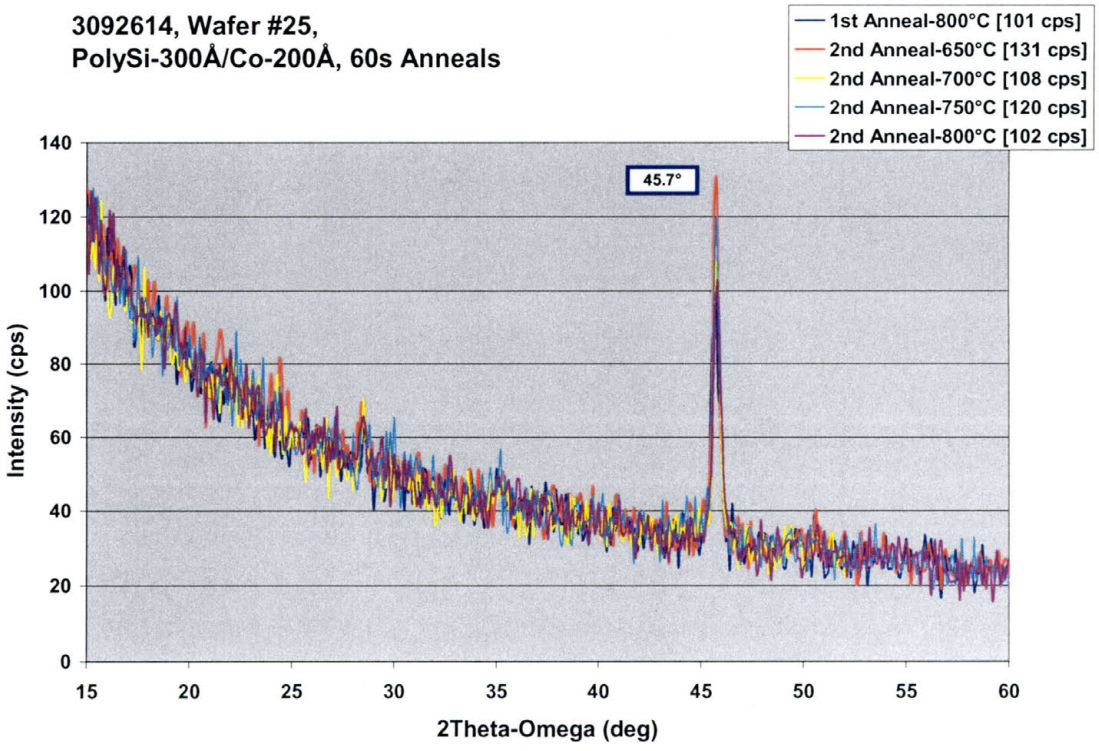

Figure B.40 - HAXRD 3092614 - Wafer# 25

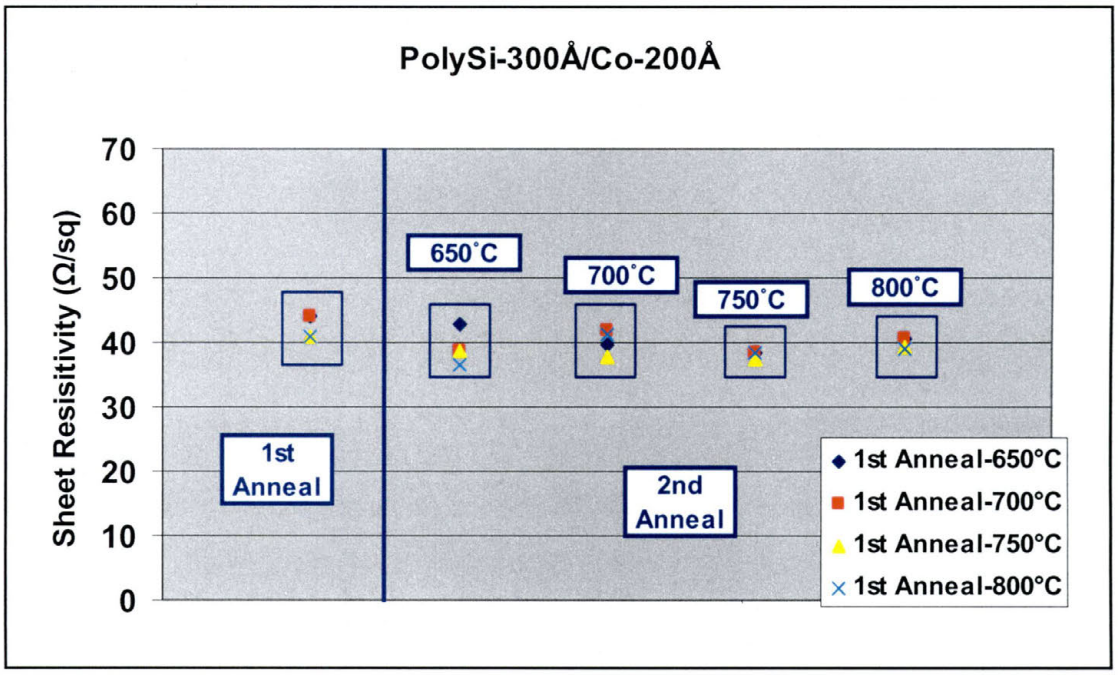

Figure B.41– Rs 3092614 - Wafer# 22-25

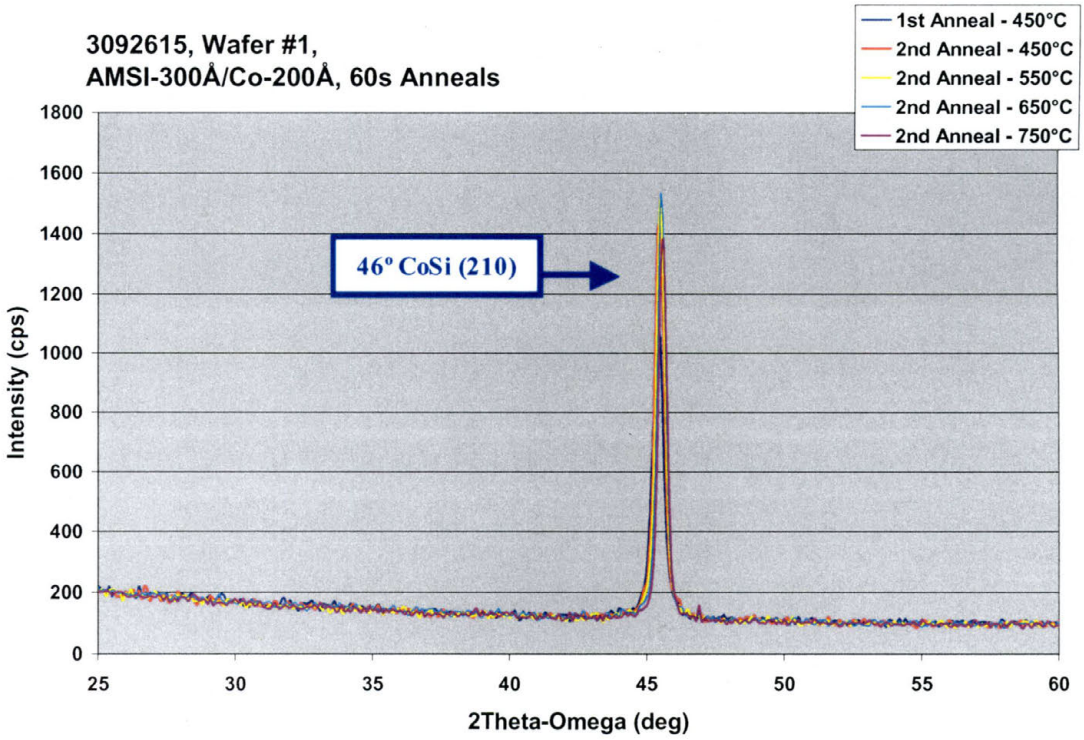

Figure B.42- HAXRD 3092615 - Wafer# 1

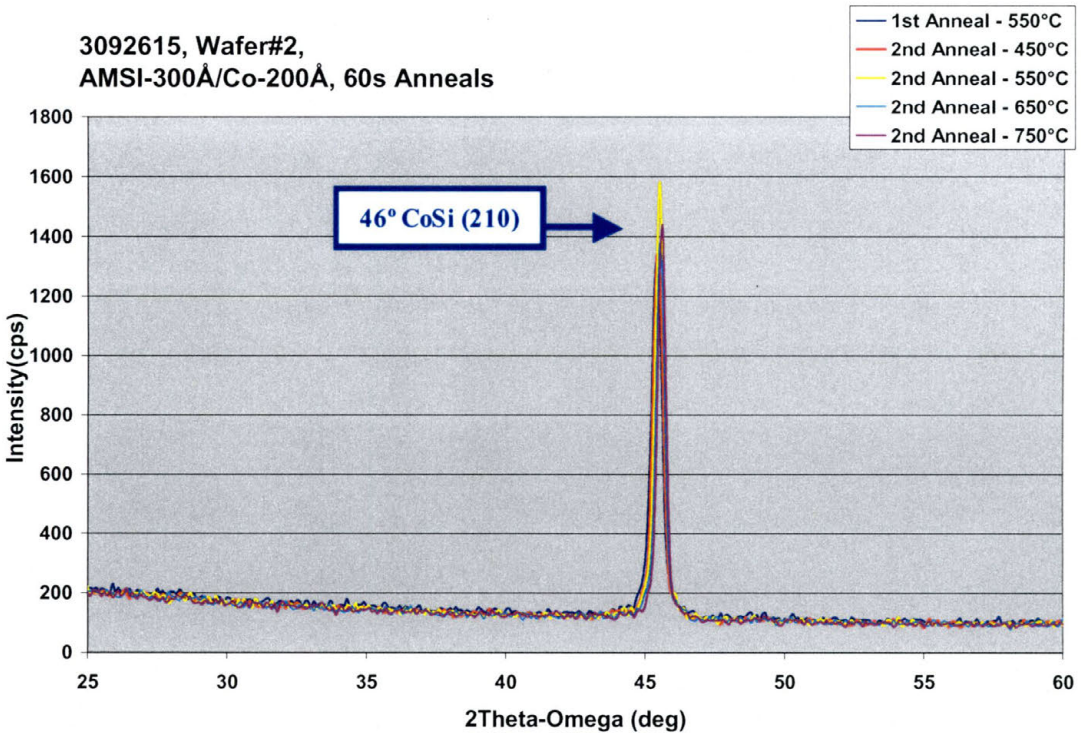

Figure B.43 - HAXRD 3092615 - Wafer# 2

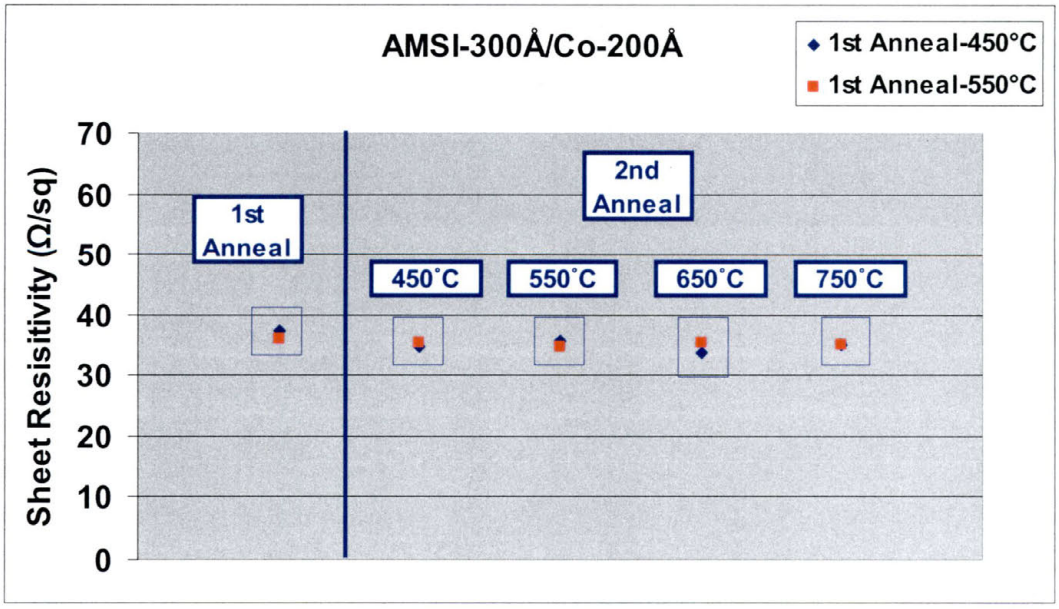

Figure B.44 – Rs 3092615 - Wafer# 1-2

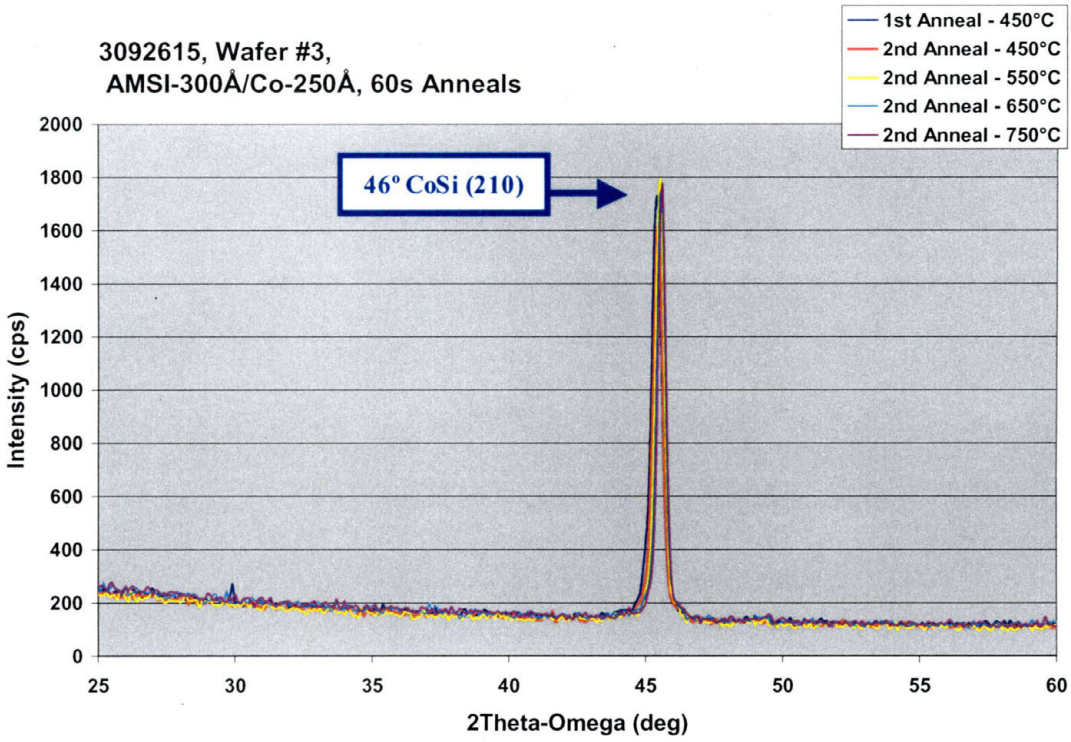

Figure B.45 - HAXRD 3092615 - Wafer# 3

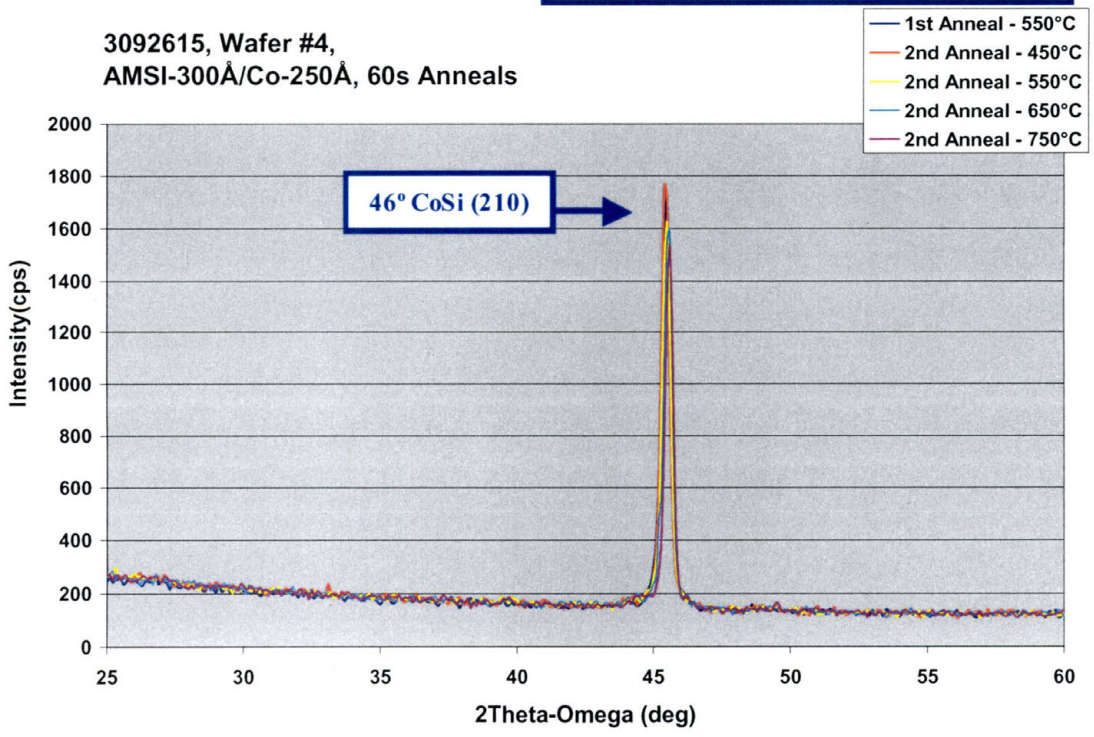

Figure B.46 - HAXRD 3092615 - Wafer# 4

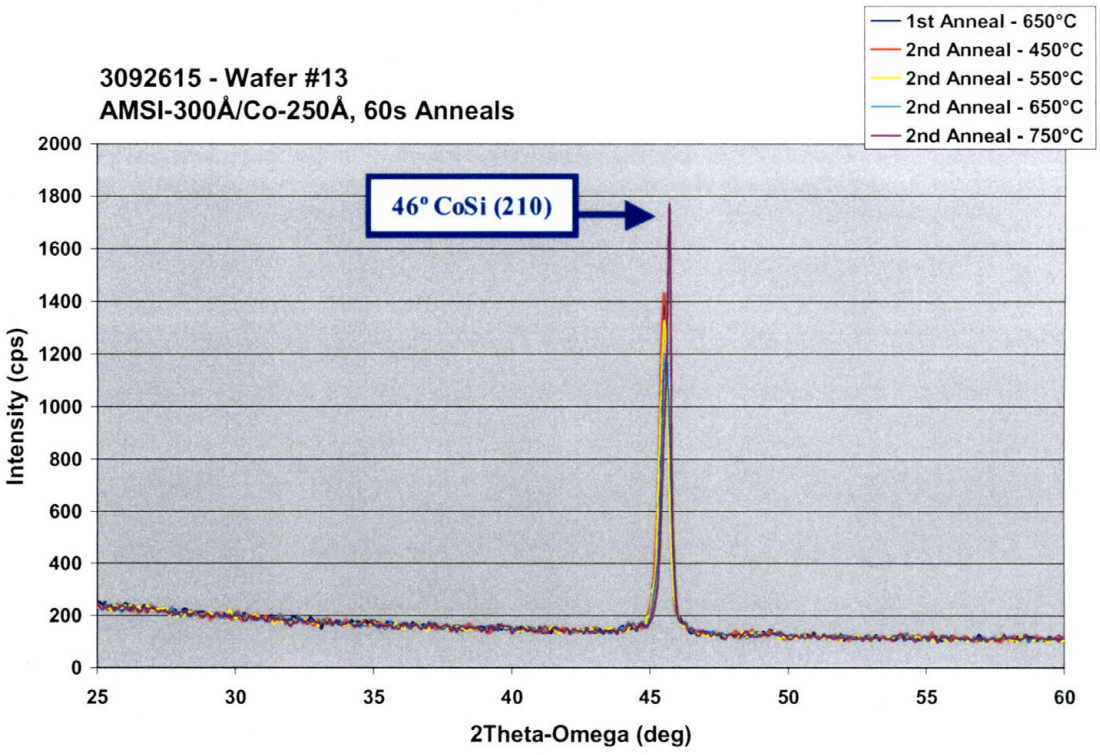

Figure B.47 - HAXRD 3092615 - Wafer# 13

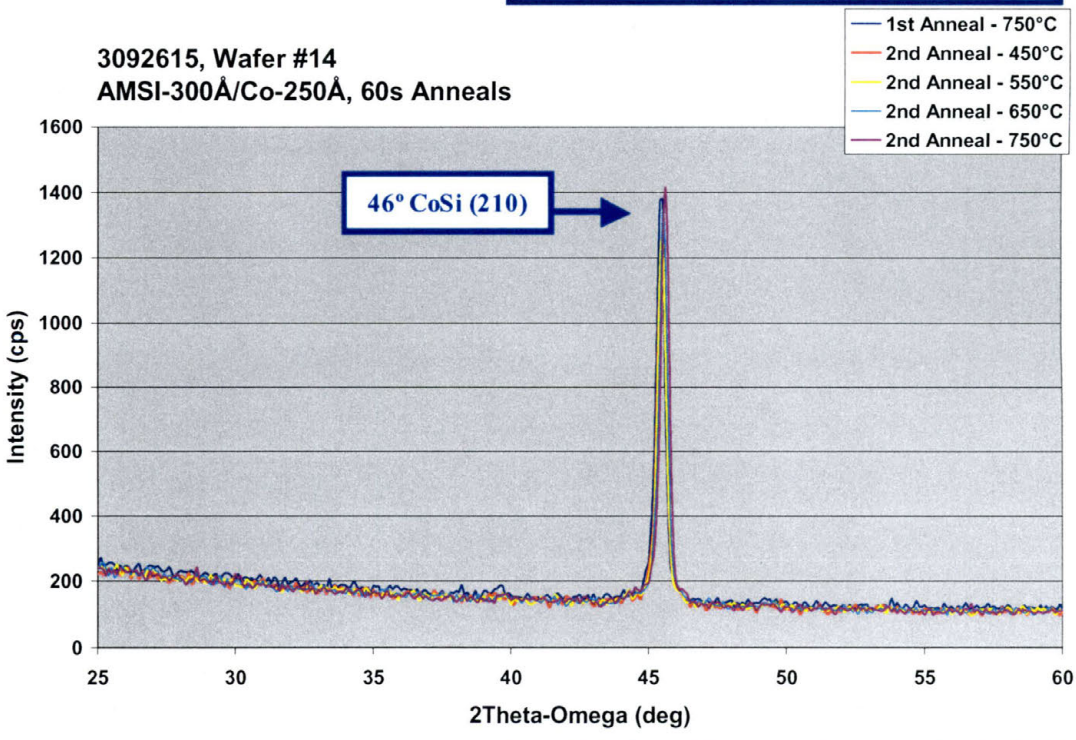

Figure B.48 - HAXRD 3092615 - Wafer# 14

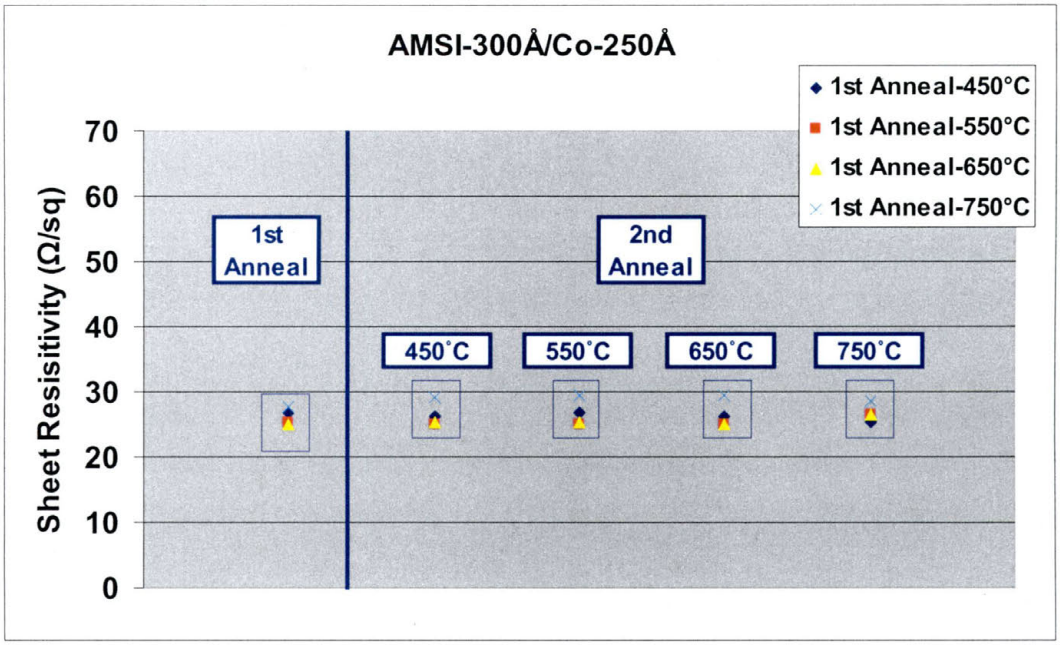

Figure B.49 – Rs 3092615 - Wafer# 3, 4, 13, & 14

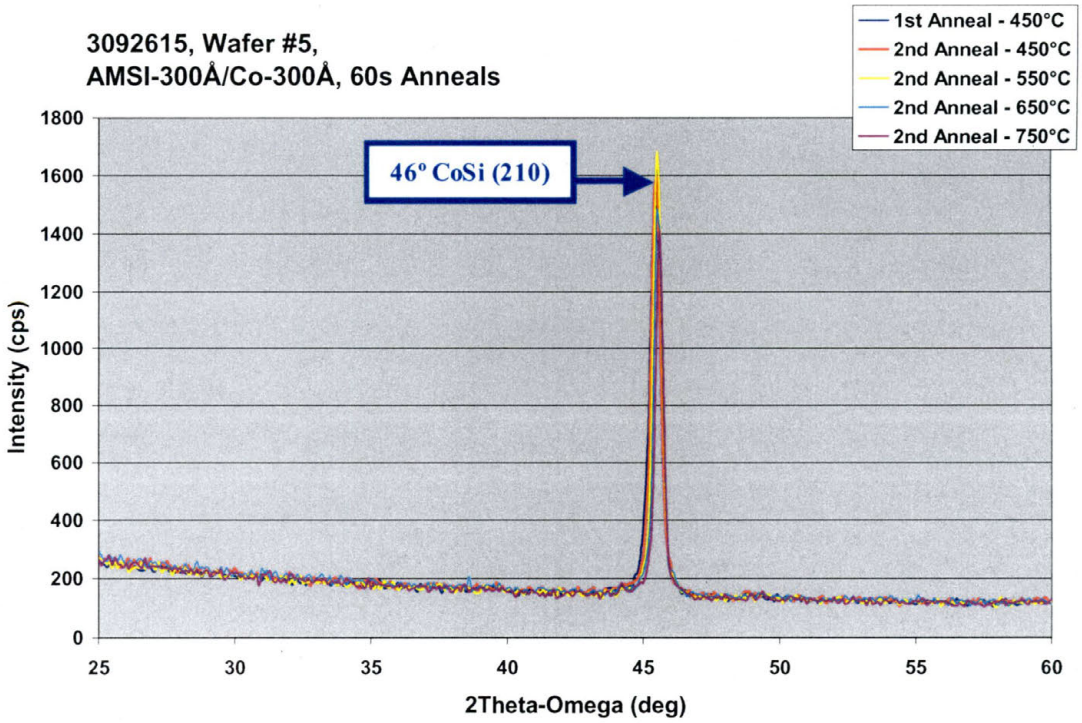

Figure B.50 - HAXRD 3092615 - Wafer# 5

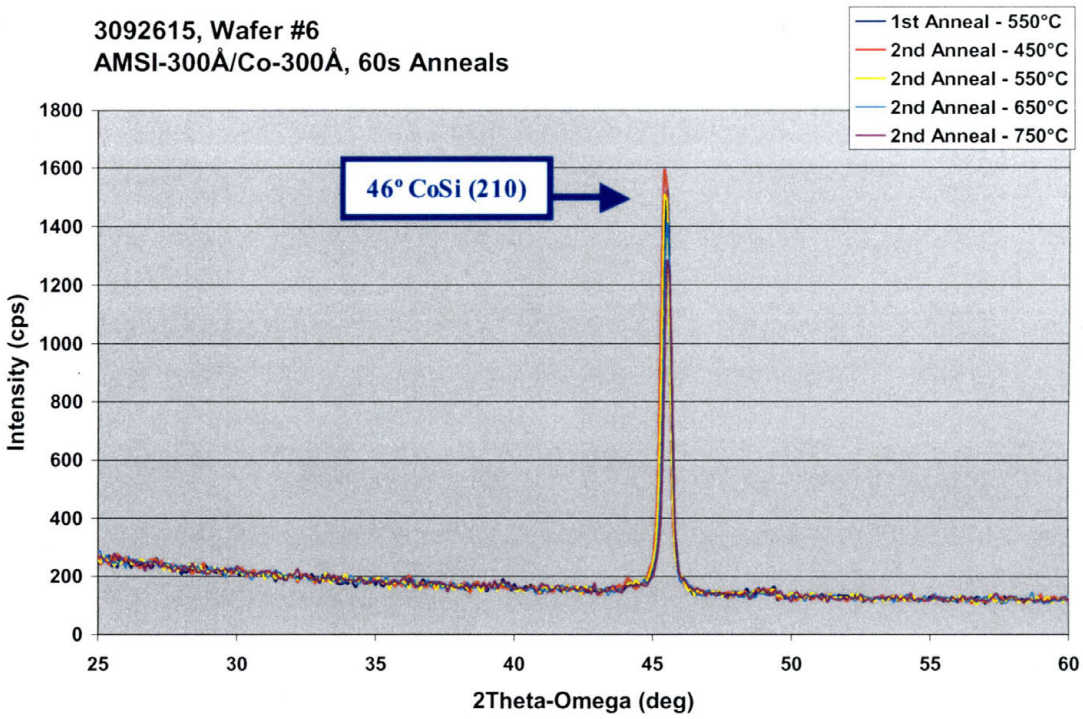

Figure B.51 - HAXRD 3092615 - Wafer# 6

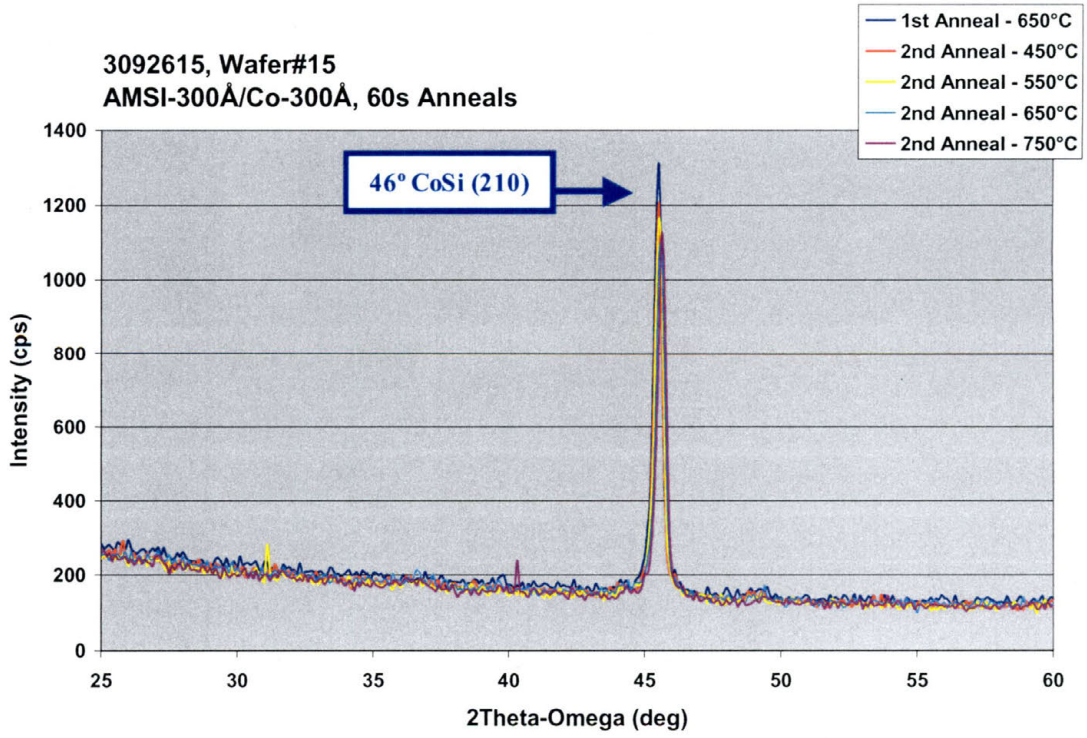

Figure B.52 - HAXRD 3092615 - Wafer# 15

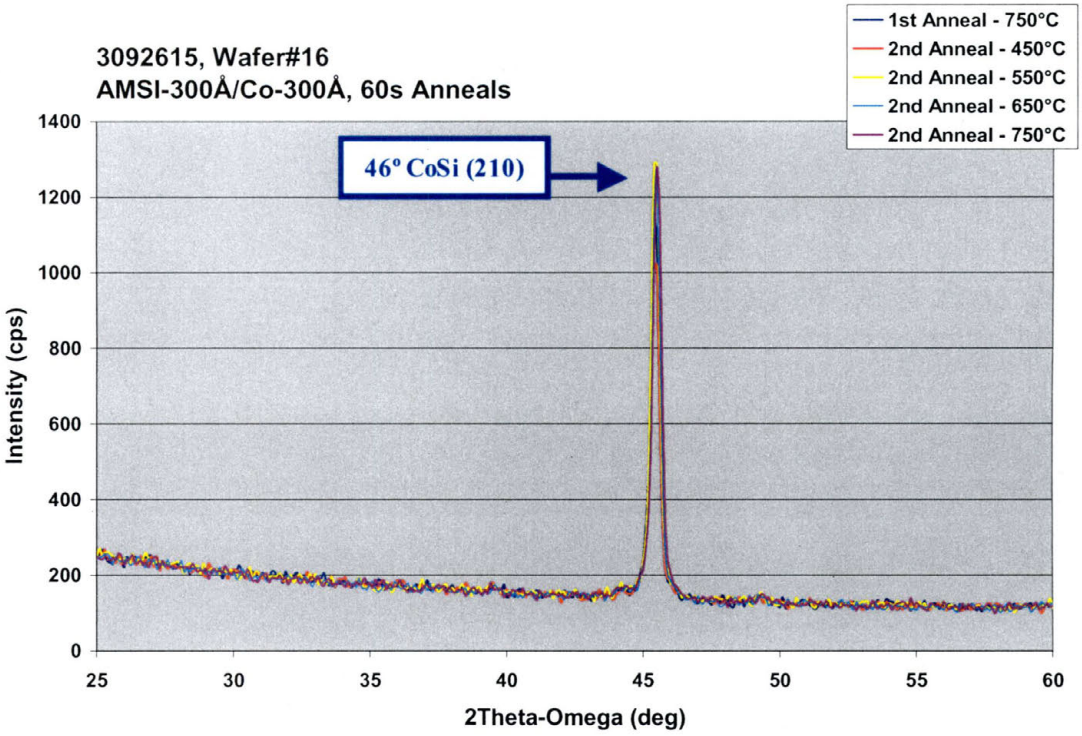

Figure B.53 - HAXRD 3092615 - Wafer# 16

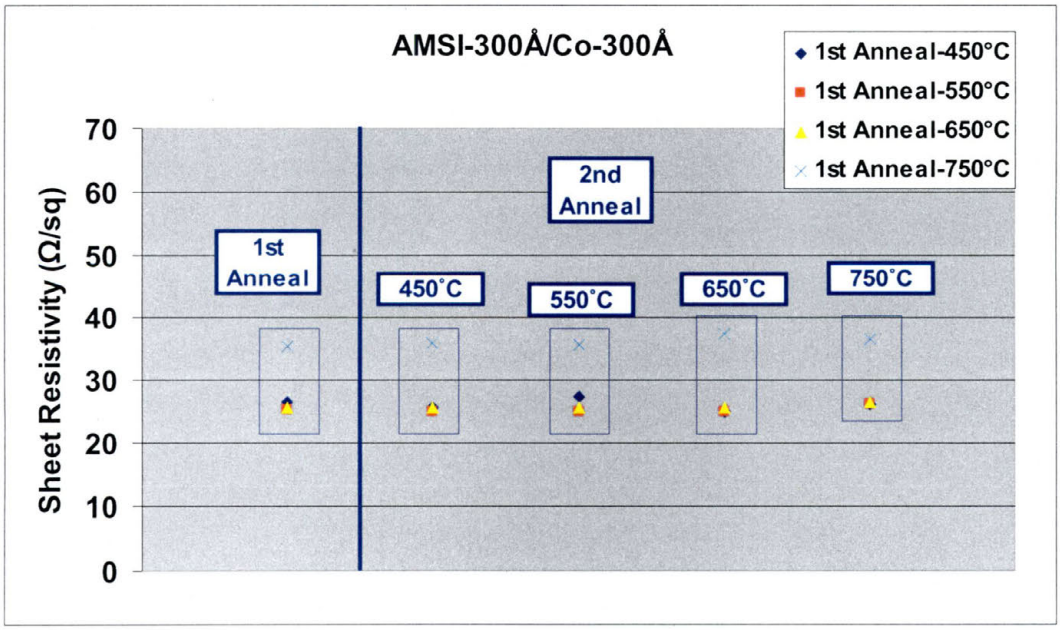

Figure B.54 – Rs 3092615 - Wafer# 5, 6, 15, & 16

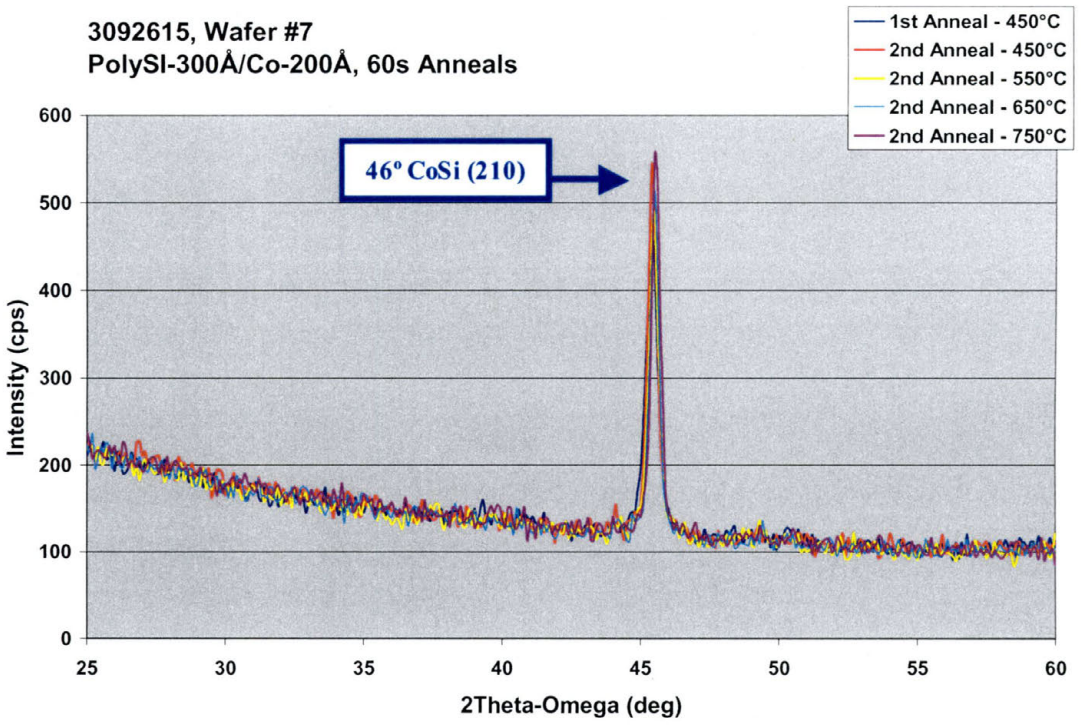

Figure B.55 - HAXRD 3092615 - Wafer# 7

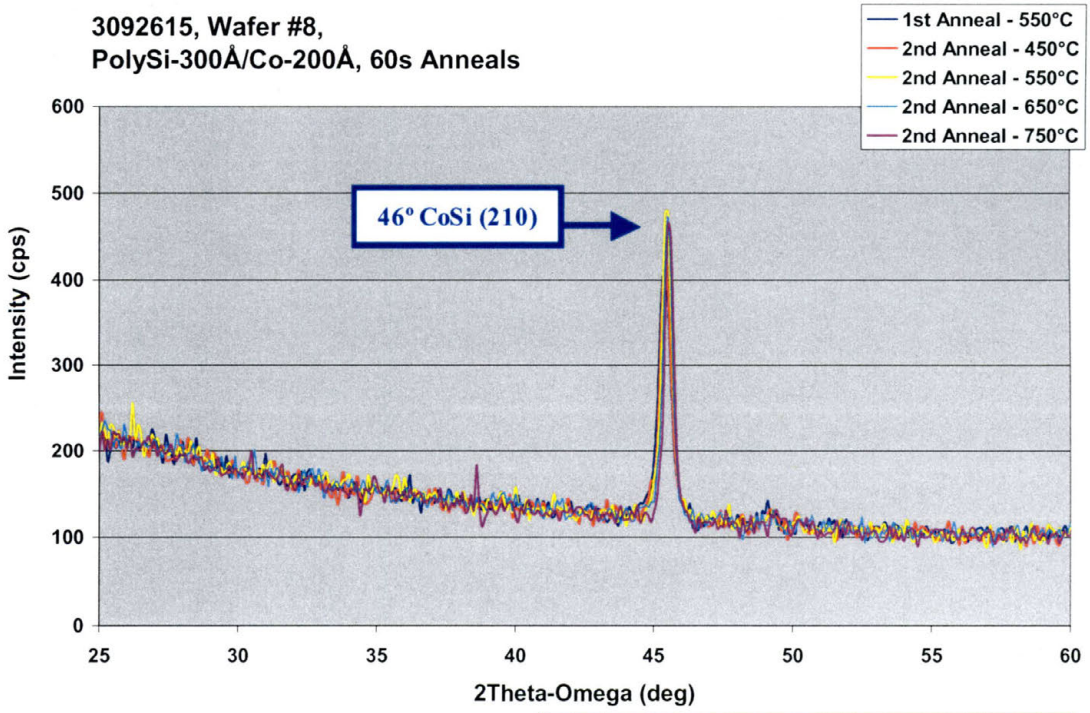

Figure B.56 - HAXRD 3092615 - Wafer# 8

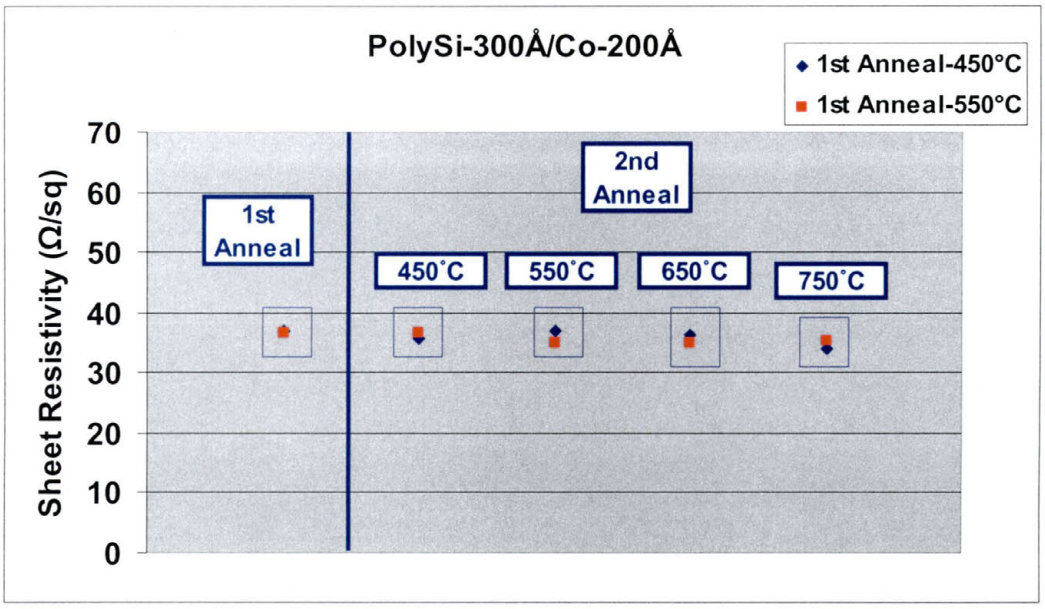

Figure B.57– Rs 3092615 - Wafer# 7-8

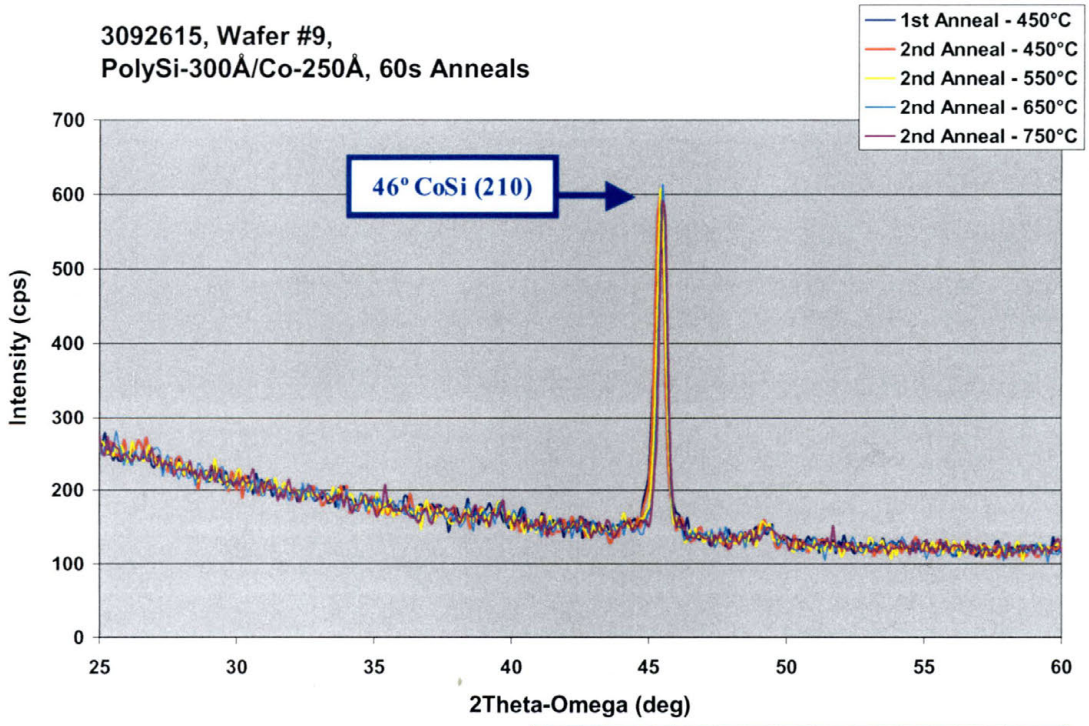

Figure B.58 - HAXRD 3092615 - Wafer# 9

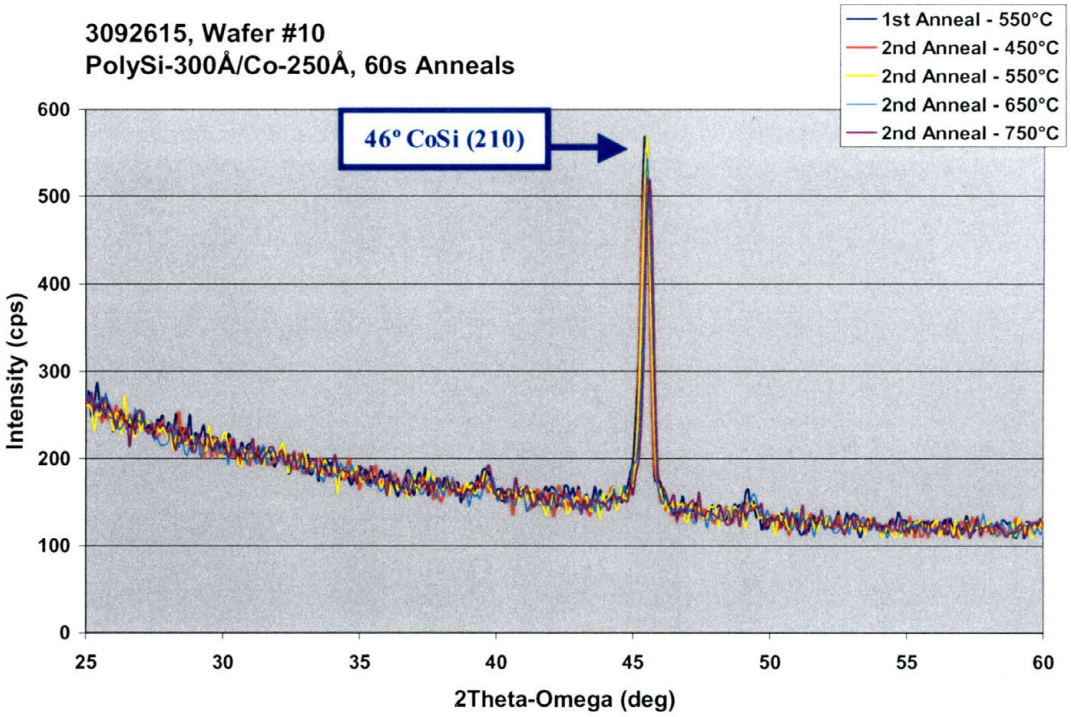

Figure B.59 - HAXRD 3092615 - Wafer# 10

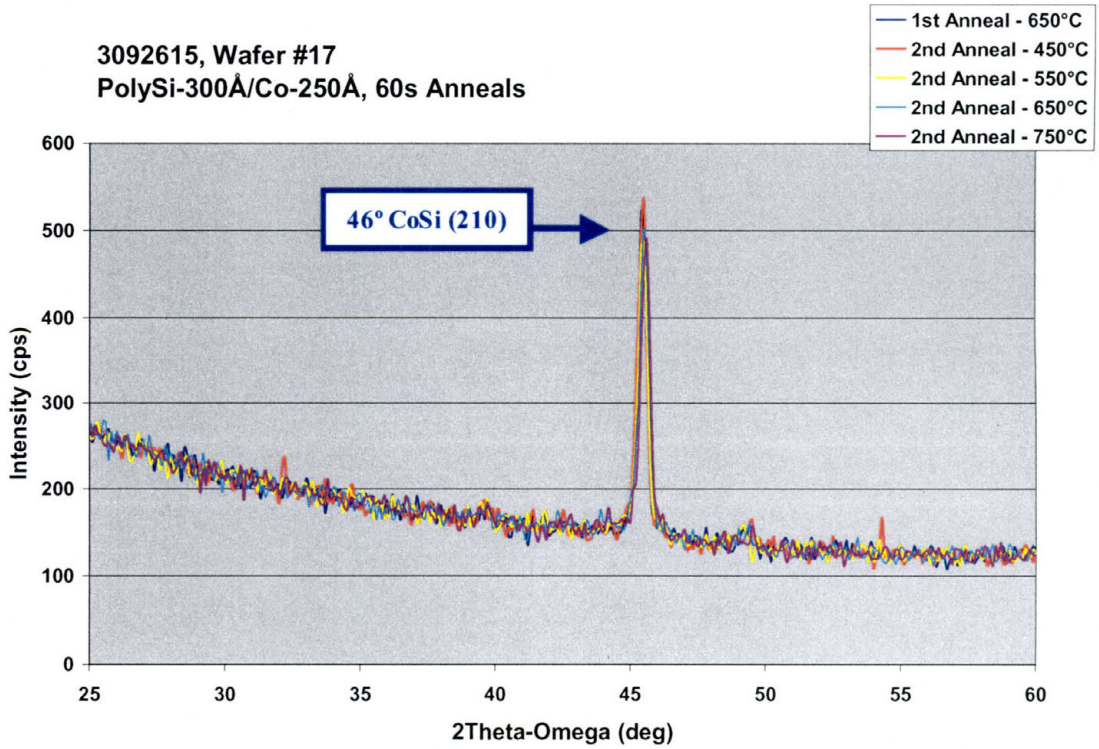

Figure B.60 - HAXRD 3092615 - Wafer# 17

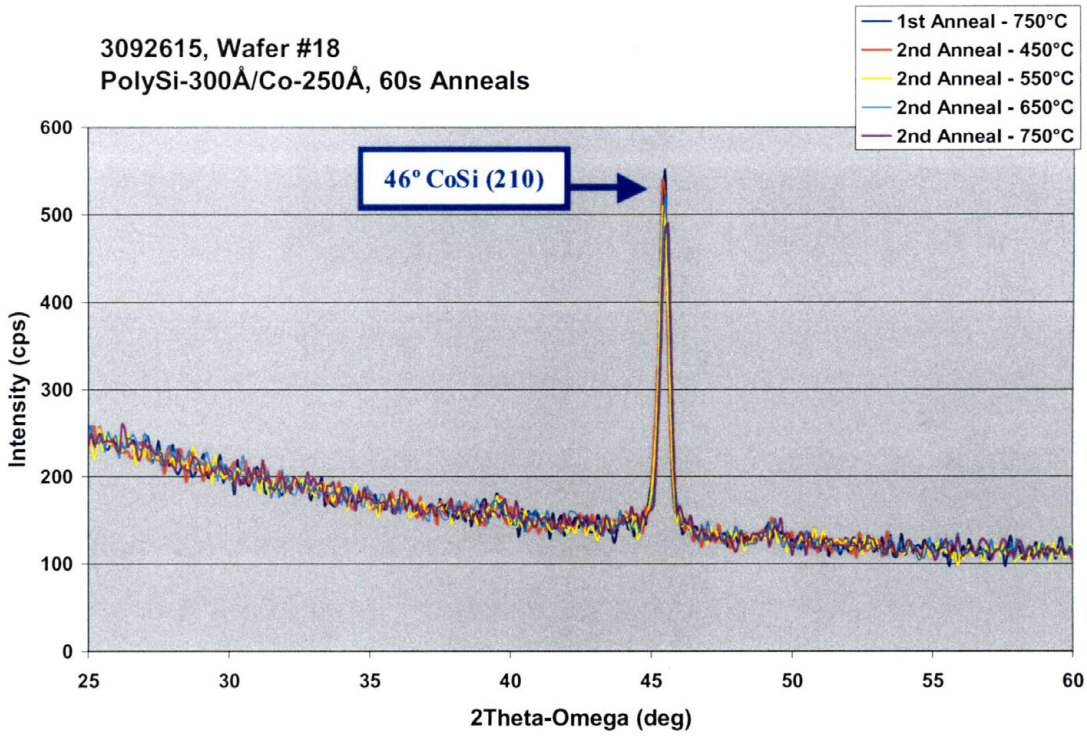

Figure B.61 - HAXRD 3092615 - Wafer# 18

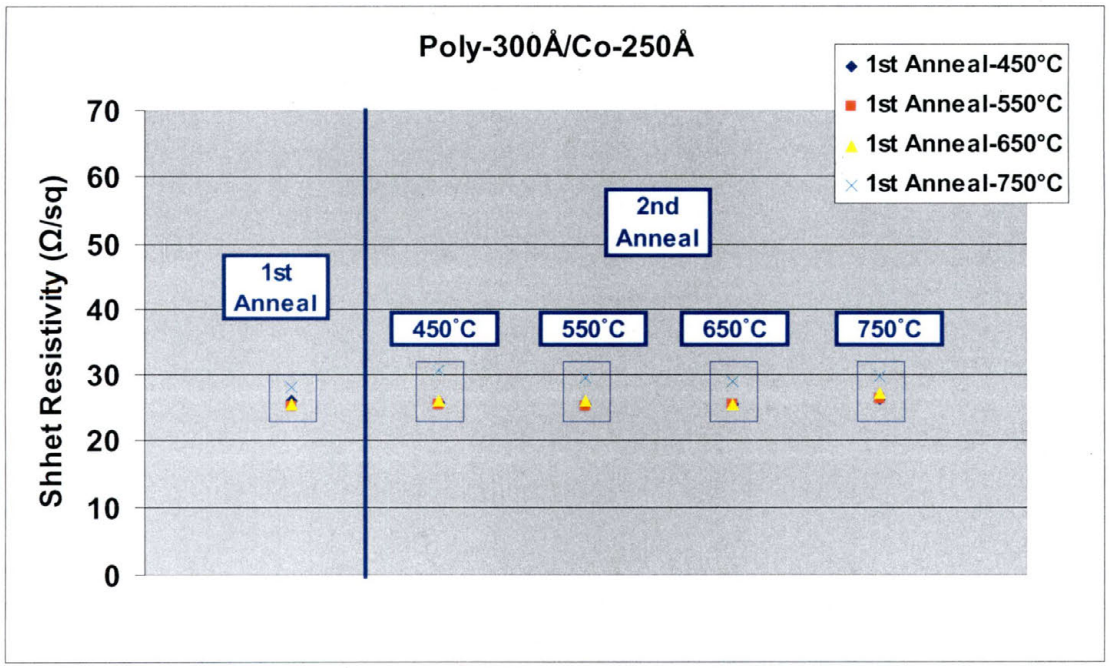

Figure B.62– Rs 3092615 - Wafer# 9, 10, 17, & 18

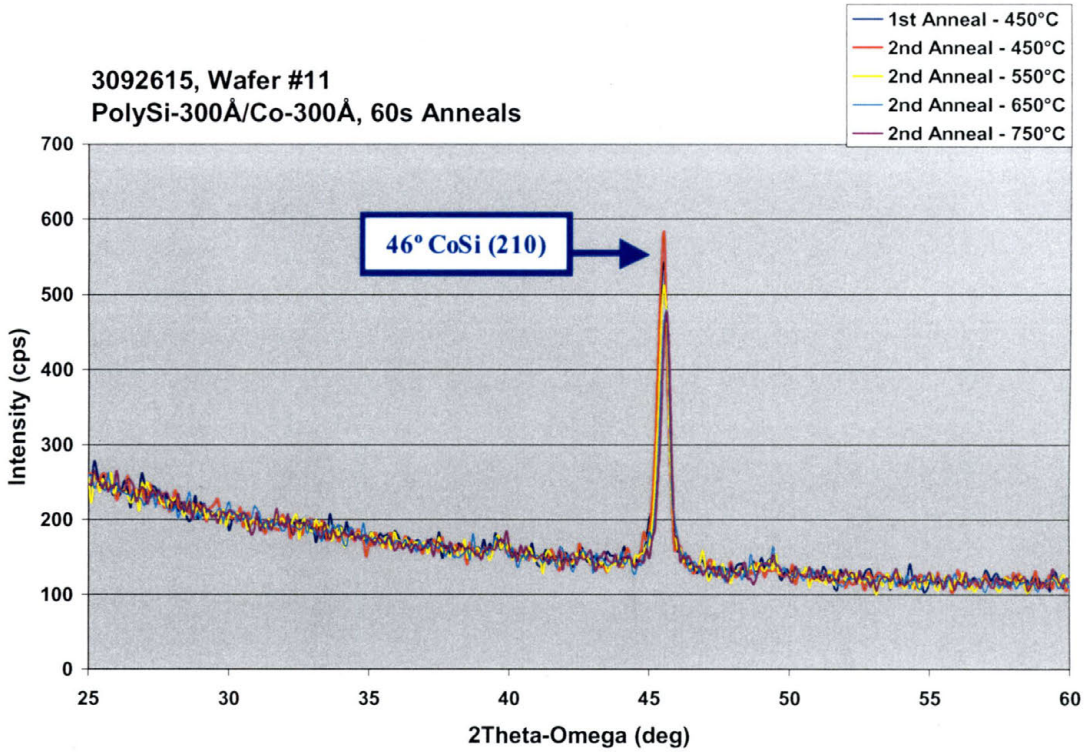

Figure B.63 - HAXRD 3092615 - Wafer# 11

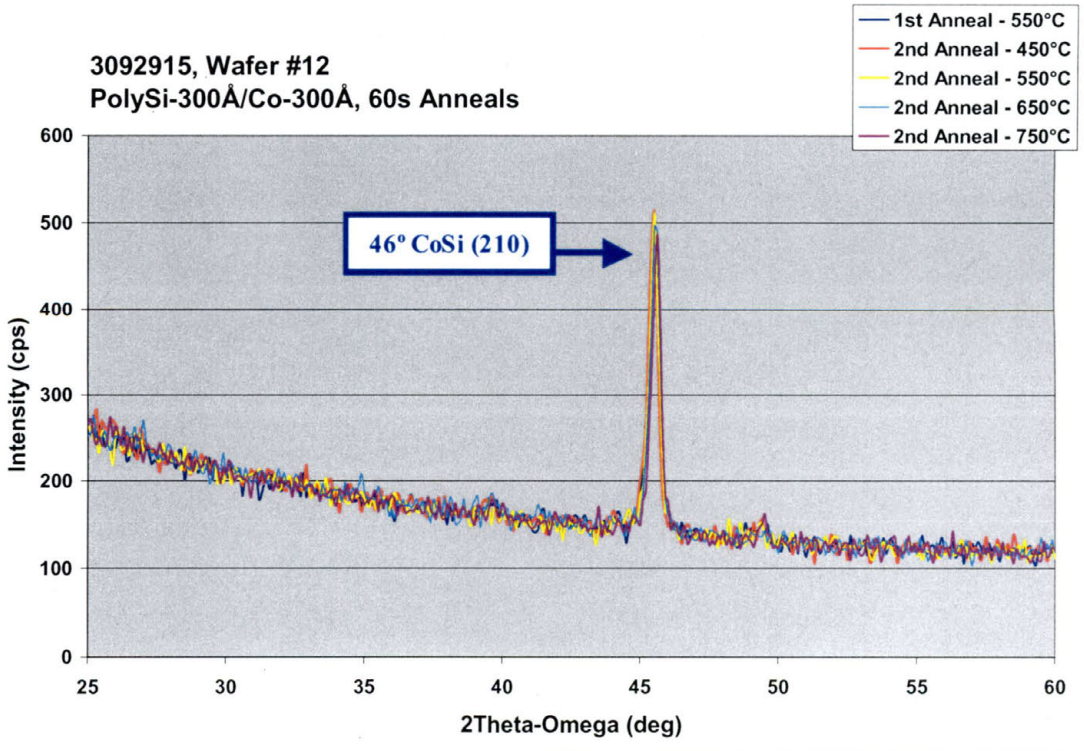

Figure B.64 - HAXRD 3092615 - Wafer# 12

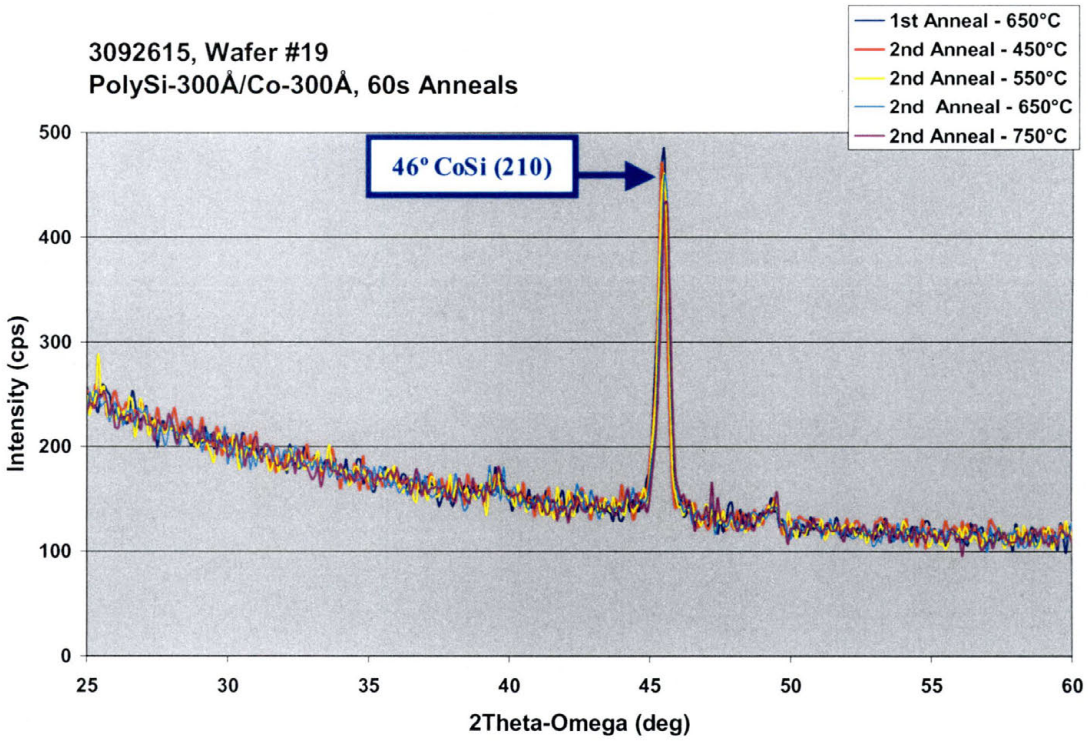

Figure B.65 - HAXRD 3092615 - Wafer# 19

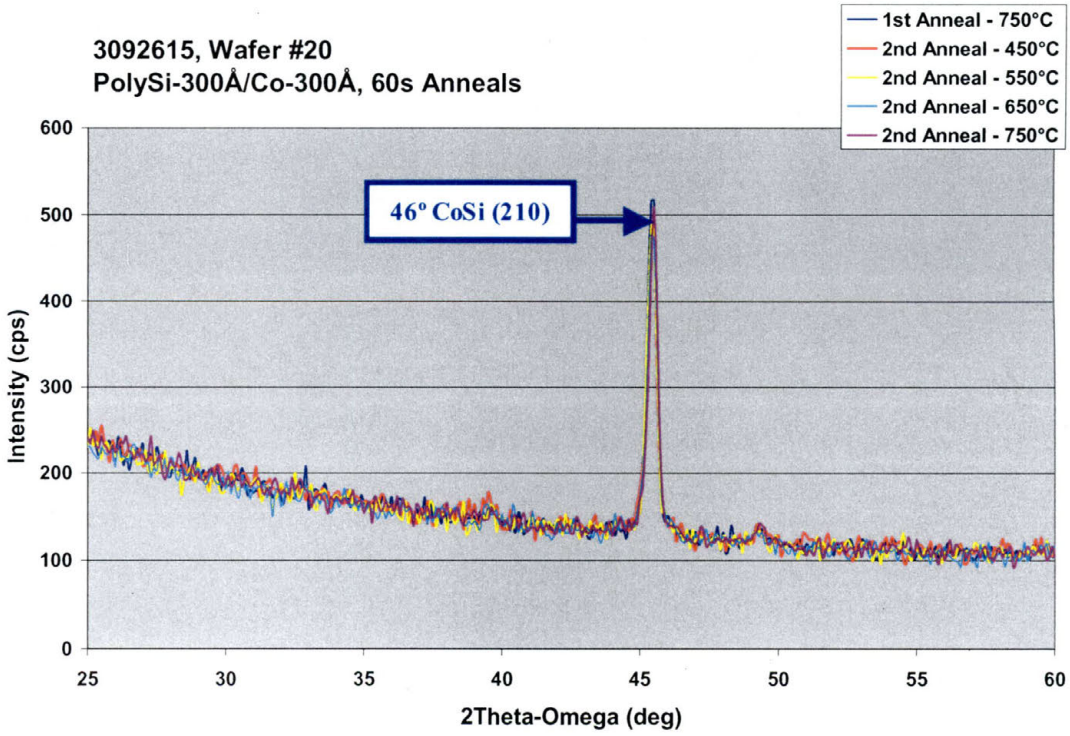

Figure B.66 - HAXRD 3092615 - Wafer# 20

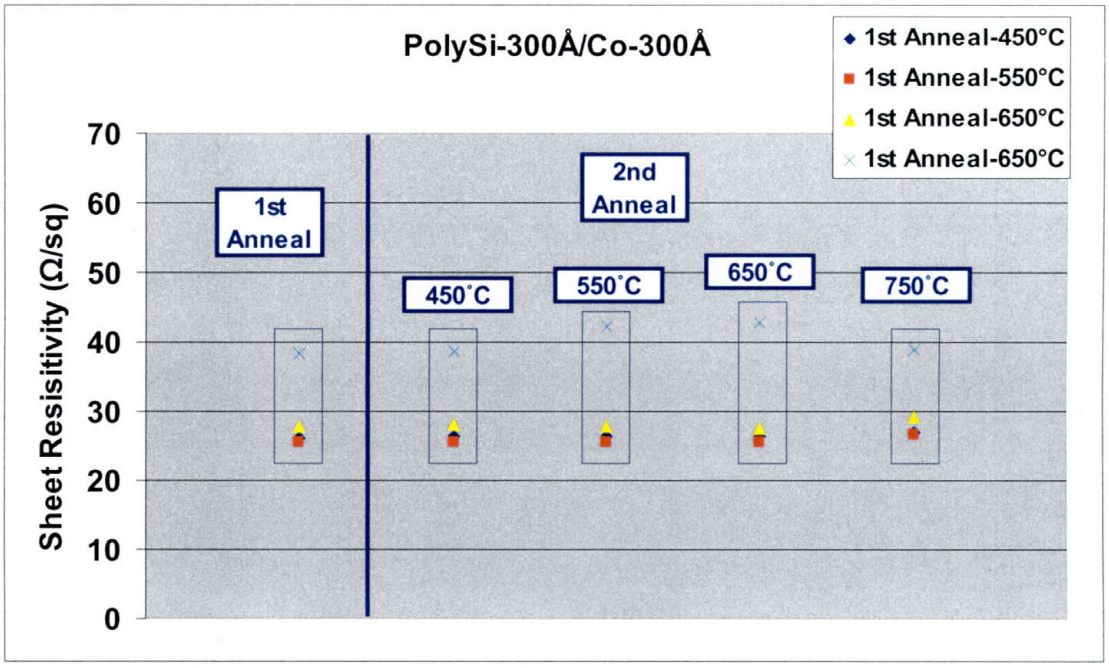

Figure B.67– Rs 3092615 - Wafer# 11, 12, 19, & 20

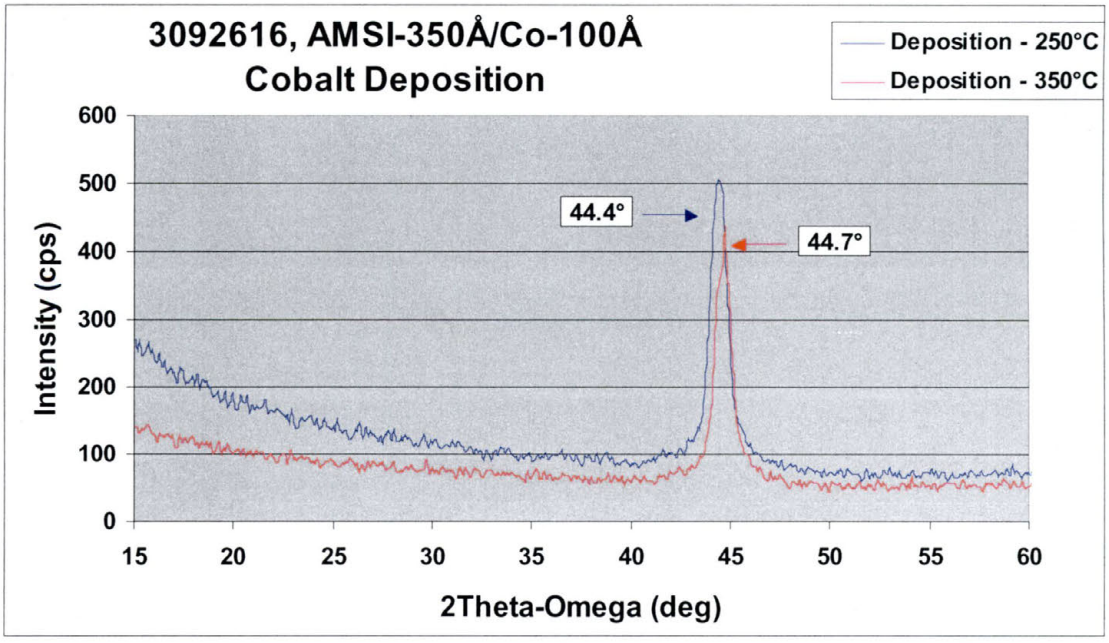

Figure B.68 - HAXRD 3092616 – Pre anneal AMSI

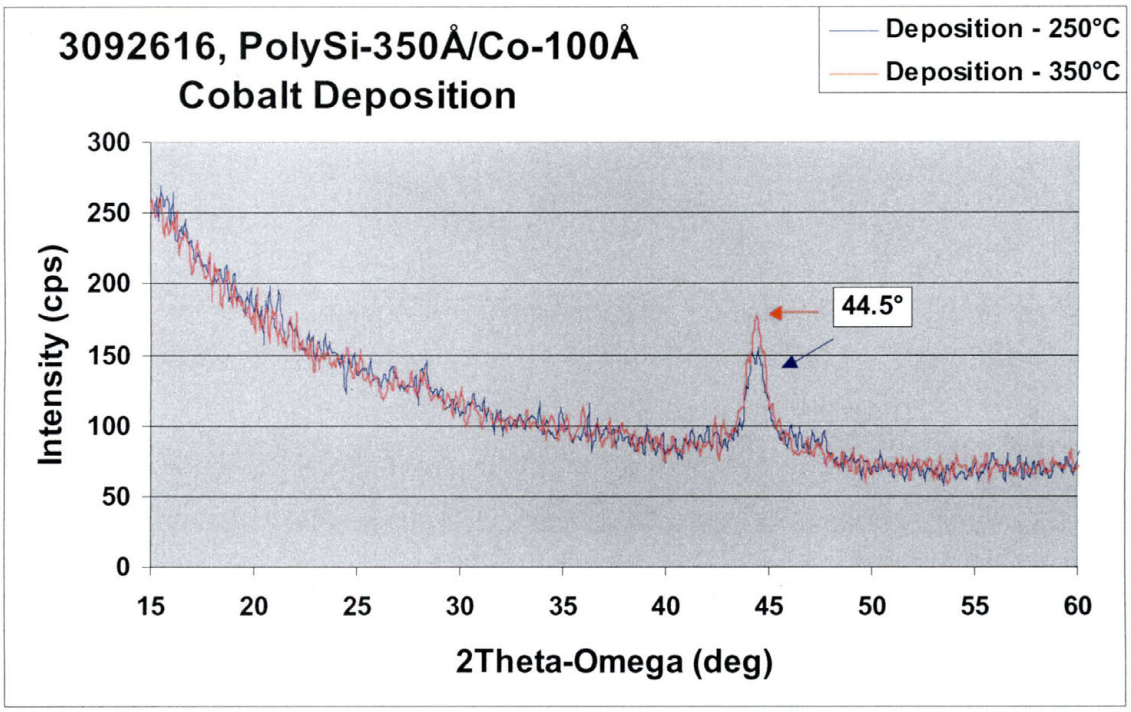

Figure B.69 - HAXRD 3092616 – Pre anneal PolySi

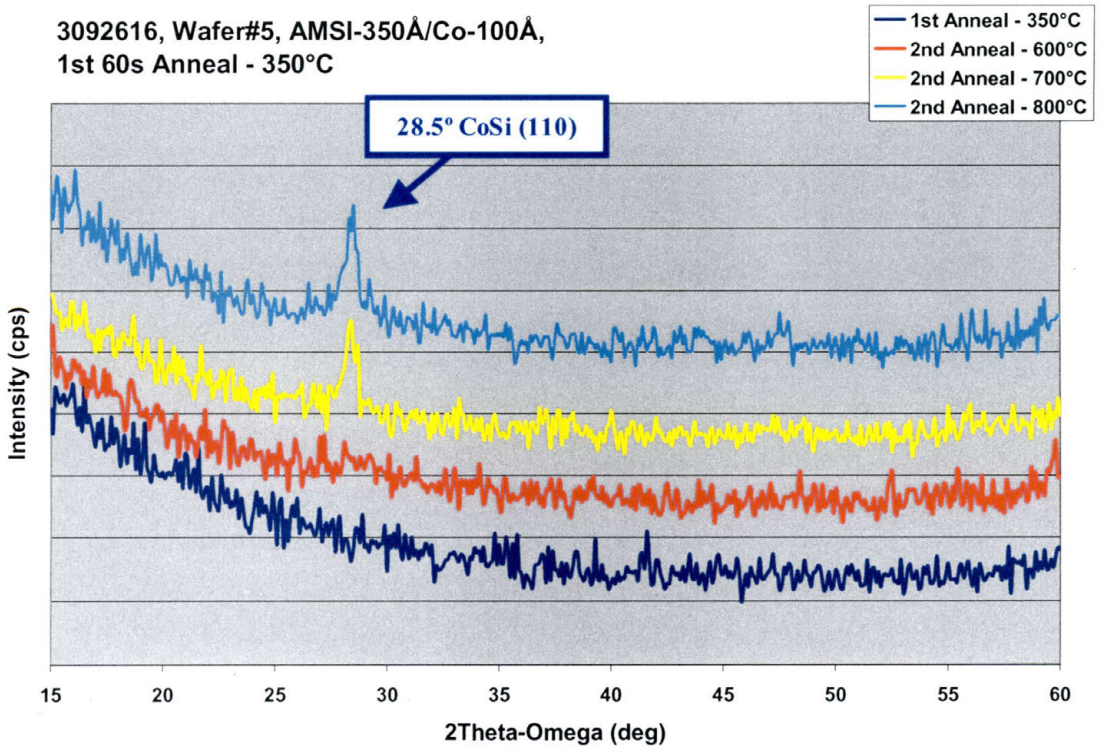

Figure B.70 - HAXRD 3092616 - Wafer# 5

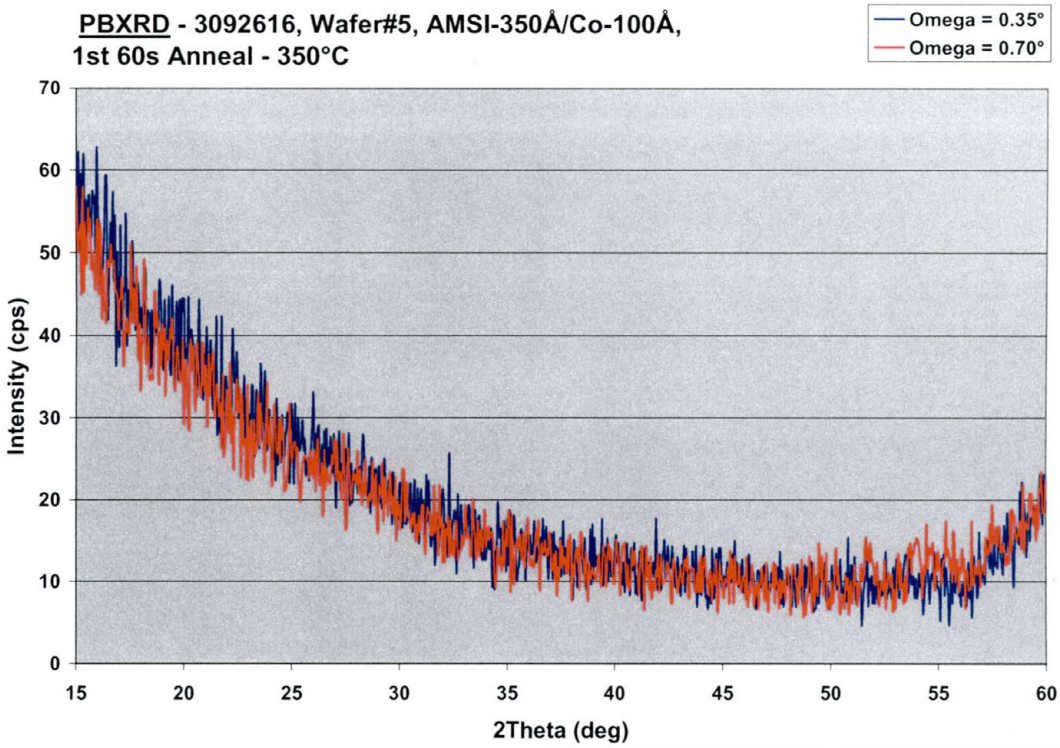

Figure B.71 - PBXRD 3092616 - Wafer# 5

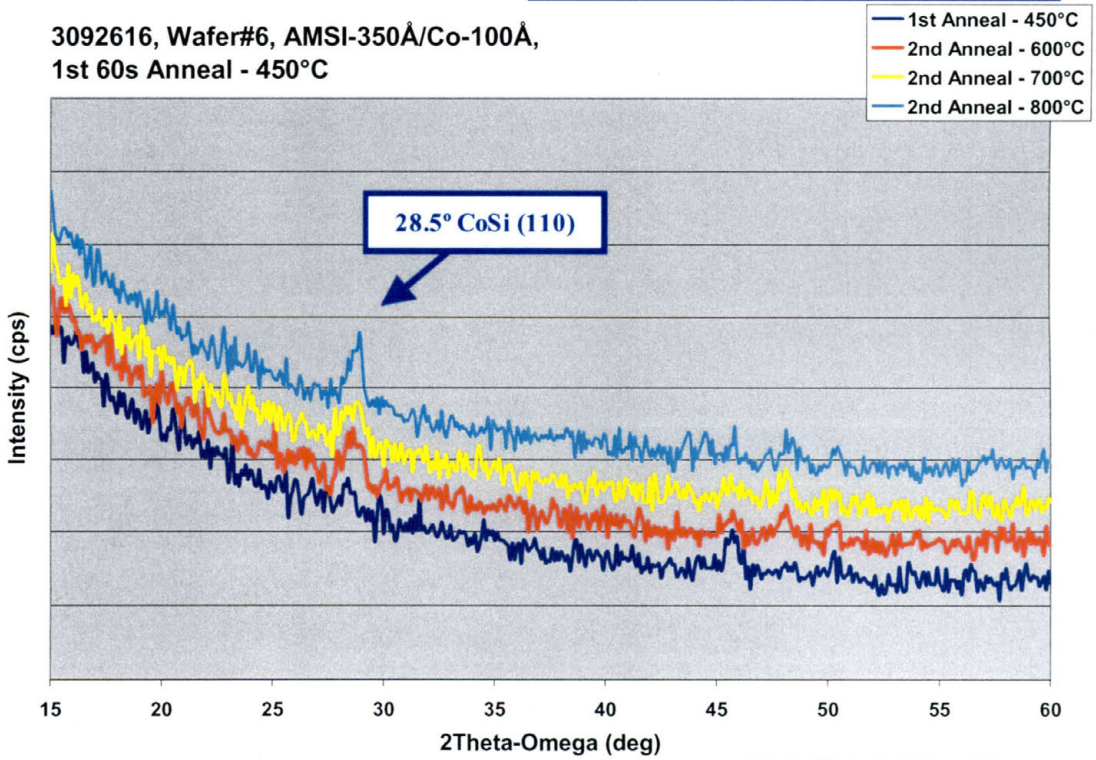

Figure B.72 - HAXRD 3092616 - Wafer# 6

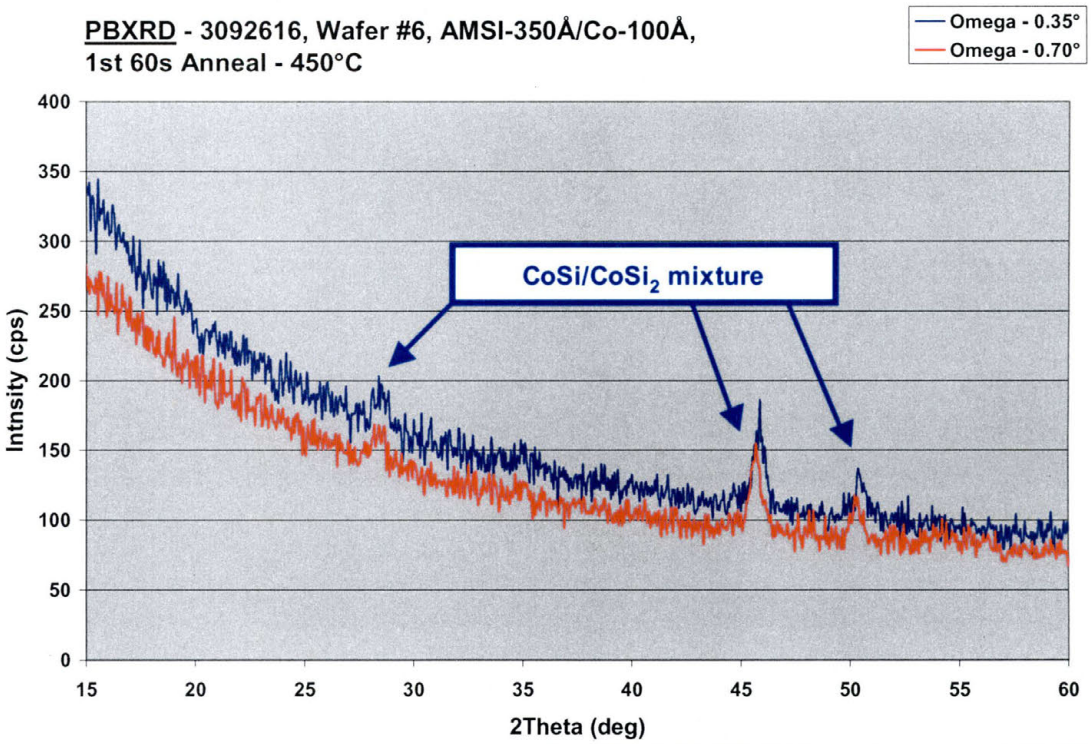

Figure B.73 - PBXRD 3092616 - Wafer# 6

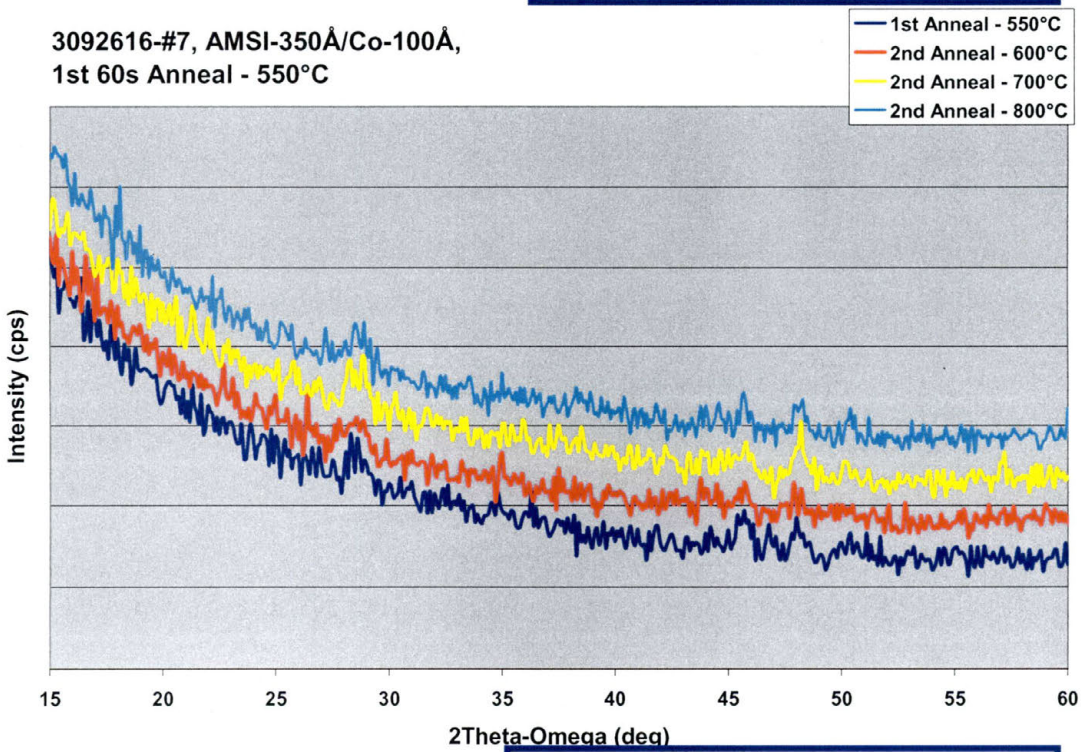

Figure B.74 - HAXRD 3092616 - Wafer# 7

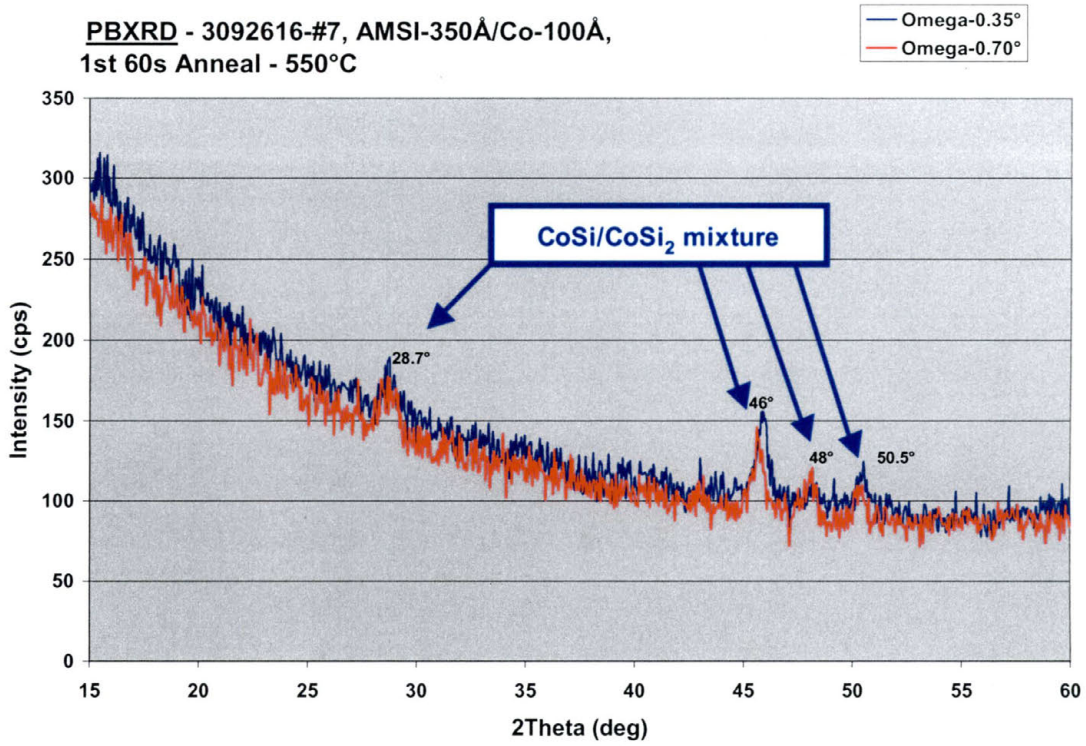

Figure B.75 - PBXRD 3092616 - Wafer# 7

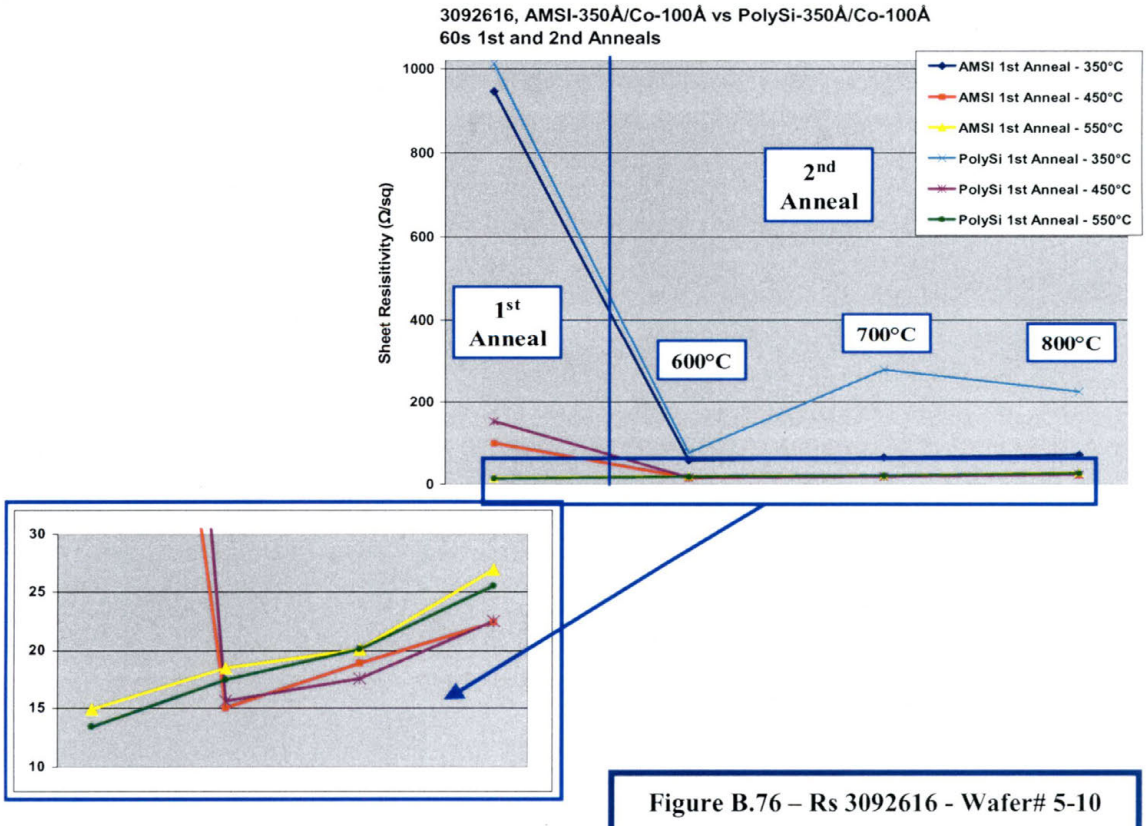

Figure B.76 – Rs 3092616 - Wafer# 5-10

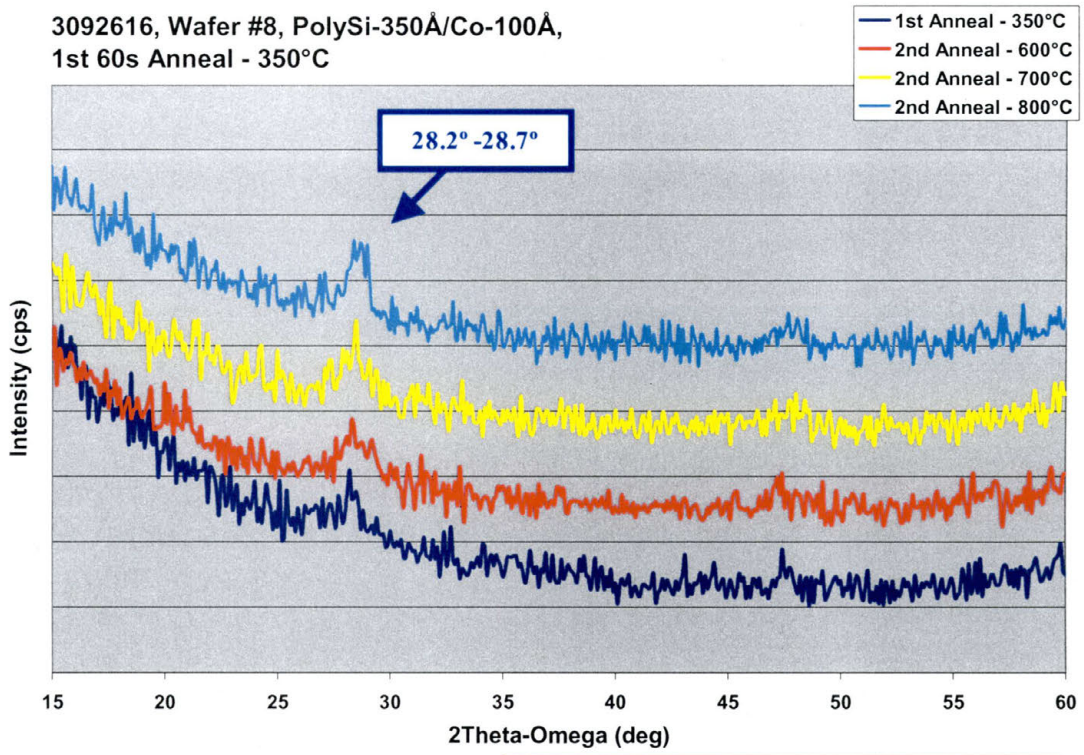

Figure B.77 - HAXRD 3092616 - Wafer# 8

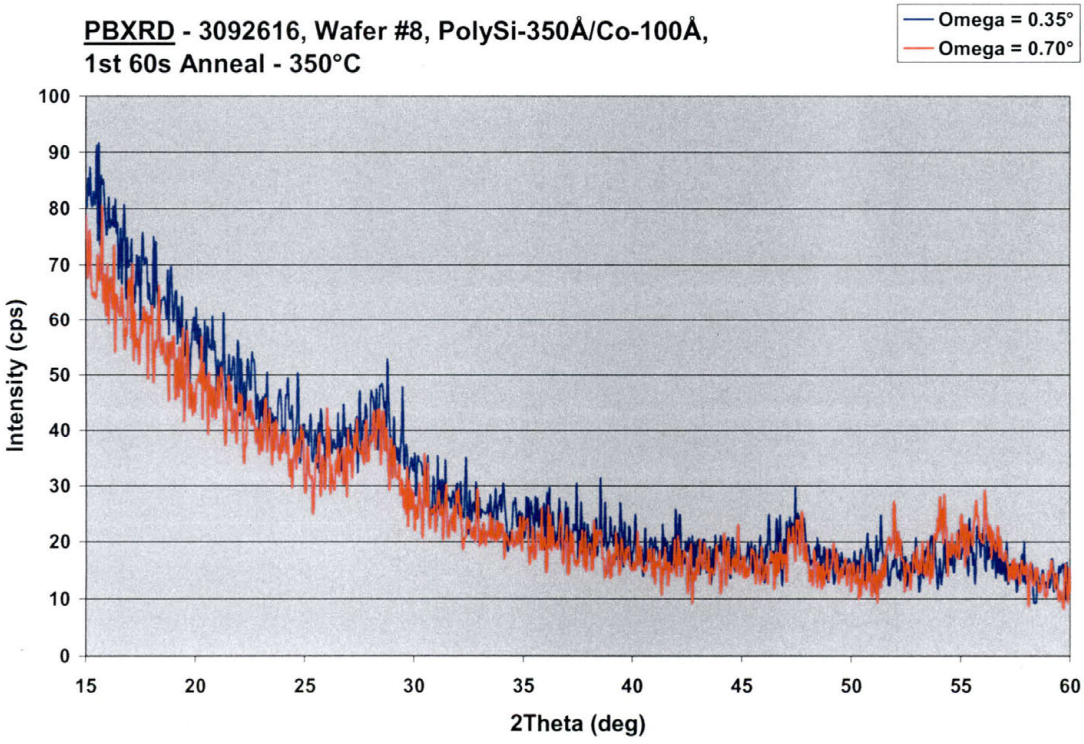

Figure B.78 - PBXRD 3092616 - Wafer# 8

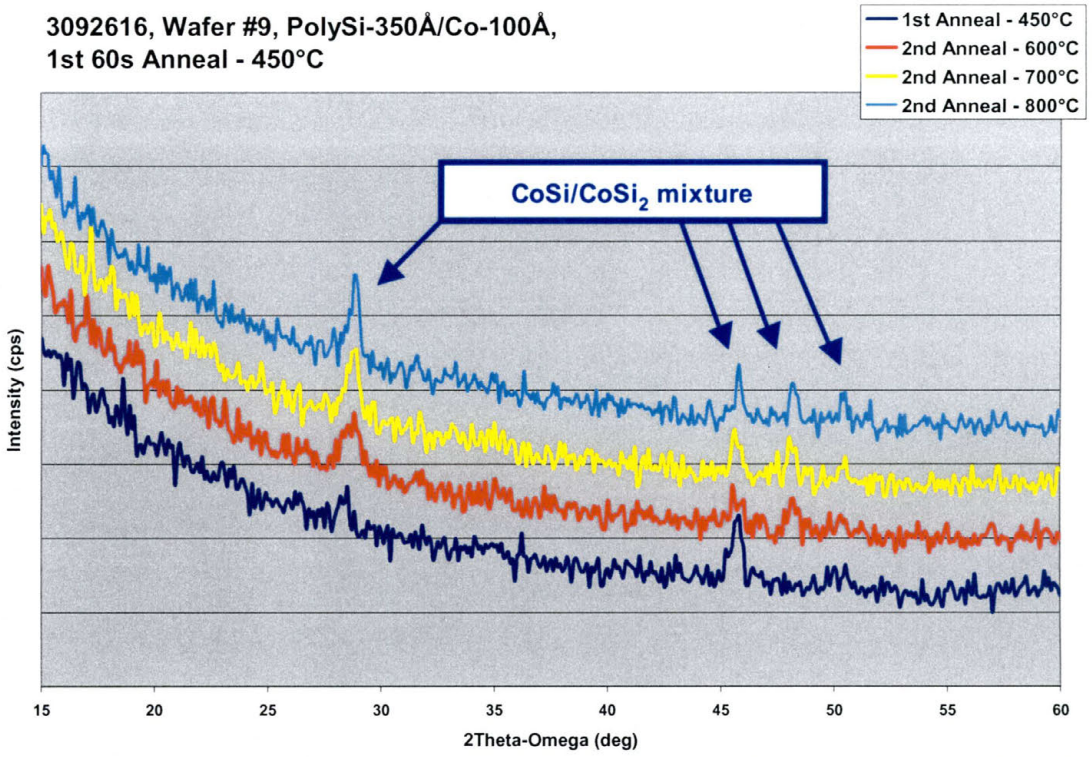

Figure B.79 - HAXRD 3092616 - Wafer# 9

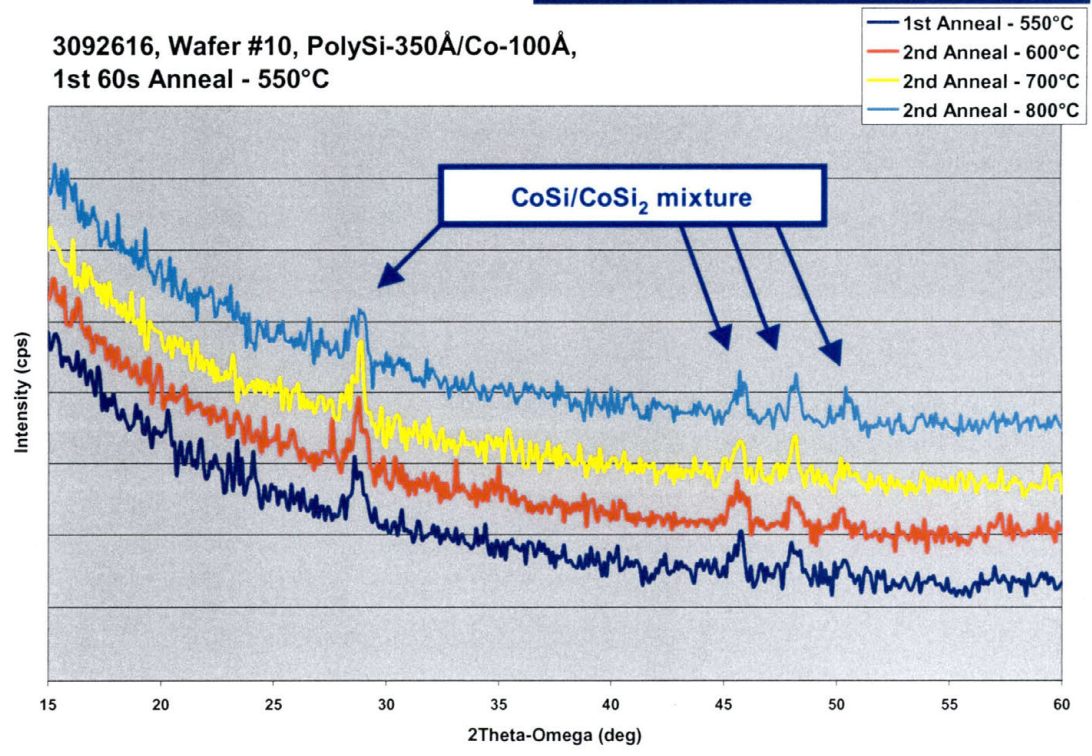

Figure B.80- HAXRD 3092616 - Wafer# 10

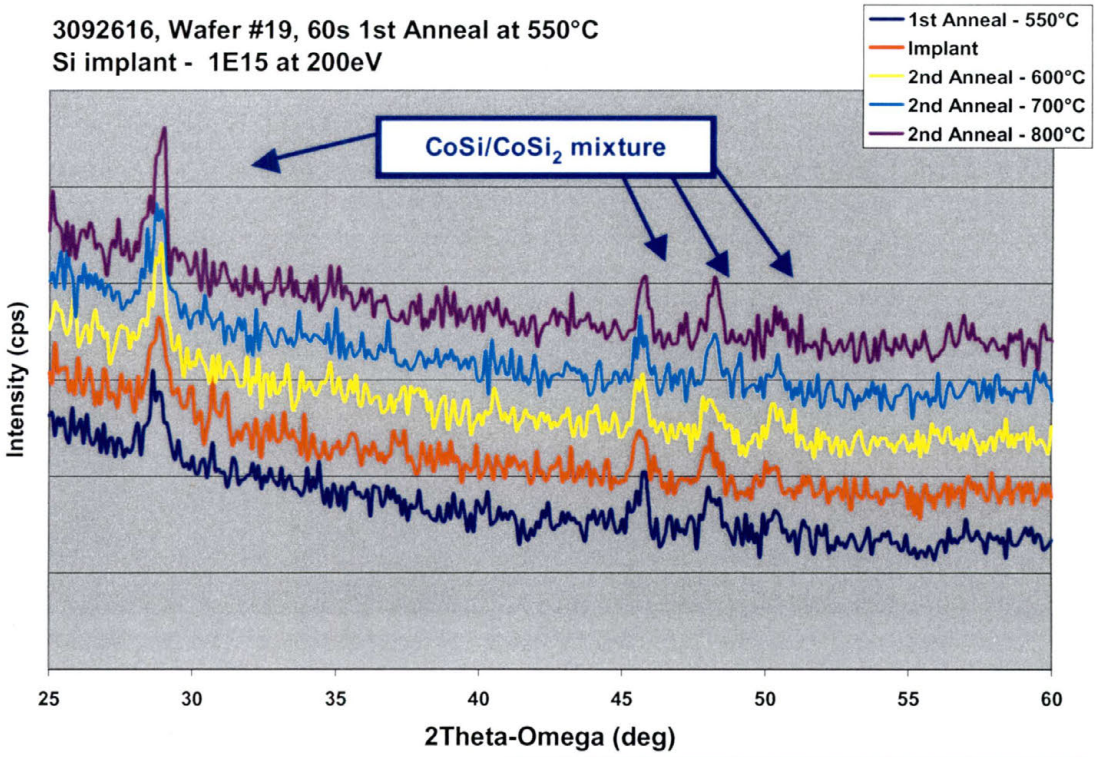

Figure B.81 - HAXRD 3092616C - Wafer# 19

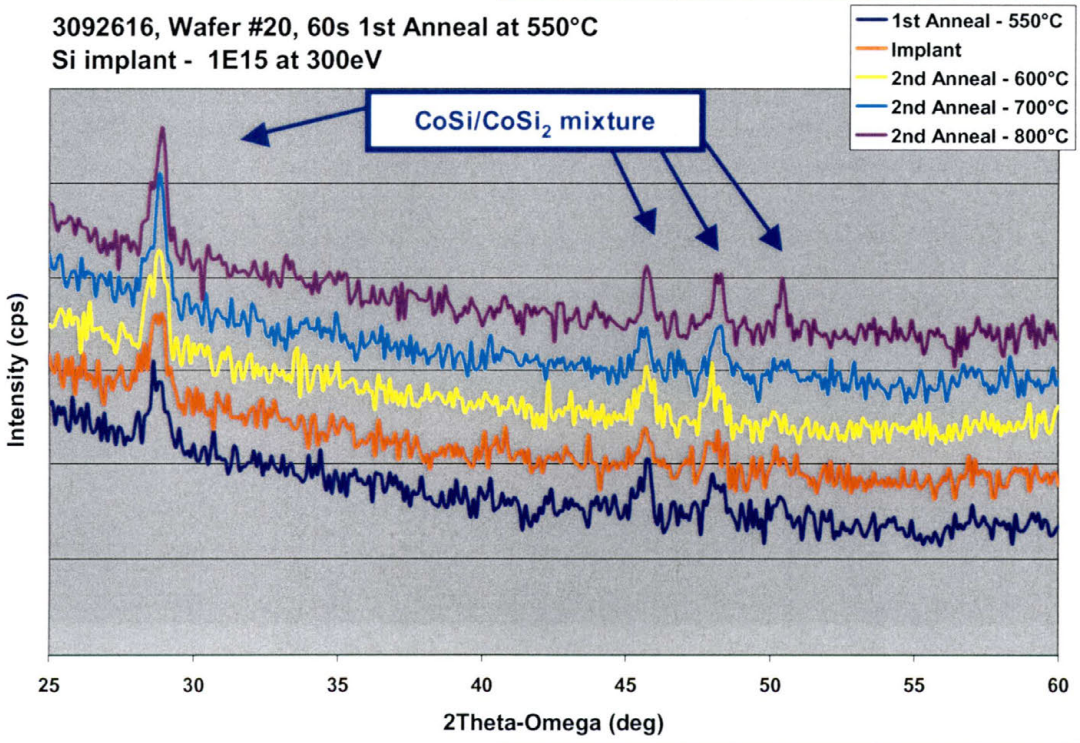

Figure B.82 - HAXRD 3092616C - Wafer# 20

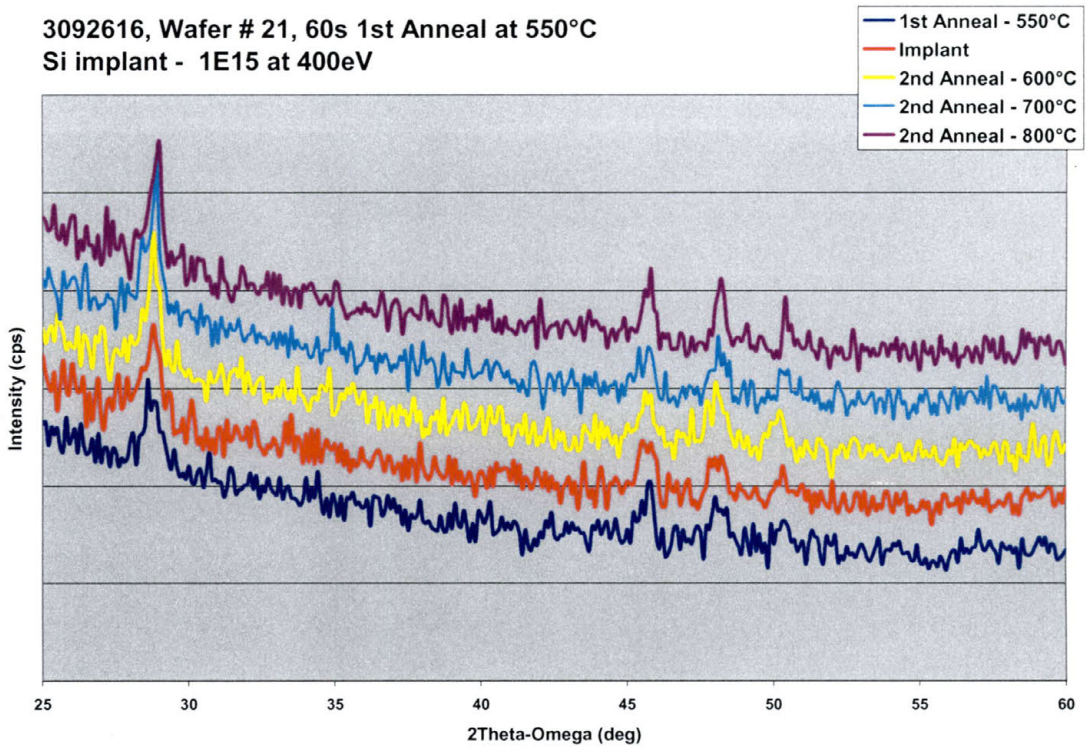

Figure B.83 - HAXRD 3092616C - Wafer# 21

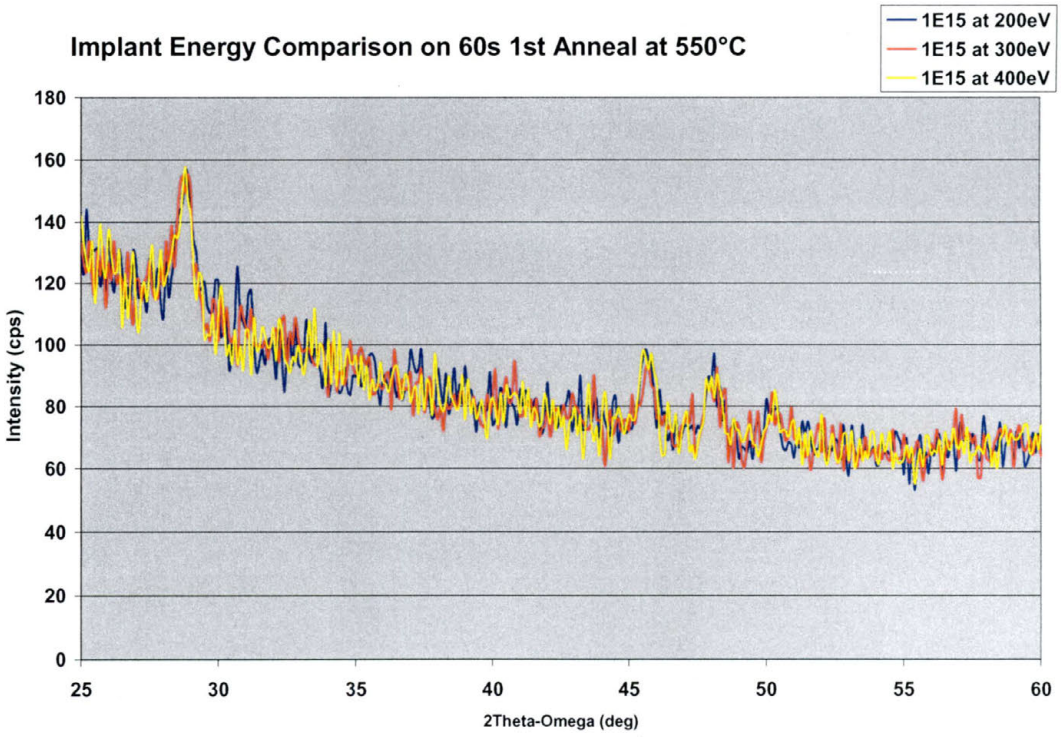

Figure B.84 - 550°C Implant Comparison

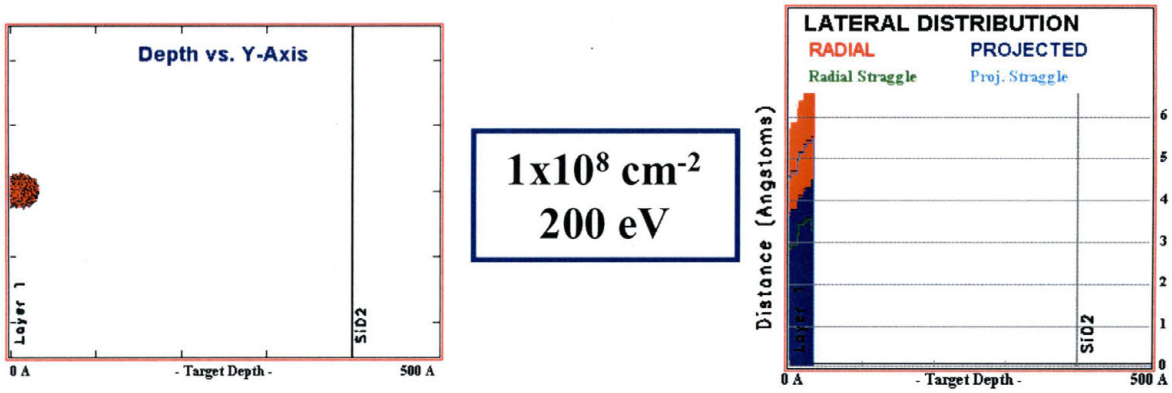

Figure B.85 – SRIM Simulation (200eV)

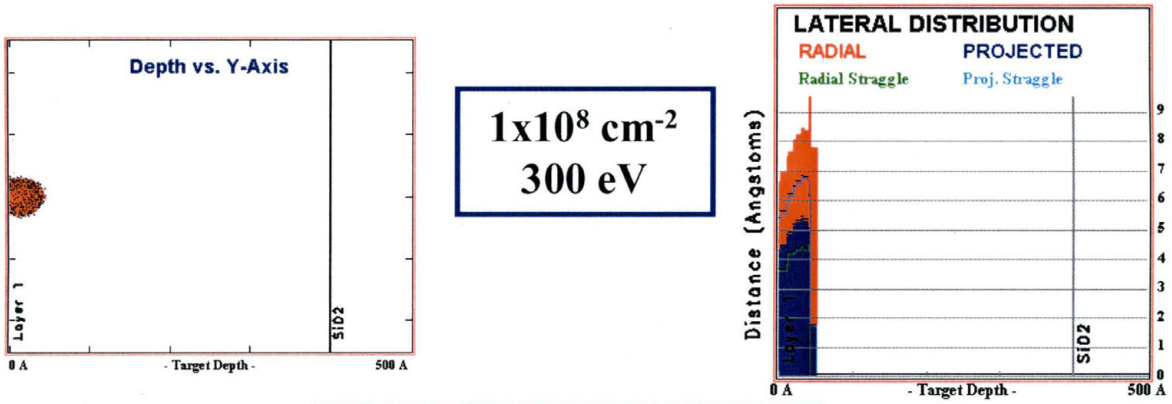

Figure B.86 – SRIM Simulation (300eV)

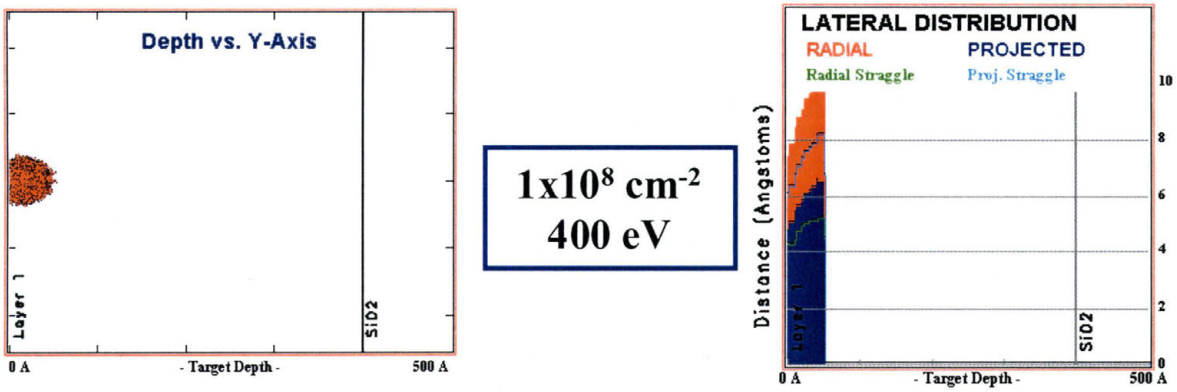

Figure B.87 – SRIM Simulation (400eV)

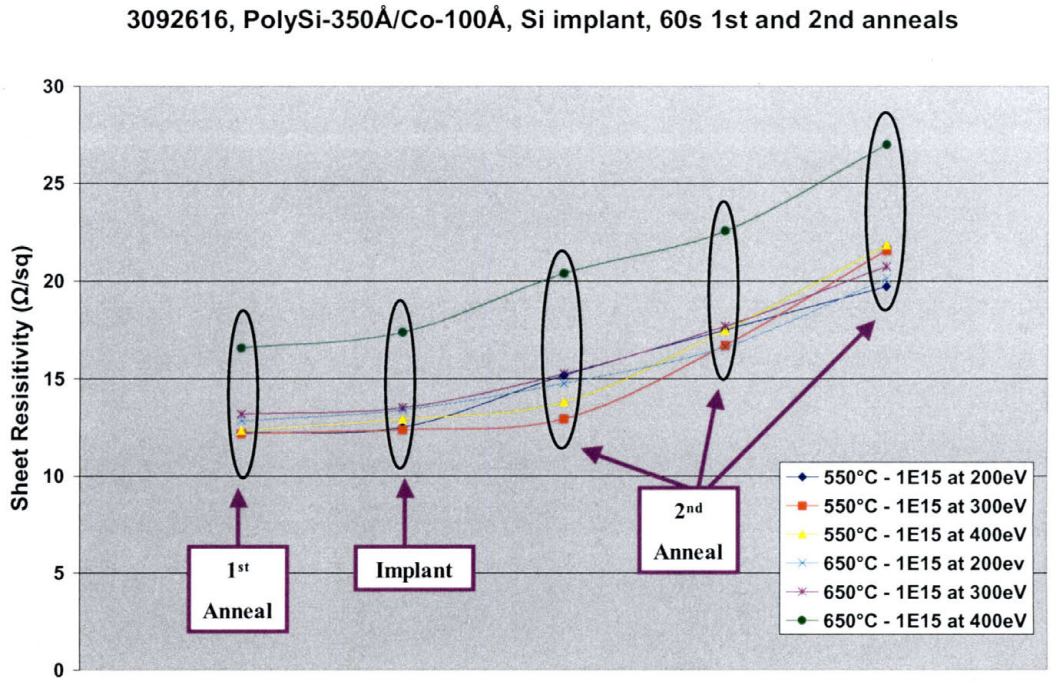

Figure B.88 – Rs 3092616C - Wafer# 19-24

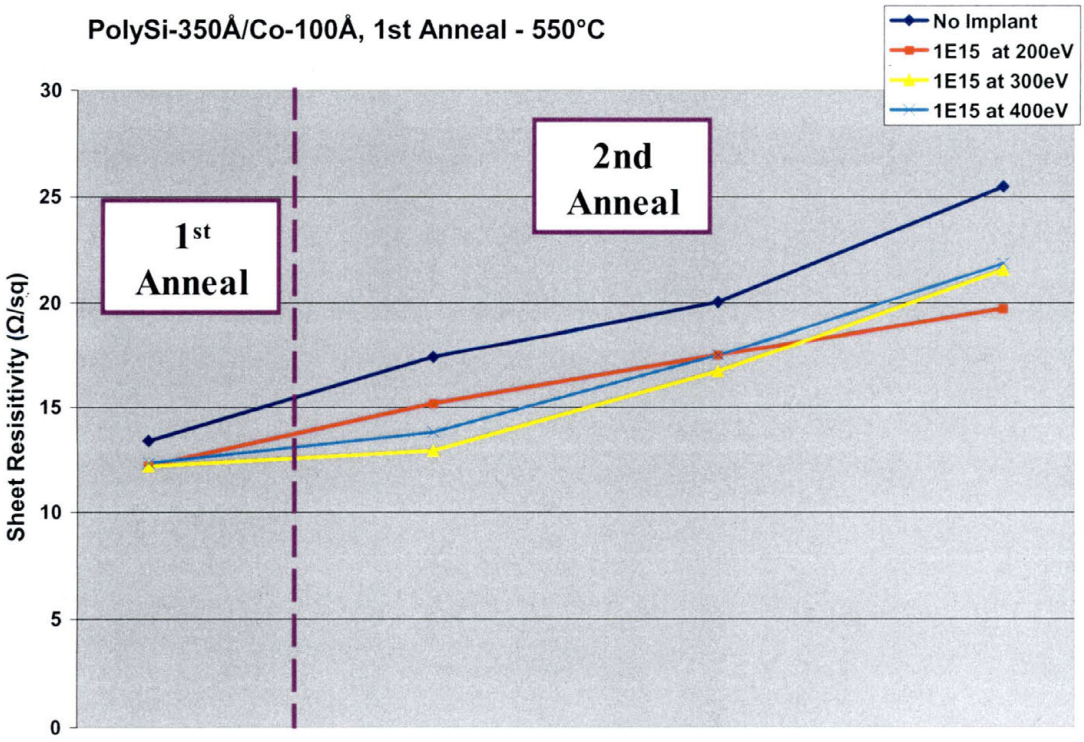

Figure B.89 – Non-implant vs. implant for 550°C 1st anneal

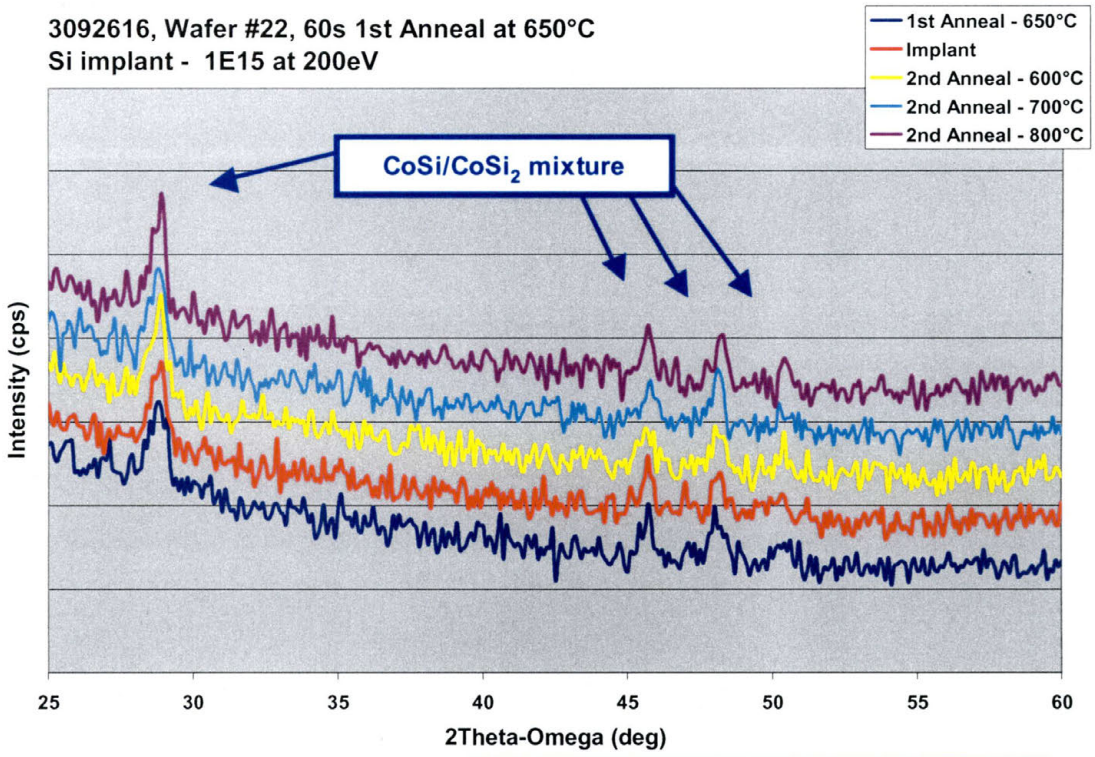

Figure B.90 - HAXRD 3092616C - Wafer# 22

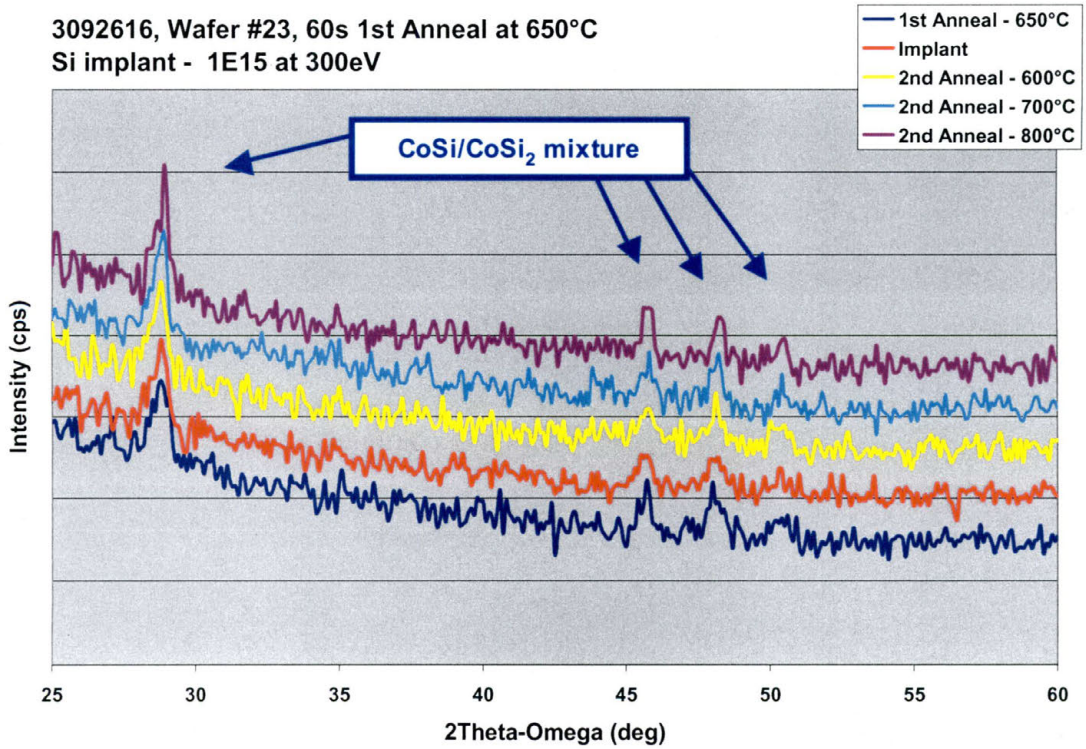

Figure B.91 - HAXRD 3092616C - Wafer# 23

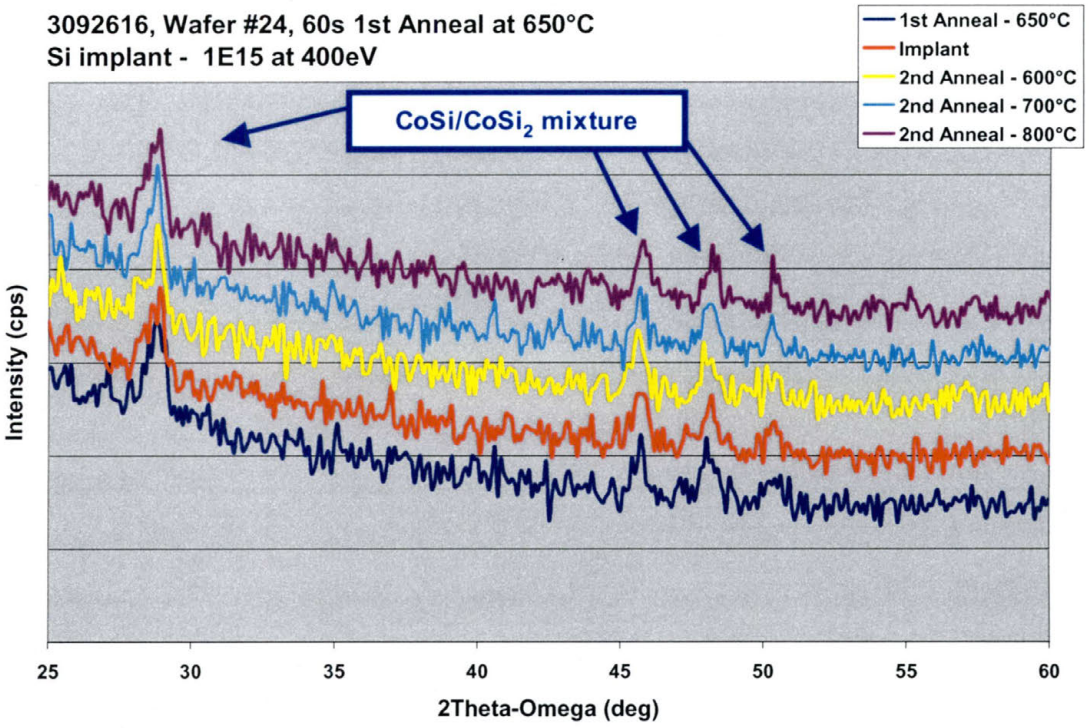

Figure B.92 - HAXRD 3092616C - Wafer# 24

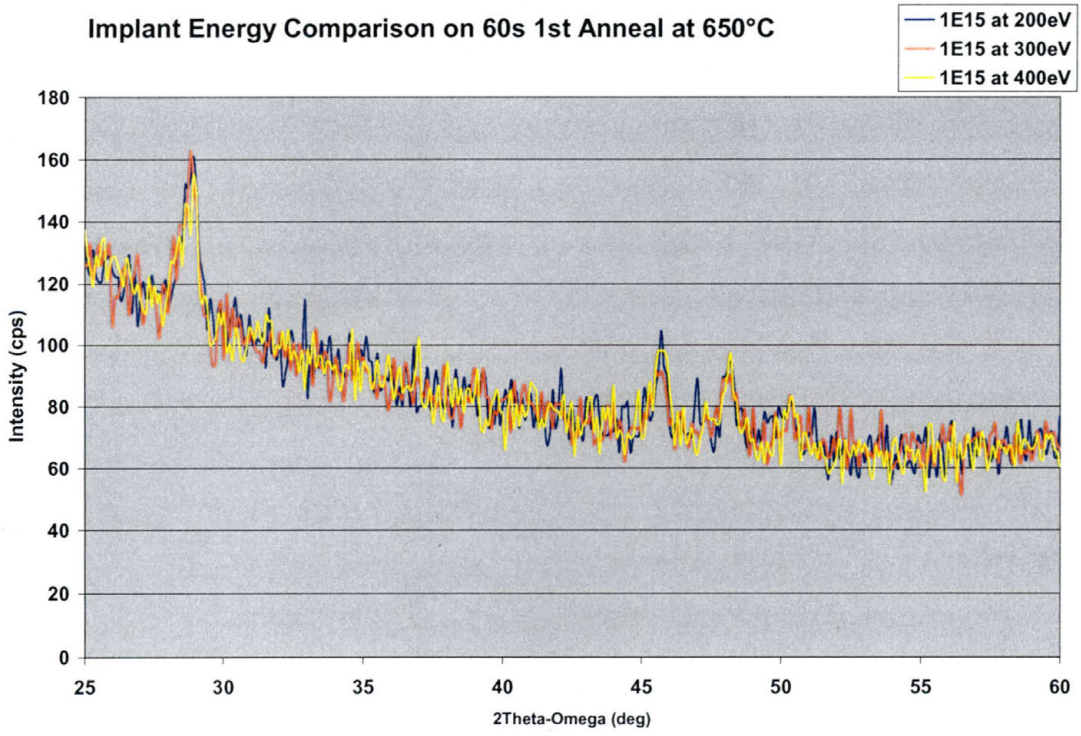

Figure B.93– 650°C Implant Comparison

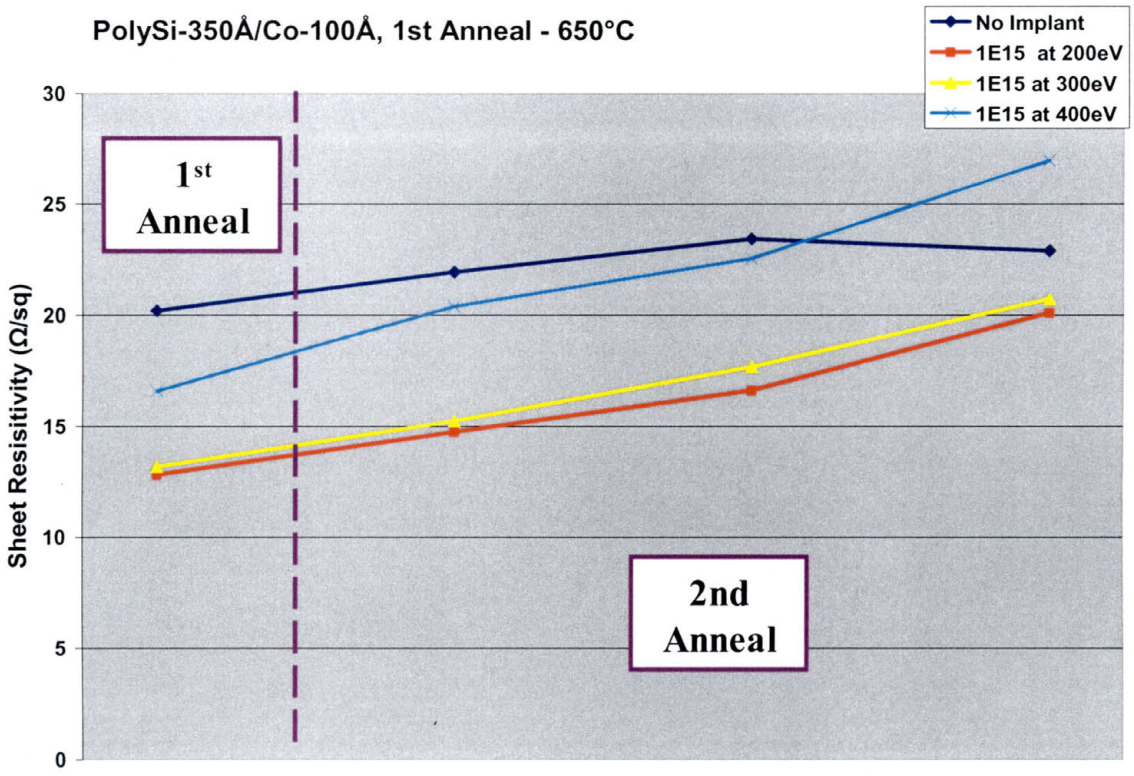

Figure B.94 – Non-implant vs. implant for 650°C 1st anneal

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