ANALYTICAL MODELING AND SIMULATION OF CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER

by

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DEDICATION

For my past, my present, and my future. To my family.

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ABSTRACT

Ultrasound technology has been studied, developed and widely used in medical imaging. Ultrasonic imaging was invented to substitute the high cost ionizing radiation in magnetic resonance imaging (MRI) system, because it is portable, has low production cost and can be embedded with external circuitry in making sensing or actuating devices. However, many conventional ultrasonic imaging systems nowadays use bulky and expensive piezoelectric Micromachined Ultrasonic Transducers (pMUTs). These utilize the piezoelectric effect of membrane material for sensing modalities, which can limit their applications and meet restrictions such as low image resolution, weak sensitivity and impedance mismatching.

Recently, capacitive Micromachined Ultrasonic Transducers (cMUTs) emerge as an alternative choice to traditional PZT ceramic based transducers in ultrasonic imaging. They not only have better bandwidth and sensitivity in producing better imaging resolution, low signal-to-noise ratio, but they allow the fabrication and integration with other electrical circuits much easier. Possessing many advantages over pMUTs, cMUTs attract interests from MEMS researchers and become more popular in medical imaging, non-destructive testing, ultrasound ranging, and flow metering applications.

This thesis presents the design characterization, modeling and microfabrication of cMUTs. Four cMUTs arrays are designed with different array geometries, membranes' dimensions as well as number of cMUT cells in an array. cMUTs are first analytically modeled and then simulated using finite element method (FEM) analysis to compare the

numerical analysis results. The analytical cMUTs modeling is characterized for spring constant, resonant frequency and pull-in voltage. COMSOL Multiphysics 4.3b is use for simulation the profound insight of cMUTs' behavior such as: resonant frequencies, pull-in voltage, membrane's deflection and implied spring constant.

This thesis also lays out the detail fabrication process flow of cMUTs. They are promised to be fabricated using mature of semiconductor processes which include photolithography, metal deposition and selective etching. In this thesis, in order to define the cMUT's membrane, we will use direct wafer bonding technique with both chemical and O_2 plasma surface activation processes to decrease the process temperature to as low as 400ºC. In this thesis, the fabrication of cMUTs is proposed at low process temperature, providing compatibility with CMOS integration.

1. INTRODUCTION

Background of Micromachined Ultrasonic Transducers

Ultrasonic transducers are basically a type of acoustic sensor that convert AC voltages to ultrasound or convert ultrasound into electrical signal in reverse. As shown in Fig. 1, ultrasounds occur at frequencies above hundreds of kilohertz which are higher than the limit of human hearing and are widely used in applications such as medical imaging [1], [2], non-destructive testing (NDT) [3], [4], sonar, flow metering [5], [6], and ultrasonic range measuring [7], [8]. For example, in medical diagnostic imaging, the ultrasonic imaging system consists of an array of ultrasonic transducers and an imaging system. Ultrasound waves propagate into the objects, then the reflecting sound waves from the objects are received. The imaging system controls the ultrasonic transducers for transmitting and receiving the ultrasound, and electronically generates an ultrasound image using a set of data collected from transducers [1], [9]. In immersion flow metering, a single ultrasonic transducer or a pair of transmitter and receiver uses the pulse-echo measurement and the speed of sound in air to calculate the distance between the target and the ultrasound source. Vice versa, it calculates the transmitting time and speed of sound from the provided distance between the targets [6].

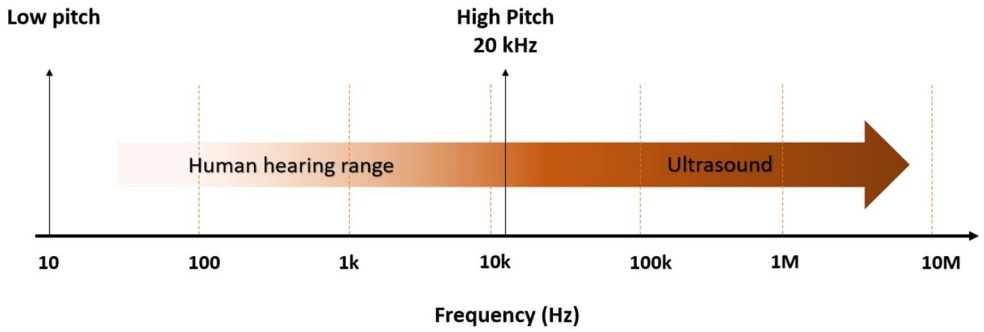


Figure 1. Sound ranging by frequencies. Ultrasound is above the human hearing range, which is at 10 kHz.

In recent decades, micromachined ultrasonic transducers have been invented as an alternative replacement to conventional piezocomposite ultrasonic transducers, but their principle is still based on piezo-ceramics [10], [11]. There are two types of micromachined ultrasonic transducer: piezoelectric type and capacitive type [7]. pMUTs have been invented and widely used for many years [7], [12]. The piezoelectric effect illustrates the ability of a certain material to generate electricity by applying a mechanical stress, and reversely generate stress by applying an electric field. pMUT commonly use lead-zirconate-titanate (PZT) film for sensing or actuating since this material has high energy density and large effective stress piezoelectric coefficient [13]. The membrane of a pMUT device is a micromachined multilayer with piezoelectric layer stacked between two metal electrode layers, which is isolated from the substrate by an insulation layer (mostly SiO_2). The PZT thin film in the membrane is mainly used to vibrate the membrane while the pMUT's frequency is decided by the membrane's dimensions and physical properties [14]. Figure 2 shows cross-section view of a basic pMUT device.

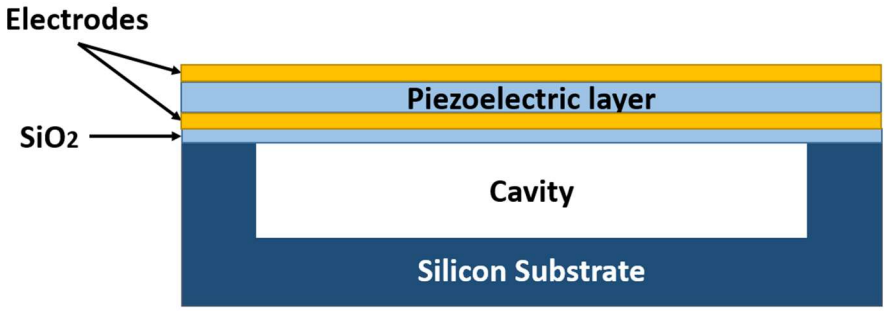


Figure 2. Cross-section view of a basic pMUT's structure. Piezoelectric layer is located between upper and lower electrodes. SiO_2 acts as an insulation layer which isolate the membrane from the silicon substrate.

pMUT has no vacuum gap between the top and bottom electrodes. Hence, the deflection of the membrane is not affected and limited by the separation of the electrodes. Moreover, piezoelectricity consumes low power since the system does not require external circuit to supply charge for measuring the signals, so that pMUTs can operate in situation when the power supply is limited [7]. However, pMUTs suffer from some limitations. They have low acoustic output and receiving sensitivity, the coupling coefficient of pMUT is relatively low which is at around 1 ~ 6% [15]. For medical field and fluid-coupled application, piezoelectric transducers have an issue of impedance mismatching. For instant, the acoustic impedance Z_α of commonly used piezoelectric materials varies from 28 MRayls to 40 MRayls (PZT5H 28.9 MRayls, PZT4 30.8 MRayls, $PbTiO_3$ 39.8 MRayls, etc) [16], which are huge compared to that of human tissues such as blood or fat, which is at around 1.5 MRayls. Here, Rayl is the unit of a specific acoustic impedance measured by the pascal second per meter. Therefore, an impedance matching layer needs to be applied between piezoelectric devices and medium of interest to improve the image quality. It results in increasing production cost and complication. Furthermore, it is difficult to provide individual electrical connection to

each element in high density transducers and to other integrated circuit (IC) elements.

Capacitive micromachined ultrasonic transducers (cMUTs) typically have an array of multiple capacitor cells. Each cell includes one fixed electrode called the substrate and one thin movable electrode called the membrane suspended over the fixed electrode with a defined air gap (Fig. 3). These transducers consist of a huge number of membranes which can be fabricated onto silicon-based wafers by mean of a silicon microelectromechanical system (MEMS) fabrication technology using standard IC fabrication process. cMUTs produce ultrasonic waves through mechanical vibrations of the membranes. The membrane is activated electrostatically by the electrode embedded in its structure [17].

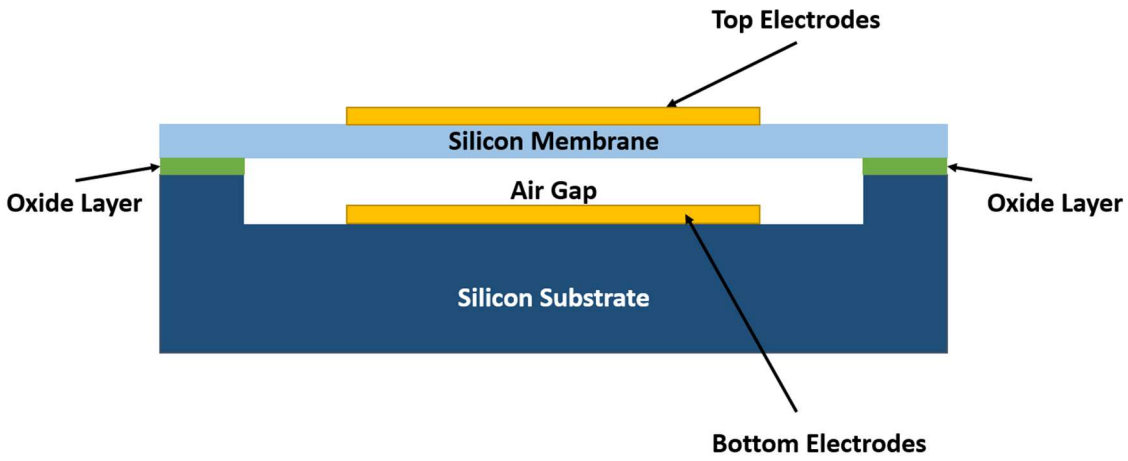


Figure 3. Cross-section view of a basic cMUT's structure.

The most noticeable advantages of cMUTs over pMUTs are wider immersion bandwidth and higher sensitivity for better imaging solution [18], high signal-to-noise ratio receivers, low mechanical impedance when used in air-coupled applications [19], eliminating the usage of a matching layer [20], and ease of integrating with other electronic circuits on the same wafer by using low temperature wafer bonding techniques

(<400°C) [21], [22]. Moreover, cMUTs can be fabricated using photolithography followed by other semiconductor techniques, which is hard to apply for piezoelectric transducers [23]. Therefore, they provide endless range of high frequency applications, such as intravascular ultrasound imaging (IVUS), air-coupled or liquid-coupled non-destructive evaluation (NDE) [24], flow metering in both air and liquid [25], and Lamb wave devices [26].

The fabrication of cMUTs can be done on silicon wafers which promises the simplified integration with CMOS electronics for mass production and narrow parameter specification, whereas it is difficult with conventional piezoelectric transducers. Furthermore, cMUTs can also be fabricated and operated in a wide range of temperatures while PZT based transducers are temperature sensitive and narrowly used in near room temperature [17]. Due to these advantages, cMUTs have alleviated the problem of conventional ultrasonic transducers and pMUTs to become an alternative choice [6].

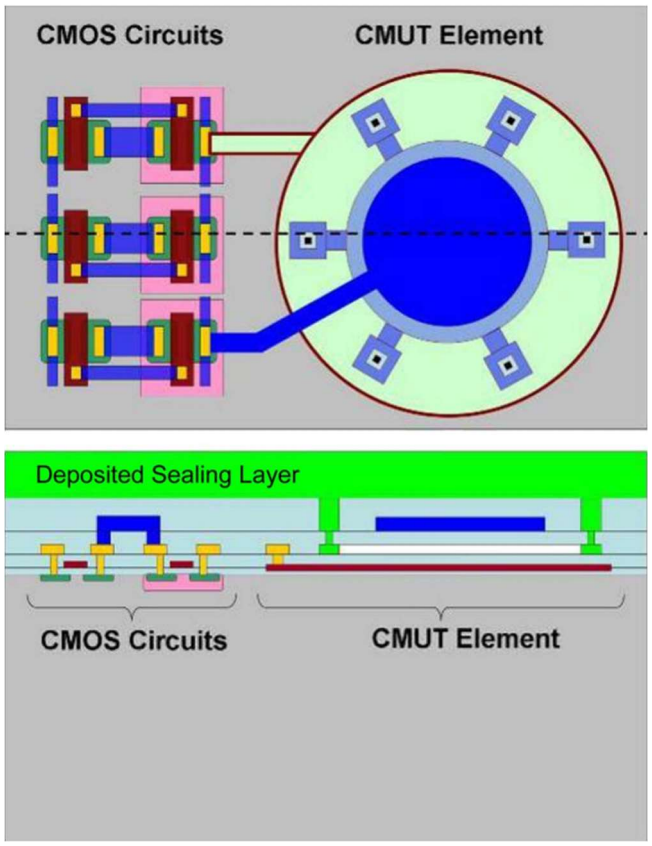
Literature Review

cMUTs can be fabricated using a standard semiconductor processes including multi-user MEMS processes (MUMPs) and complementary metal-oxide-semiconductor (CMOS) process [27,28]. MUMPs have the advantages in terms of low cost and accessibility to general users, and they allow users to fabricate cMUTs in the simpler process without using wafer-bonding and sacrificial release processes [29]. However, MUMPs have several limitations. One of them is that the material thickness and gap thickness have limited choices. The other is that the collapse voltage and resonant frequency have to be controlled at the same time, which limits the cMUTs applications.

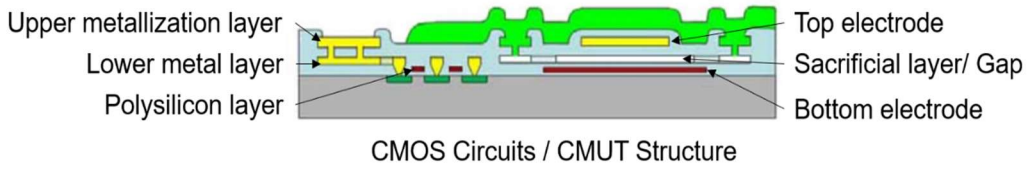
The other technique is a CMOS based process [30]. Figure 4 (a) shows the top

and cross-section view of a cMUT element side by side with CMOS circuits in cMUT in CMOS process. The standard structural layers for the cMUT and CMOS transistors are fabricated on the same chip [24], [25]. The cMUT devices are alternatively patterned by defining sacrificial layers, electrodes, and passivation layers within the interconnect metallization and dielectric passivation layers of the CMOS process. The upper CMOS metallization layer is used as the top electrode, the lower metal layer forms the sacrificial layer that creates the gap, and the polysilicon layer is used as the bottom electrode (Fig. 4 (b)). The silicon dioxide layer is deposited on the top of polysilicon layer and yields an isolation between these electrodes. The cMUT membrane is formed by the inter-metal dielectric combined with the overglass layer [31]-[35].

cMUT on CMOS process enables cMUTs to be fabricated on CMOS wafer. Hence, CMOS based process helps in reducing the problem of parasitic capacitance, which is induced in MUMPs based cMUTs. Moreover, since the fabrication processing of cMUTs is in parallel with the CMOS technique, cMUT-in-CMOS fabrication technique can save time and cost of the overall process. However, many current immersion applications such as intravascular ultrasound (IVUS) require a limited working space (human tissue), whereas both the electronic CMOS circuit and cMUTs have to be designed side by side and consume more space, so that it is not ideal for some medical applications. CMOS compatible fabrication process limits the cMUTs to be processed in low temperatures. Even though the flip chip bonding method has been invented to overcome this problem, the interconnection method still requires numerous fabrication steps which consequently increase overall cost.



(a)



(b)

Figure 4. Illustration of cMUT in CMOS process. (a) Top and cross-section view of cMUT side by side with CMOS circuits. (b) Cross-section view of a finished cMUT in CMOS fabrication process. [30]

Thesis Organization

The remainder of this thesis is organized as follows. Chapter 2 provides a working principle and some critical analytic equations of cMUT including spring constant, resonant frequency and pull-in voltage. In Chap. 3, four mask designs with dimension parameters are examined to study the analytic results. In Chap. 4, the main objective is to simulate the operation of cMUT using a commercial finite element software, COMSOL Multiphysics 4.3b, and to compare the simulation results with the analytical modeling results from previous chapter. In Chap. 5, a low-temperature CMOS compatible fabrication process is proposed in terms of: cavity formation, bottom electrode deposition, wafer bonding, membrane defining, top electrode deposition. Finally, we conclude the content of thesis and discuss the future works in Chap. 6 and Chap. 7, respectively.

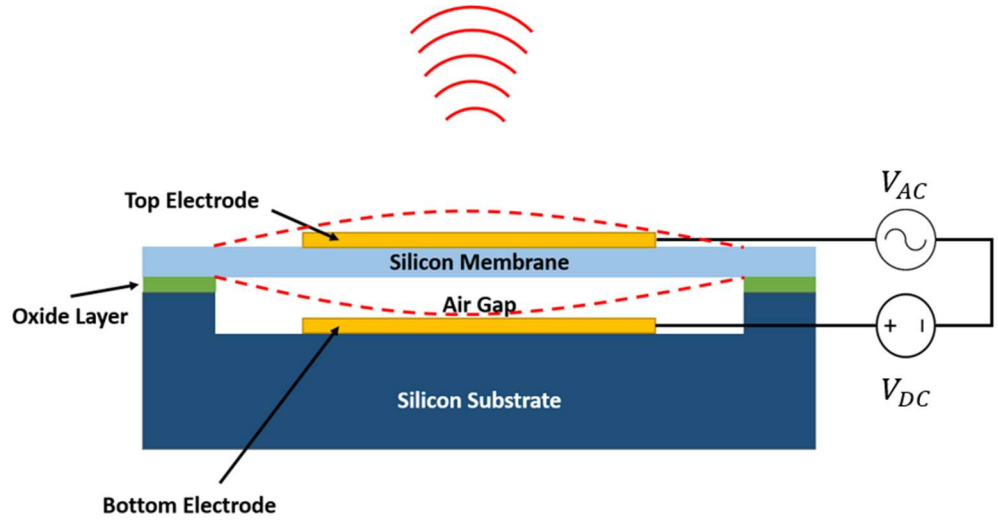
2. MODELING OF A CIRCULAR CMUT

Operation Principle of cMUT

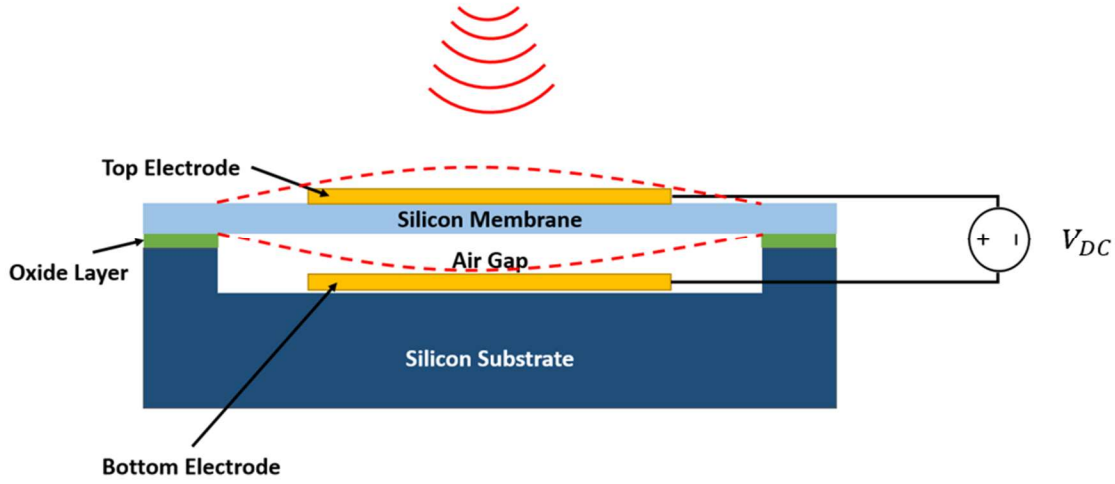
cMUTs make up arrays of multiple cMUT cells, and each cell consists of a thin, flexible membrane suspended over the cavity of the substrate, leaving an open-air gap in the medium between membrane and substrate as shown in Fig. 3. cMUT has a top electrode deposited on the silicon membrane and a bottom electrode deposited on silicon substrate. They are separated by an air gap like a capacitor. The detail fabrication process of cMUTs will be discussed in Chapter 5.

cMUTs can be used as both transmitters and receivers, as seen in Fig. 5 Their working principle is similar to that of pMUTs. In transmitting mode, an AC voltage with a DC biased voltage is applied across the two electrodes as shown in Fig. 5 (a). Due to an electrostatic force between two electrodes, the flexible membrane is bent toward the silicon substrate. The modulation results in vibration of the membrane to generate ultrasonography at the same frequency with the driving AC voltage. Here, DC bias voltage is required to be larger than the peak voltage of AC source in order for the cMUTs to work properly [4]. Otherwise, the membrane frequency will be larger than the AC frequency without applied DC bias voltage since electrostatic force is unipolar.

In receiving mode, the membrane is appropriately biased with a DC voltage and driven by continuous ultrasound waves seen in Fig. 5 (b). The capacitance changes among the cells thus generating electrical current under a constant biased voltage. The value of this current which is readout electronically results from the combination of the incident ultrasonic wave, the applied voltage, and the capacitance change.



(a)



(b)

Figure 5. Working principle of a single cMUT cell in (a) transmitting mode and (b) receiving mode.

Analytical Modeling of cMUT

In this section we develop an analytic model to determine the deflection, spring constant and pull-in voltage of cMUTs. Figure 6 shows the schematic drawing of the cross-section of a single cMUT cell with a bending membrane. The top and bottom

electrodes are ignored to simplify the analytical modeling and simulation. However, their thicknesses will be included in thickness of membrane and gap distance for calculation. In Fig. 6, *a* is a radius of silicon membrane, *t* is a membrane thickness, *g* is a gap distance from the bottom surface of membrane to the top surface of bottom electrode and *r* is a radial position from the center of circular membrane. The operation of cMUTs in specific or MEMS devices in general depends on spatial changes between electrodes or a slight bending of membranes resulting in the changing of its electrical properties. A small displacement can easily be detected through sensing of a capacitance and movement of the top electrode can be evaluated by changing electrical potential.

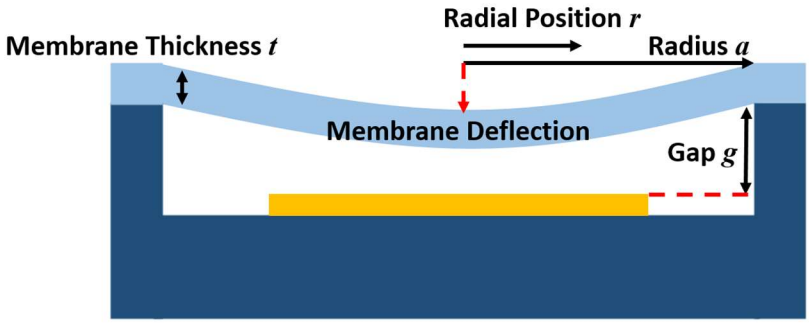


Figure 6. An ideal circular membrane cMUT. *a* is radius of membrane; *g* is the distance between the bottom surface of membrane and the top surface of bottom electrode; *t* is the membrane thickness.

Circular Membrane Spring Constant

We assume that a uniform pressure which evenly applying on surface of the membrane, P_0, includes the atmosphere pressure, P_{atm}, and the electrostatic force, F_{el}, between the two electrodes and is given

$$P_0 = P_{atm} + \frac{F_{el}}{\pi a^2}. \quad (1)$$

For the case of circular membrane with clamped edges, the deflection value has

zero at the edges and maximum at the center of circular membrane under a uniform pressure. Timoshenko and Woinowsky-Krieger introduced the equation of membrane's deflection, *w*, as function of P_0 [36]

$$w = \frac{P_0 a^4}{64D}\left(1 - \frac{r^2}{a^2}\right)^2. \quad (2)$$

where *D* is flexural rigidity of the membrane. *D* is also known as the resistance of a structure while undergoing bending loads. It depends greatly upon the membrane's elastic thickness and material properties, and is calculated from [37]

$$D = \frac{Et^3}{12(1-\nu^2)}. \quad (3)$$

Here, *t* is the thickness of the membrane, *E* and ν are the Young's modulus and Poisson's ratio of membrane material, respectively. At the center where $r = 0$, the top and bottom electrodes are closest and the deflection of membrane is at its peak value, w_{pk}:

$$w_{pk} = \frac{P_0 a^4}{64D}. \quad (4)$$

Since cMUTs operate at high frequency and the displacement of membrane due to the atmosphere pressure is relatively small compared to the thickness of the membrane, the term, P_{atm}, can be ignored for simplicity. Equation (4) can be rewritten in term of electrostatic force, F_{el}:

$$w_{pk} = \frac{F_{el} a^2}{64\pi D}. \quad (5)$$

A linear spring constant, *k*, when the membrane undergoes a load is analytically solve by applying Hooke's law to equation,

$$k = \frac{64\pi D}{a^2}. \quad (6)$$

Resonant Frequency and Effective Mass Modeling

One of the prominent characters of a moving membrane of a cMUT is resonant frequency, which is defined as the oscillation of a system that is not being excited by any external force. The membrane of a cMUT is actuated by an AC voltage and then vibrates to generate ultrasound waves in the medium in front of it. A cMUT device can be looked at as a mass-spring system where the flexible membrane is the spring, the attractive force drives the mass and the surrounding medium causes damping to the system. When an ultrasound penetrates into a fluid medium such as human body, there is reduction in amplitude of the ultrasound as a function of travel distance which is known as attenuation of ultrasound. This attenuation should be as low as possible for the receiver to detect the returning ultrasound waves from the target. High frequencies lead to high attenuation and it is challenging to detect the echo waves, whereas low frequencies will diminish the image resolution which is not good as well. The relationship between the attenuation coefficient and frequency is described as $A \sim A_0 f^{\beta}$, where A is attenuation, A_0 and β are material dependent constants, f is the frequency [38]. Therefore, keeping the resonant frequencies in range will optimize the quality of cMUTs. The first order resonant frequency, f_n, of a circular clamped plate is studied and defined as [39]

$$f_n = \frac{0.47t}{a^2}\sqrt{\frac{E}{\rho(1-\nu^2)}}. \qquad (7)$$

where ρ is the density of the membrane material. Considering a mechanical system with a spring fixed at one end and attached to a movable mass at the other end as shown in Fig. 7, the resonant frequency of the oscillating system is expressed as a function of spring constant, k

$$f_n = \frac{1}{2\pi}\sqrt{\frac{k}{m_{eff}}} \ . \quad (8)$$

where m_{eff} is the effective mass of the membrane and it can be developed by substituting equation (8) to equation (7). Therefore, the effective mass, m_{eff}, of circular membrane with clamped edge is given

$$m_{eff} = 1.92a^2\rho t \ . \quad (9)$$

Pull-in Voltage Modeling

As the potential difference between electrodes increases, the electrostatic force will proportionally increase. Meanwhile, the mechanical force stays the same independently with the applied voltage. There is a certain voltage point at which the attractive force overwhelms the restoring force of the spring and the membrane begins to collapse onto the substrate. It is called pull-in voltage, V_p. The pull-in voltage is the maximum voltage value at which the movable plate fluctuates at its peak and do not collapse to the bottom plate. Therefore, the evaluation of the pull-in voltage is a key factor in designing microstructure transducers. Figure 7 shows the simple mass-spring system of a typical cMUT device with two parallel capacitor plates with plate area, A. One plate is connected to a mechanical spring and movable and the other is fixed at base and separated by an initial cavity depth, g. The spring is used to represent the elasticity of the movable plate and has spring constant, k. The capacitance of the cMUT cell, C, is proportional to a plate area, A, and inversely proportional to a gap distance between the two plates, g-x, and is generated by

$$C = \frac{\varepsilon A}{g-x} \ , \quad (10)$$

where $\varepsilon = 8.854 \times 10^{-12}$ F/m is the permittivity of free space, x is the displacement of

membrane from the initial position.

To lessen the complexity of the system, a DC voltage, V_{el}, is only applied across the plates. The potential energy, E, stored in a parallel plate is given:

$$E = \frac{1}{2} C {V_{el}}^2$$

$$= \frac{1}{2}\left(\frac{\varepsilon A}{g-x}\right) V_{el}^2 \,. \tag{11}$$

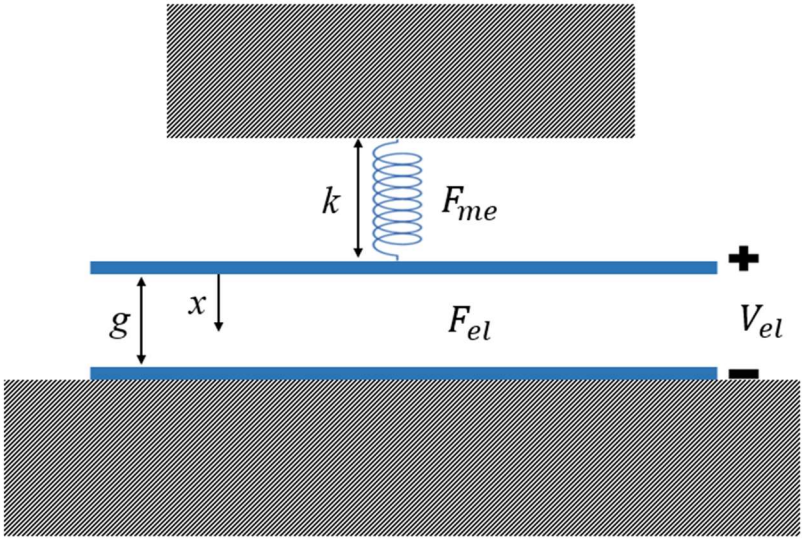


Figure 7. Schematic of an electrostatic capacitor.

The electrostatic force, $F_{el,}$ can be generated by differentiating the potential energy of the capacitor, E, with respect to the displacement of the top electrode, x:

$$F_{el} = \frac{\partial E}{\partial x}$$

$$= \frac{1}{2} V_{el}^2 \frac{\partial}{\partial x}\left(\frac{\varepsilon A}{g-x}\right)$$

$$= \frac{1}{2} \frac{\varepsilon A}{(g-x)^2} V_{el}^2 \,. \tag{12}$$

An electrostatic attraction force generating over the capacitor plates will pull them

together, while there is a retaining force, F_{me}, which is created by the mechanical spring restoring back in the opposite direction. We assume the membrane's restoring force acting on the top electrode has linear relationship to its displacement and is represented by:

$$F_{me} = -kx \ . \tag{13}$$

The negative sign indicates that F_{me} has opposite direction with F_{el}. Therefore, the net force, F, that causes the membrane to actuate is measured by:

$$F = F_{el} + F_{me}$$

$$= \frac{1}{2}\frac{\varepsilon A}{(g-x)^2}V_{el}^2 - kx \ . \tag{14}$$

At equilibrium, the net force on the membrane equals to zero because the electrostatic force and mechanical spring force cancel each other.

$$\frac{1}{2}\frac{\varepsilon A}{(g-x)^2}V_{el}^2 = kx \ . \tag{15}$$

Therefore, DC bias voltage, V_{el}, can be derived and has an expression of:

$$V_{el} = \sqrt{\frac{2kx(g-x)^2}{\varepsilon A}} \ . \tag{16}$$

To calculate the pull-in voltage, we first need to analyze the stability of the system at equilibrium point. From Hooke's law, the derivative of force of equation (14) with respect to x is the stiffness of the system. The stiffness of the system will be obtained by:

$$\frac{\partial F}{\partial x} = \frac{\partial}{\partial x}\left(\frac{1}{2}\frac{\varepsilon A}{(g-x)^2}V_{el}^2 - kx\right)$$

$$= \frac{\varepsilon A}{(g-x)^3}V_{el}^2 - k \ . \tag{17}$$

From equation (16), the stiffness at the equilibrium is expressed

$$\frac{\partial F}{\partial x} = \frac{2kx}{g - x} - k$$

$$= (\frac{2x}{g-x} - 1)k \, . \tag{18}$$

Let $\frac{\partial F}{\partial x}$ equals to zero, the pull-in point, x_p, at which the membrane begins to collapse is derived as:

$$\frac{2x_p}{g-x_p} = 1 \, . \tag{19}$$

Therefore, the pull-in point, x_p, can be simplified:

$$x_p = \frac{g}{3} \, . \tag{20}$$

It means that the system will work properly below the pull-in point, x_p, where is found to be 1/3 of the cavity depth, *g*. As shown in Fig. 8, the graph of stiffness with reference of the spring constant, *k*, shows negative when membrane displacement is less than 1/3 of the cavity depth and is rapidly positive when the membrane displacement passes over the pull-in point, x_p. Positive means the electrostatic force is greater than the spring mechanical force resulting in collapse condition when the membrane will completely deflect and collapse to the substrate.

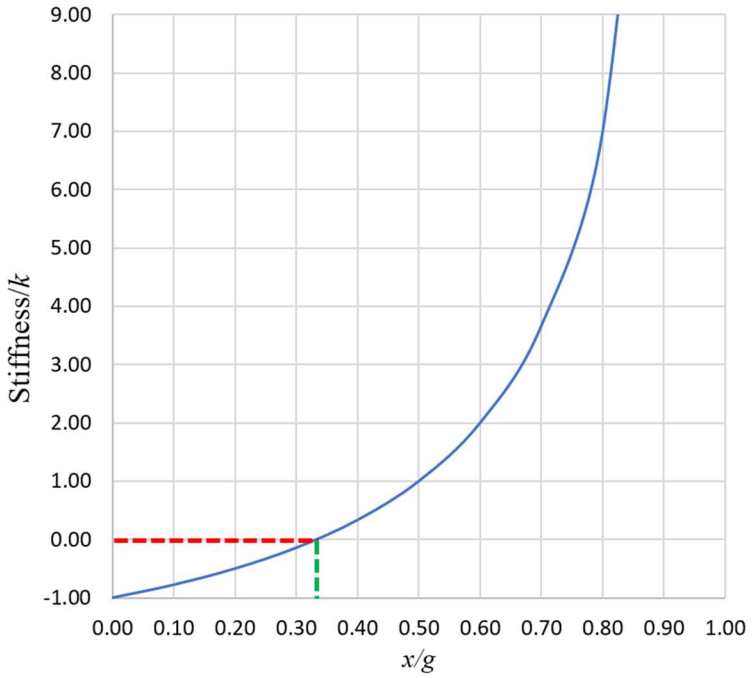


Figure 8. Equilibrium relationship between stiffness (reference k) and displacement of membrane. For $\frac{\partial F}{\partial x} < 0$ the membrane still be retained. For $\frac{\partial F}{\partial x} > 0$ the membrane starts to collapse to the bottom substrate.

Pull-in voltage is known as the maximum voltage that drives the membrane to collapse onto the bottom substrate. At that point, the attractive electrostatic force cannot be balanced by the restoring mechanical force of the membrane. Therefore, the pull-in voltage, V_p, can be extracted by substituting the pull-in point, $x_p = \frac{g}{3}$, into variation x in the DC bias voltage equation (16):

$$V_p = 0.54\sqrt{\frac{kg^3}{\varepsilon A}}. \tag{21}$$

One can find in Fig. 9 that the curve starts from origin value of zero, increases quickly to the maximum value of 0.54 and then decreases gradually for larger values of $\frac{x}{g}$. That maximum point corresponds to the 1/3 value of the cavity depth. Therefore, we can conclude that there is no solution for V_{el} greater than V_p, which is unstable condition for

the system.

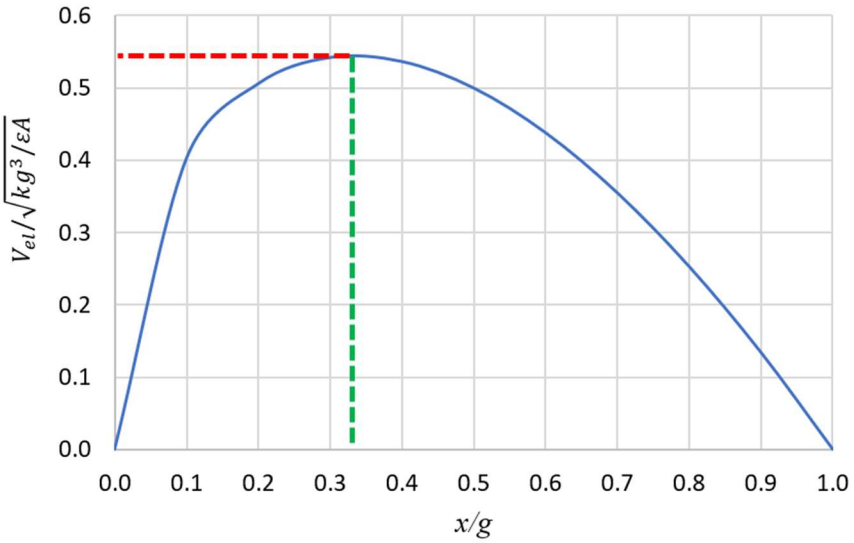


Figure 9. Equilibrium relationship between voltage (reference$\sqrt{kg^3/\varepsilon A}$) and displacement of membrane.

Figure 10 illustrates the relationship between system stiffness and applied bias voltage, it is the combination of the graphs shown in Fig. 8 and Fig. 9. The critical point is the pull-in point, x_p, where the membrane displacement is at 1/3 of the cavity. Notice that increasing bias voltage will make stiffness be less negative. At the pull-in voltage, the stiffness/k ratio equals to zero, where the electrostatic force equals to the spring mechanical force. Beyond that critical point, the graph shows a rapidly increasing in stiffness/k values which indicates that the membrane starts to collapse to the substrate.

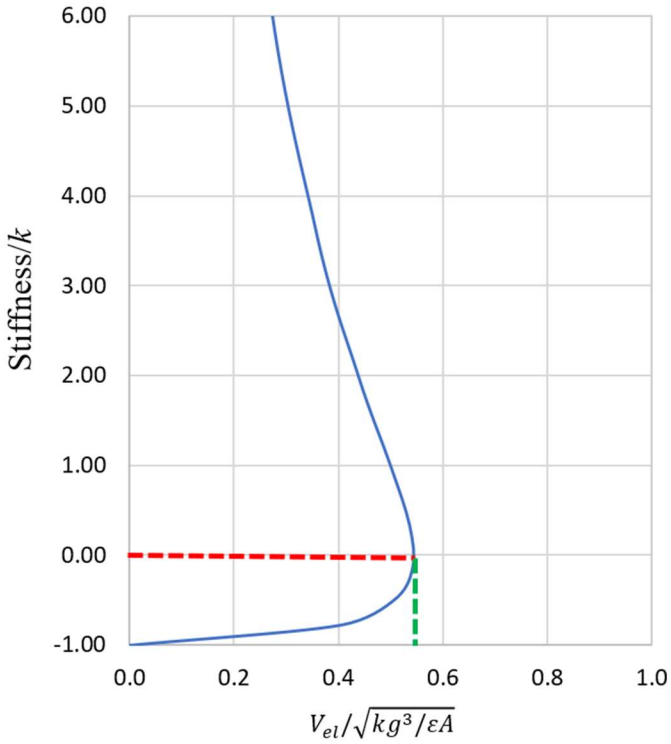


Figure 10. Spring stiffness (reference k) as function of applied voltage (reference $\sqrt{kg^3/\varepsilon A}$).

3. DESIGN OF CMUT

UV Mask Design

The proposed cMUT device is fabricated using photolithography to pattern microcavities, electrodes and contact pads. One particular mask is only used for each etching or deposition step. The layout of the UV mask designs is shown in Fig. 11. The mask designs are patterned on 5-inch soda-lime glass coated with chrome layer to block UV light during UV exposure. Mask I is for cavity formation, Mask II is for bottom electrode deposition, Mask III is for top electrode deposition and Mask IV is finally for opening the bottom electrode contact pads.

cMUT Cell Design

From the analytical equations that are derived from Chapter 2, it is obvious that the cMUT membrane's resonant frequency and spring constant scale with both thickness and radius of the membrane while the device's pull-in voltage is determined by the distance of cavity gap. Therefore, dimension parameters play important role in the working characteristic of cMUT as well as designing a cMUT device to achieve a desired resonant frequency application. Four different designs of cMUT cells have been made on the same wafer. Square array and circular array designs of cMUT with different number of elements as well as shape and size of the membranes are shown in Fig. 12. Table 1 is list of four geometrical designs for cMUT devices.

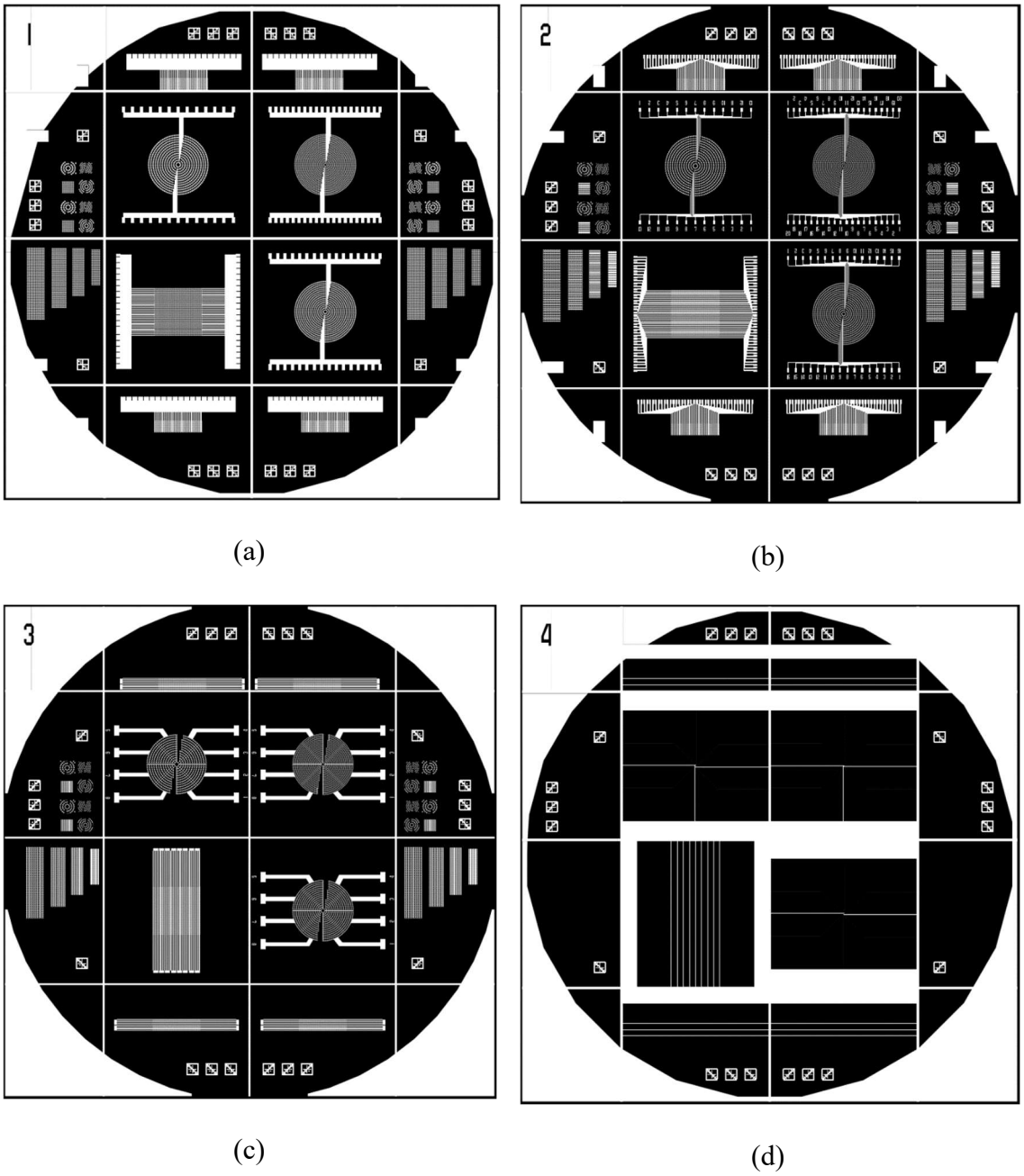


Figure 11. Four mask designs of cMUT. (a) Mask I for cavity formation, (b) Mask II for bottom electrode, (c) Mask III for top electrode, (d) Mask IV for opening bottom electrode contact pads.

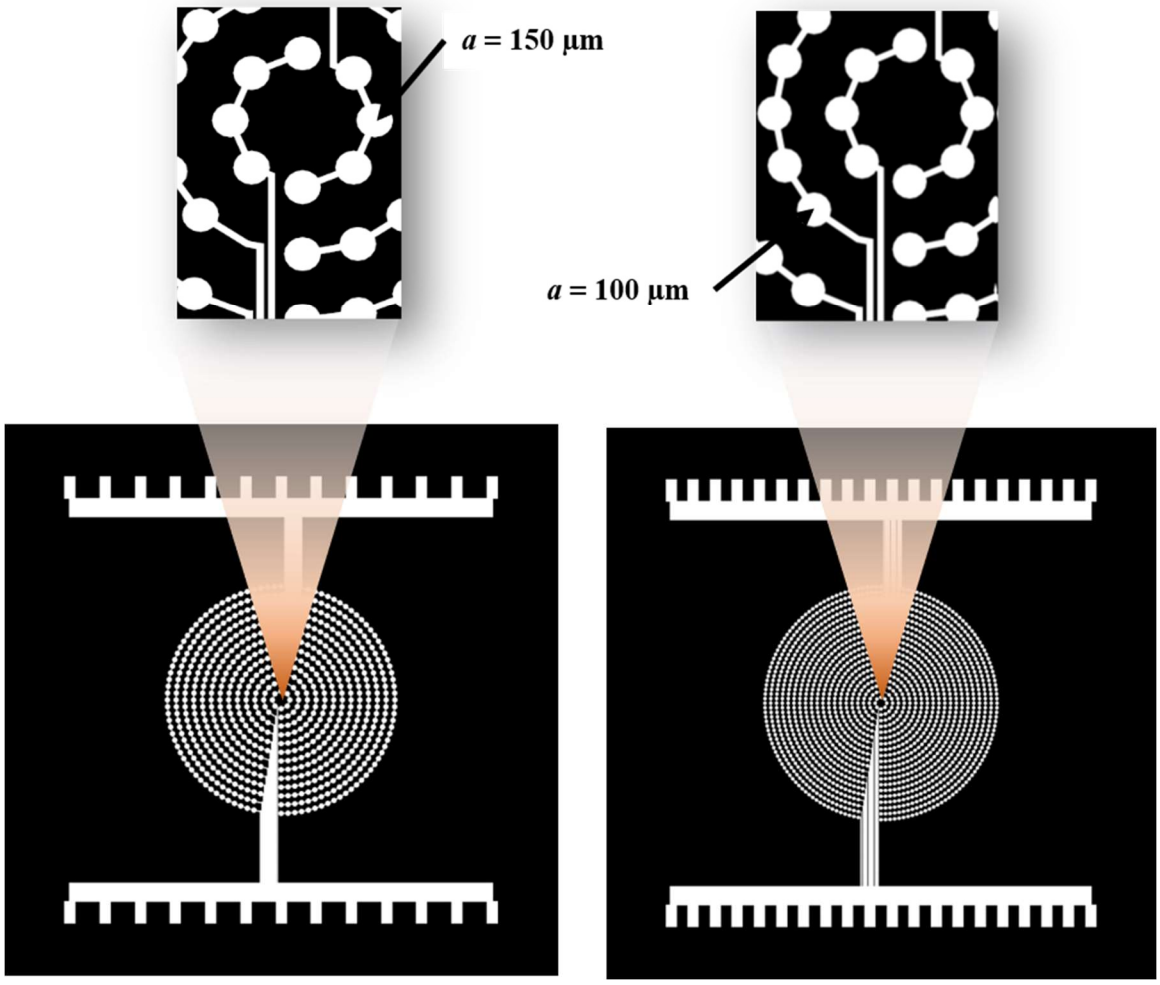


Figure 12. cMUT's mask designs. (a) Design 1: circular array, a = 150 µm, (b) Design 2: circular array, a = 100 µm, (c) Design 3: rectangular array, a = 100 µm, (d) Design 4: circular array, a = 125 µm.

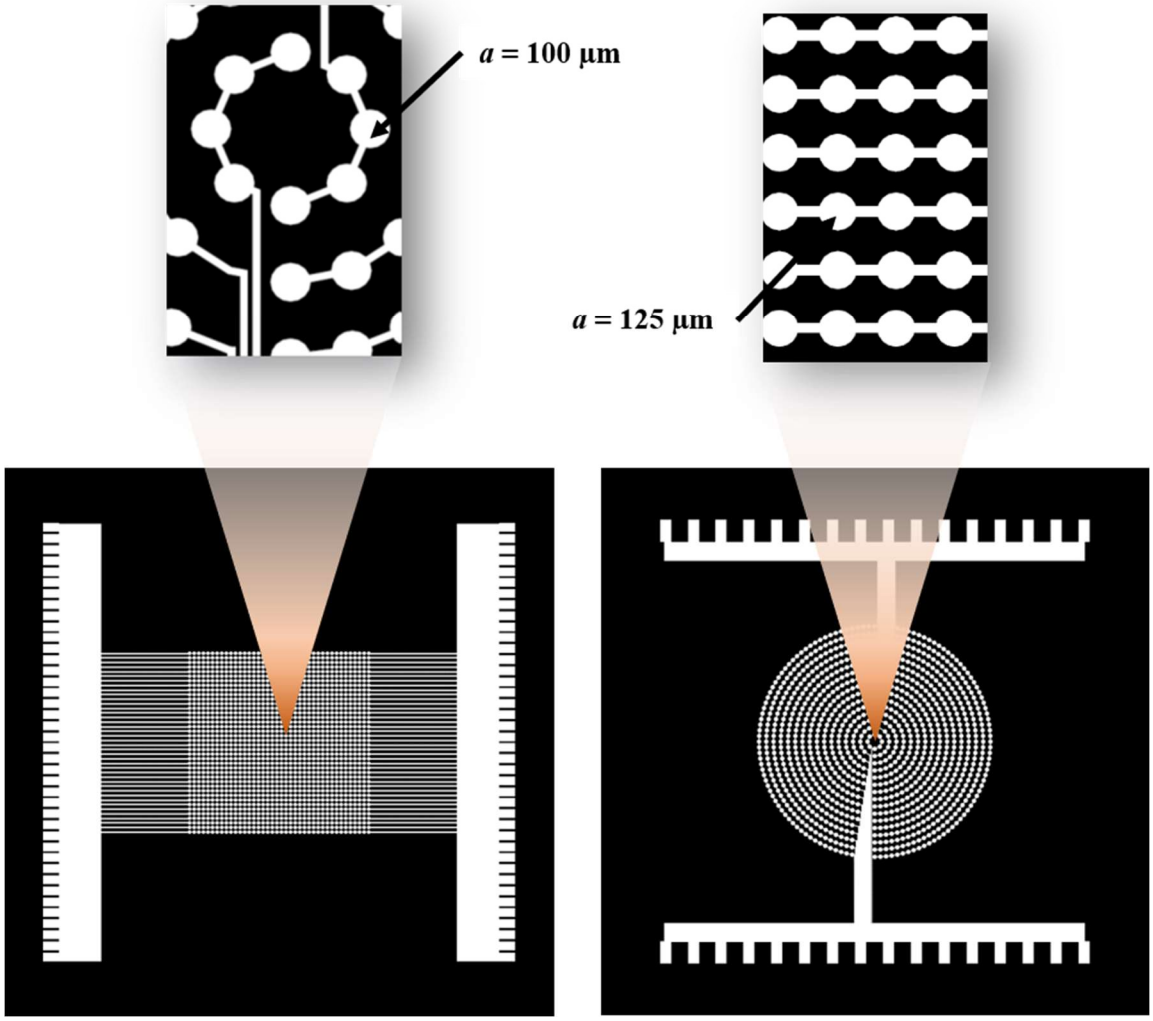


Figure 12 continued.

Table 1. The parameters of the designed capacitive Micromachined Ultrasonic Transducers (cMUTs) structure.

Designs	Array geometry	Number of elements	Membrane radius, *a*
Design 1	Circular	688	150 μm
Design 2	Circular	1590	100 μm
Design 3	Rectangular	1600	100 μm
Design 4	Circular	1030	125 μm

cMUTs with radiuses between 100 m and 150 m are design for evaluation of frequency response. Table 1 shows that cMUT cells in the second and third arrays have 100 μm in radius, while in the first and fourth arrays, the cells' radius are 150 μm and 125 μm, respectively. For simulation and modeling, the value of gap distance, *g*, is of 400 nm for analytic calculation considering 500 nm of the etched depth and the 100 nm of bottom electrode thickness. The membrane thickness of cMUT which is constrained by 1.5 μm device layer thickness of SOI wafer, is defined during the fabrication process. Additionally, 100 nm thickness of the top electrode is deposited on the membrane layer. So, the total of 1.6 μm thick membrane layer is used for simulation and analytical solutions. Thinner membrane improves the mechanical sensitivity of cMUTs since the membrane is more flexible resulting in lowering the pull-in voltage. The device with thicker membrane, on the other hand, allows higher bias voltage before pull-in condition and has higher resonant frequency which is suitable for high frequency application. Table 2 shows the results of analytical equations with the dimension parameters of cMUTs designs.

Table 2. Summary analytical results of cMUTs. Membrane thickness, t = 1.6 μm, gap distance, g = 400 nm, Young's modulus of silicon membrane, E = 170 GPa. Poisson's ratio of silicon membrane, ν = 0.28. Density of silicon membrane, ρ = 2330 kg/m^3.

Designs	Membrane radius, a	Spring Constant, k, Eq. (6)	Resonant Frequency, f_n, Eq. (7)	Pull-in Voltage, V_p, Eq. (21)
Design 1	150 μm	562 N/m	297 kHz	4.13 V
Design 2 & 3	100 μm	1264 N/m	669 kHz	9.28 V
Design 4	125 μm	809 N/m	428 kHz	5.94 V

4. SIMULATION

Both analytic modeling and simulation method have the potential for investigating system performance with different conditions. The analytical computation is a mathematic abstraction which provides a quick and simple analysis for characteristics of cMUT. However, it just provides generic ways to get performance results in multiple conditions and its accuracy of the model is based on assumptions. It means there is a limit to analytical modeling to represent a realistic cMUT device. Analytical modeling only considers the linear relationship between membrane's reflection and applied force. The membrane is as well assumed uniformly loaded, which only happens in ideal situation. Hence, the analytical modeling lacks accuracy and precision and ignores the non-linear property of the cMUT. Simulation, on the other hand, is used when analytical formulation cannot be derived. It provides result for each specific case with various function inputs, and its parameters can easily be adjusted for an appropriate environment. This chapter focuses on finite element method (FEM) analysis of cMUT using COMSOL Multiphysics 4.3b to fully characterize the device, and the analyzed results are then compared to previous analytical modeling results. It will present a profound insight on cMUT behavior. Simulating in 3D not only provides a better visualization of the behavior of cMUT cell but also illustrates the reality of the modeled process. The half section of 3D simplified model in COMSOL is shown in Fig. 13.

The dimension parameters of cMUT such as: membrane radius, membrane thickness, cavity depth, etc. are implemented in the geometry, and the geometry is created with a 3D model. For simplification, the supporting post and top electrode are not shown in the setup. However, the outer boundary of the membrane and the silicon

substrate are set to be fixed constraints during the simulation. For the materials, silicon is set for the membrane and substrate domain while air is set as the gap domain between the membrane and the substrate.

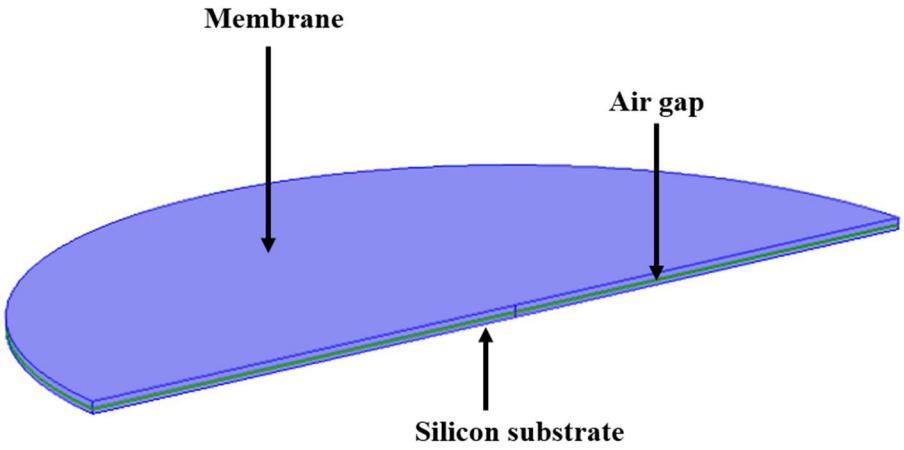


Figure 13. Half 3D model draw using COMSOL.

Eigen-Frequency Modal Analysis

Eigen-frequencies and mode shapes are considered thoroughly during designing cMUTs, because they define the characteristics of the system as well as show how the device response in the real life. When a cMUT vibrates at a certain eigen-frequency, its structure deforms into a corresponding shape which is called eigen-mode. Since circular membrane exhibits many symmetrical portions, it will have multiple eigen-frequencies, and the corresponding eigenmodes will not be the same. The Solid Mechanics (solid) model and Eigenfrequency analysis are set up for simulating the eigen-frequencies.

Figure 14 shows the first six mode shapes and eigen-frequencies for a particular silicon membrane's radius of 150 μm and a membrane thickness of 1.6 μm. The first eigen mode has frequency of 298 kHz and the membrane's deflection is perpendicular to the plane. The second and third modes have the same eigenfrequency of 621 kHz and the

plotted shape of twist which are rotated by 90°. The fourth and fifth modes also have the same frequency of 1.02 MHz and plotted shape of quadratic twist rotated by 45°. In the sixth mode, the membrane deflects at same direction with the first mode at 1.16 MHz. Observe that the first resonant frequency, 298 kHz is in close agreement with the analytical value, 297 kHz from Table 2 in Chapter 3.

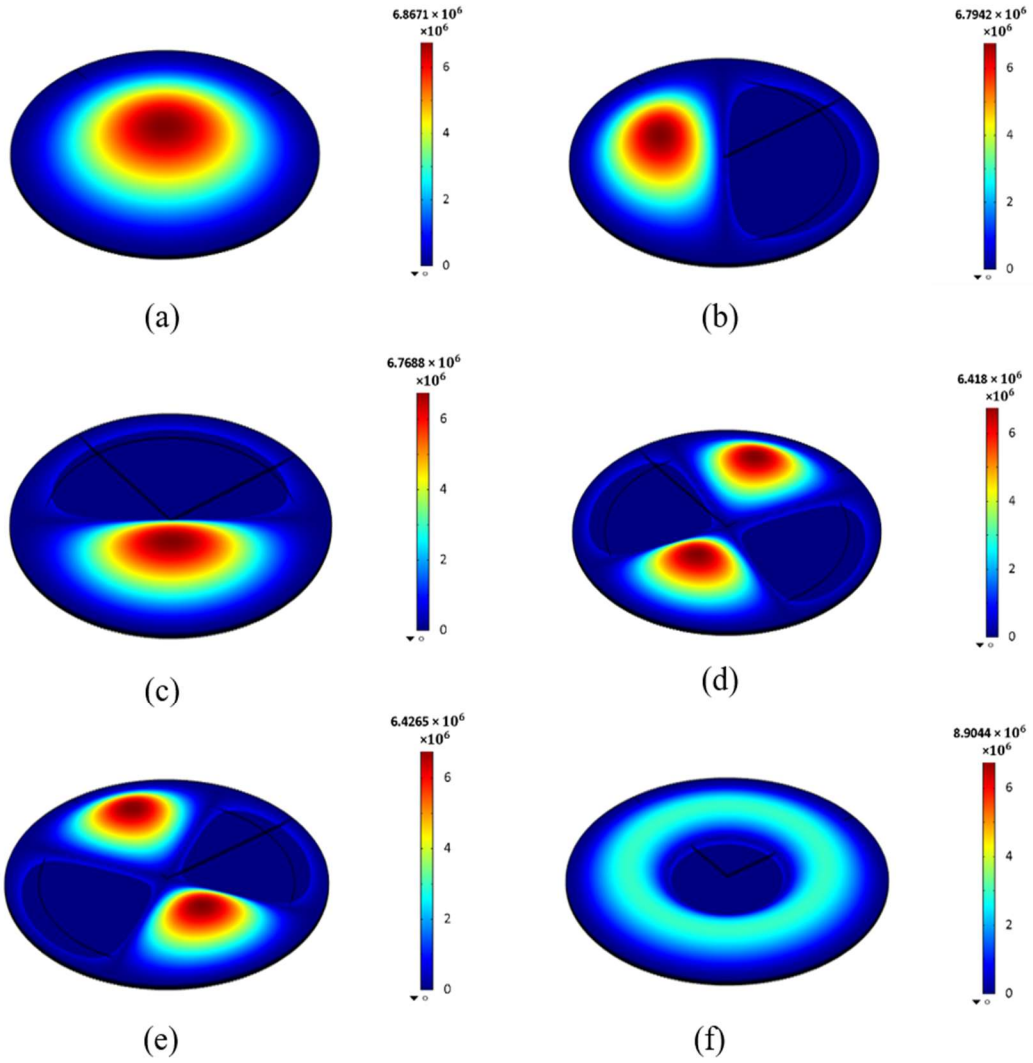


Figure 14. First six eigen-frequency modes of cMUT membrane with 150 um radiuses: (a) 298 kHz, (b) 621 kHz, (c) 621 kHz, (d) 1.02 MHz, (e) 1.02 MHz and (f) 1.16 MHz.

The first harmonic is chosen as a suitable mode for cMUT operation and the other frequency modes are not interesting since uneven shapes of membrane can cause non-uniform pressure radiation [40]. The operating frequencies of the proposed designs are the first eigen-frequencies of each design. Furthermore, the cooler to warmer range indicating the relative displacement which is lower to higher, and the red color represents the highest displacement of the membrane. Figure 15 shows the first resonant frequencies as a function of the radius of membrane for a fixed membrane thickness of 1.6 µm. Note that the larger membrane's radius results in lowering the resonant frequencies. A graph showing the relationship between the membrane thickness and the resonant frequencies is also created in COMSOL (Fig. 16). In this figure, the membrane thicknesses are linear proportional to the resonant frequencies of the membrane.

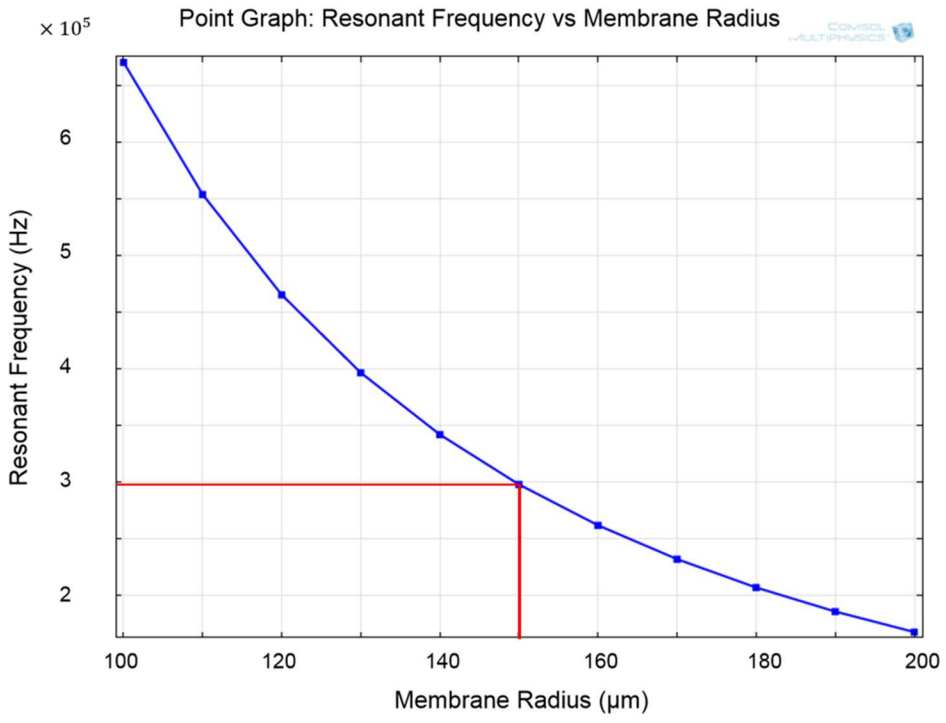


Figure 15. COMSOL result of relationship between membrane radius and resonant frequency with the membrane thickness of 1.6 µm.

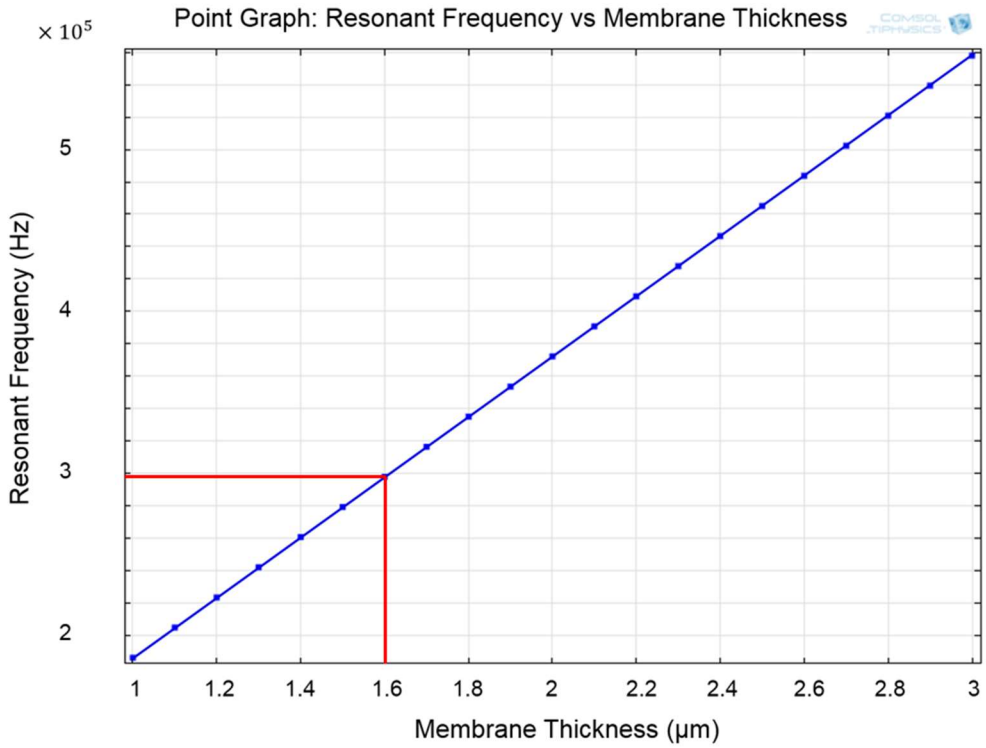


Figure 16. COMSOL result of relationship between membrane thickness and resonant frequency with the membrane radius of 150 µm.

Spring Constant

Using Hooke's law, the spring constant can be extracted from the displacement due to a given force. To simulate the spring constant of the membrane using COMSOL, the Electromechanics (emi) physics in the model library and Stationary study are chosen. A total force with magnitude of 300 nN is applied continuously in the negative z direction onto the upper boundary of the membrane. Silicon is used as the membrane's material with a defined membrane thickness of 1.6 µm. The result of membrane displacement deflected by 300 nN external force with membrane's radius of 150 µm is 0.53 nm occurring at the center of membrane which is shown in Fig. 17. By calculation, the spring constant received from Hooke's law is at approximate 567 N/m, which is in close agreement with the analytical value of 562 N/m in Table 2. The comparison of the

spring constants and the resonant frequencies between the modal analysis and simulation values using COMSOL are shown in the Table 3.

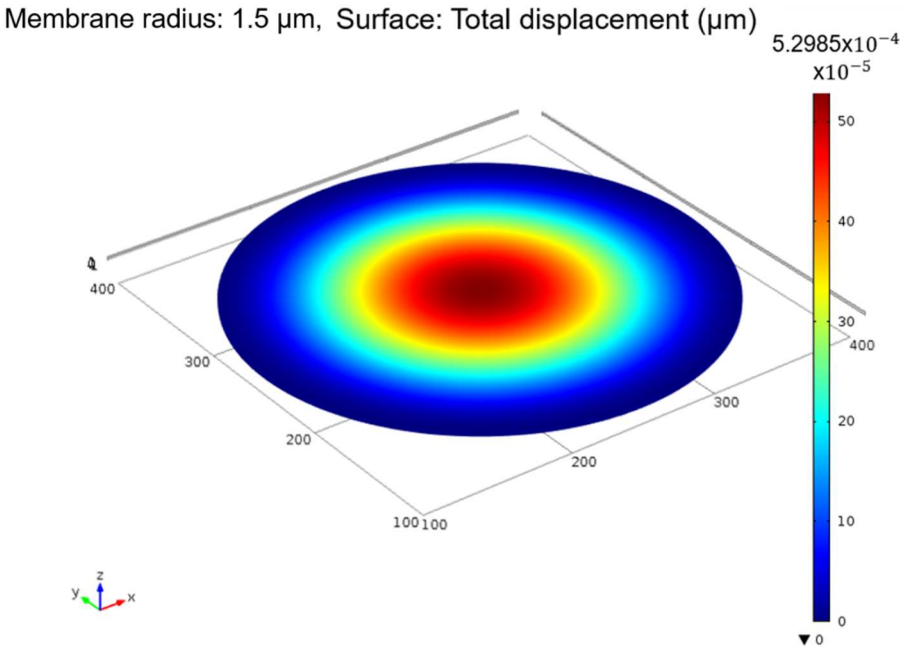


Figure 17. COMSOL result of membrane displacement when applying 300 nN force over a membrane with radius of 150 µm.

Table 3. Comparing analytical results and COMSOL simulation of cMUT.

Designs	Membrane radius, a	Spring Constant, k		Resonant Frequency, f_n	
		Analytical	COMSOL	Analytical	COMSOL
Design 1	150 µm	562 N/m	567 N/m	297 kHz	298 kHz
Design 2 & 3	100 µm	1264 N/m	1273 N/m	669 kHz	670 kHz
Design 4	125 µm	809 N/m	815 N/m	428 kHz	465 kHz

Pull-in Voltage

To perform the parametric analysis for pull-in voltage, a range of DC biased voltage from 1V to 8V is applied in the Parametric Sweep of the study. The Electromechanics (emi) model is also created. However, the boundary load from previous section is disabled, terminal is selected with the electric potential applied on the bottom surface boundary of the membrane and the top surface of the silicon substrate is set to ground. The model is run through a sequence of static analyses for different parametric voltage values. Every sequence follows through a certain number of iterations and the convergence is calculated. The process is repeated with the increment of 1V until the applied voltage reaches 8V. From previous chapter, we calculated the pull-in voltage is *4.13 V* for the 150 µm radius membrane. Observing the Fig. 18, the maximum displacement cMUT membrane's central point displacement is at *60 nm*, and this value is smaller than one third of the gap distance which is about 133.33 nm.

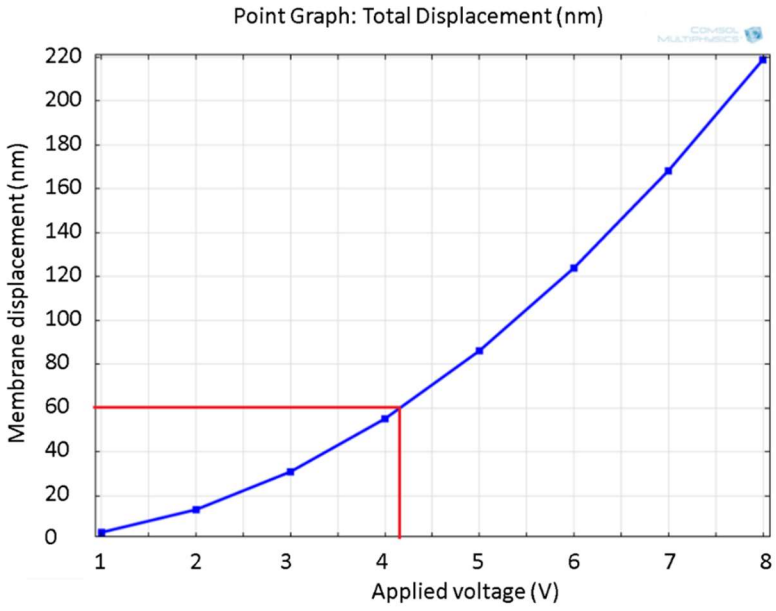


Figure 18. COMSOL result of relationship between applied voltage and membrane displacement.

Discussion

As mentioned earlier, cMUTs with four different array geometries and membrane dimensions are designed. A circular membrane cMUT cell is also studied for characterizing the properties such as resonant frequency, pull-in voltage and spring constant using COMSOL software. Measured resonant frequencies and spring constants for membrane radius of 100 μm, 125 μm and 150 μm respectively are shown in Table 3. It tells that the membrane radius has significant effect on cMUT's working properties. As the membrane radius increases, the resonant frequency and the spring constant values decrease rapidly. However, based on Fig. 16, if the membrane thickness increases in size, the resonant frequency also increases and is linearly proportional with the membrane thickness. For our design, since we already had our photomasks designed and fabricated, we may consider in changing the membrane thickness instead of membrane radius if we want to change the cMUTs' resonant frequency property in future.

5. FABRICATION OF CMUT

The fabrication of cMUTs is a four masks process using a wafer bonding technique to form resonant membranes. Wafer bonding technique is used to simplify the fabrication process of cMUT. In comparison to the surface micromachining, in which the cavity underneath the membrane is form by wet etching the scarified layer, wafer bonding technique is more flexible and less constrained [40], [41]. The proposed cMUTs are fabricated with a silicon wafer, which shows good electrical and mechanical properties, and is compatible with standard semiconductor processes such as etching, lithography, deposition, etc. The proposed fabrication sequence of cMUTs is classified into four steps: (1) cavity formation, (2) bottom electrode, (3) membrane bonding, and (4) top electrode. Since the wafer bonding process is under development, the ideas of the membrane bonding and top electrode processes are briefly described in this proposal.

Cavity Formation

In this research, 4-inch, <100> oriented, 500 μm thick, p-type silicon wafers are used. A silicon wafer is dipped into Nanostrip solution for 5 minutes. Nanostrip is a stabilized formulation of sulfuric acid and hydrogen peroxide compound which is used to remove organic and inorganic contamination on the silicon surface. The wafer is then rinsed in DI water and blow- dried with nitrogen gun. After rinsing, the wafer is dehydrated in an oven at 100ºC for 15 minutes and cooled down to a room temperature. Prior to applying photoresist, a thin layer of HMDS is spin-coated on the wafer at 3000 rpm for 30 seconds and the wafer is baked on a hot plate at 115ºC for 2 minutes. The HMDS layer promotes adhesion between photoresist and silicon wafer. Then, a 1.4 μm thick S1813 photoresist layer is spin-coated at 3600 rpm for 30 second and baked at 115ºC on hot plate for 90 second. After letting it cool for 1 minute, the wafer is UV-

exposed using the SuSS MJB4 mask aligner, which utilizes a 350W Hg bulb with i-line filter. Exposure is done for 5.5 seconds at lamp intensity of 24 mW/cm² measured at 365 nm wavelength with hard contact mode as seen in Fig. 19 (a). Development is done with 4 minutes immersion in MF-321 developer solution followed by 10 seconds immersion in another clean developer solution to get the image of the Mask I. The wafer is then brought in the oven for dehydration at 100°C for 10 minutes, the final photoresist thickness obtained is at 1.4 µm. Figure 19 (b) shows the photoresist patterns on the wafer's surface which reflects the patterns of the image of Mask I. After developing, the wafer is post- baked at 100ºC for 10 minutes.

The Oxford ICP-RIE Plasmalab 100 is used for producing microcavities on silicon substrate. In the reactive-ion etching (RIE) process, S1813 masks silicon from etching, and the opening area is etched. Prior to etching process, the chamber is cleaned with O_2 gas to remove any byproduct and gases that still remained in the chamber from previous use. With the wafer loaded in the chamber, an initial etching with Ar gas sputters away the native oxide that is grown on the surface of wafer. Then a mixture of SF_6 and Ar is chosen to produce the cavities. SF_6 etches Si by providing fluorine ions that reacts with the silicon substrate to form volatile SiF_4 gas, and Ar is a sputtering agent which works to remove non-volatile byproduct that inhibit chemical etching. Table 4 summarizes the parameters for the chamber cleaning and etching recipes for cavity formation. Total etching time for silicon is 17 second, then the photoresist is dissolved in acetone in a petri dish and rinsed under DI water, followed by drying with nitrogen shown in Fig. 19 (c). The etched wafer is then immersed in Nanostrip solution beaker for 5 minutes to remove any leftover photoresist from the solvent clean. The wafer is again

rinsed with DI water and dehydrated in oven at 100ºC for 10 minutes. The final etch depth of the cavities is 500 nm, which is inspected with a Bruker Dektak XT stylus profiler.

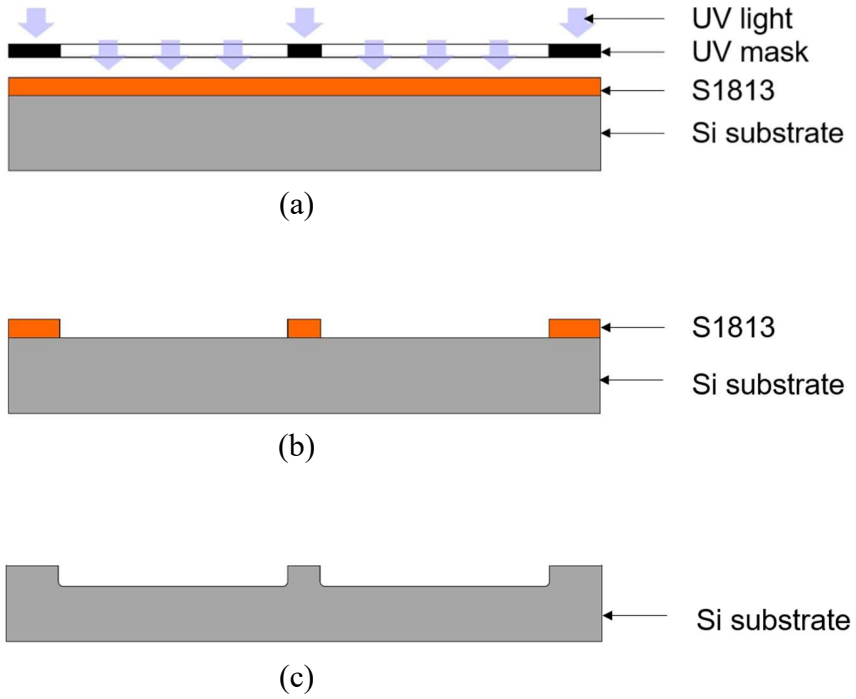


Figure 19. (a) Photoresist S1813 is manual applied by spin coating and then brought to expose under UV light, (b) Photoresist pattern appear on wafer's surface after developing with MF 321, (c) Etch profile of the cavities after plasma etching.

Since silicon substrate is not an insulator, an oxide layer is grown on the silicon wafer to isolate each electrode electrically before depositing the metal layer for bottom electrodes. A 20 nm thick oxide is thermally grown at 1000ºC for 25 minutes in the oxidation furnace. Figure 20 shows the microscope images of array of cMUT cells formed after plasma etching to create the cavities and furnace oxidation to create the insulation layer.

Table 4. Oxford ICP/RIE recipes for chamber cleaning, breaking through and real etching for cavities formation on silicon wafer.

	Chamber Cleaning	Etching	
		Breaking Through	Silicon Etching
Gas flow (sccm)	O_2: 40	Ar: 40	SF_6/ Ar: 45/ 5
Pressure (mTorr)	20	20	20
Source power (W)	1200	1500	800
Substrate power (W)	40	150	80
Chamber temperature (ºC)	70	70	70
Backside He cooling (ºC)	25	25	25
Time (sec)	300	5	17

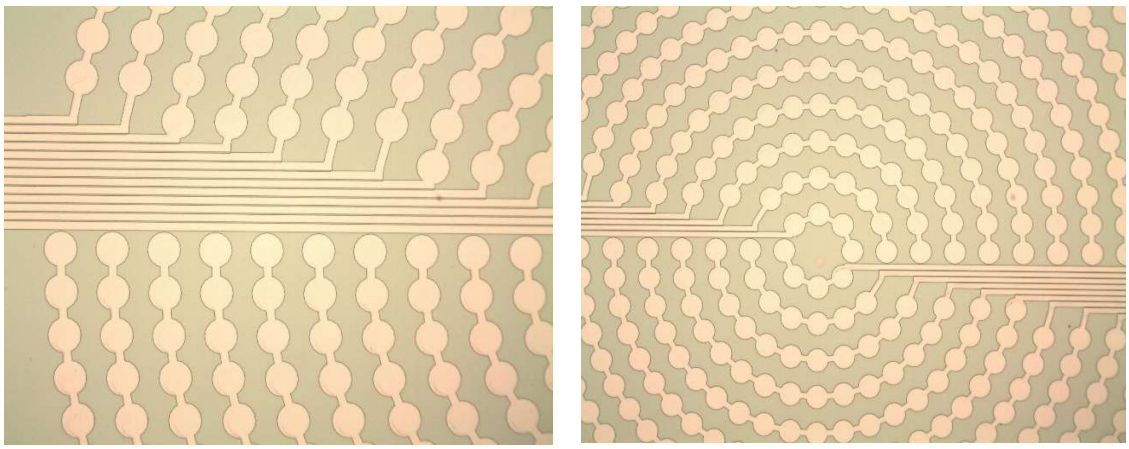


Figure 20. Images of partial of cMUT taken under microscope after the cavity formation and oxidation in furnace.

Bottom Electrode

cMUTs consist of two electrodes: a top electrode and a bottom electrode. The bottom electrodes are deposited in the cavities which were formed in the previous step using ICP RIE. In order to pattern bottom electrodes, UV lithography is employed. First, S1813 photoresist with thin layer of HMDS adhesion are spin-coated on the cavity patterned silicon substrate. The spin-coating, prebaking, UV exposure and developing processes are repeated with Mask II as shown in Fig. 21 (a). However, a mask aligning step is carried before the UV exposure. Four alignment marks which locate at four corners of Mask II are used to accomplish the perfect alignment between Mask II and wafer's pattern. Figure 21 (b) shows the schematic of close-section view of silicon substrate after developing. Prior to metal layer deposition, the wafer is dehydrated at 100ºC for 10 minutes in oven. Otherwise, the metal layer could not adhere successfully to the silicon surface and falls apart during lift-off process. A 100 nm thick Au layer is deposited as an electrode layer using e-beam evaporator (Angstrom Engineering EvoVac) with a 10 nm thick Cr layer as an adhesive layer between silicon wafer and Au layer. The thin film metal layer is deposited over the entire area (Fig. 21 (c)). Then, during lift-off process, the wafer is brought for sonicating in an acetone bath for 10 minutes at room temperature. The metal area with photoresist underneath is washed away which leaves behind the metal layer of the patterned areas inside the cavities. These metal patterned areas are the bottom electrodes of cMUTs (Fig. 21 (d)). Figure 22 shows a finished silicon wafer with a metal layer deposited in the cavities of cMUT. This wafer is the substrate of cMUT and will be bonded to the device layer of a SOI wafer in later processes. SEM images of cMUTs cavities and bottom electrode patterns are also taken

(Fig. 23). The difference in grayscale indicated the difference in material as well as the difference in height of the structure. As seen in Fig. 23, the darkest grey areas are the bottom electrode layers that are deposited in the cavities and the lighter grey areas are the silicon substrate with the cavities.

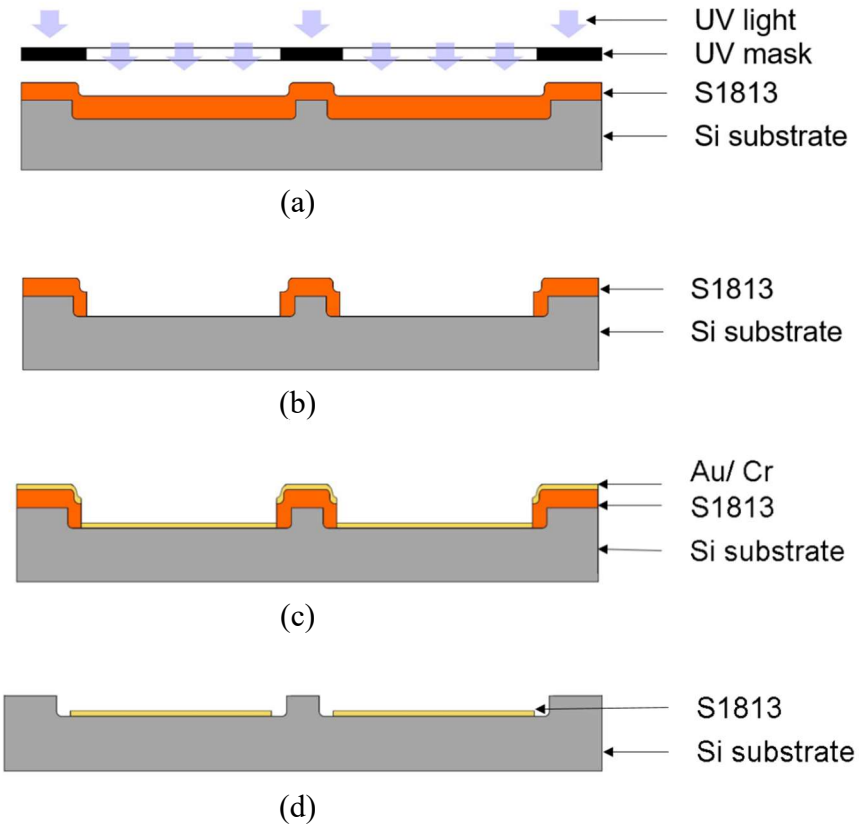


Figure 21. (a) Photoresist S1813 is applied over SiO_2 and. Mask II's pattern is aligned with pattern on the wafer through alignment marks using mask aligner, then UV light is used to expose the photoresist, (b) Photoresist pattern on wafer's surface which is used for metal lift-off, (c) Au/Cr deposition over the surface using Ebeam evaporation, (f) Metal lift-off to define the bottom electrodes.

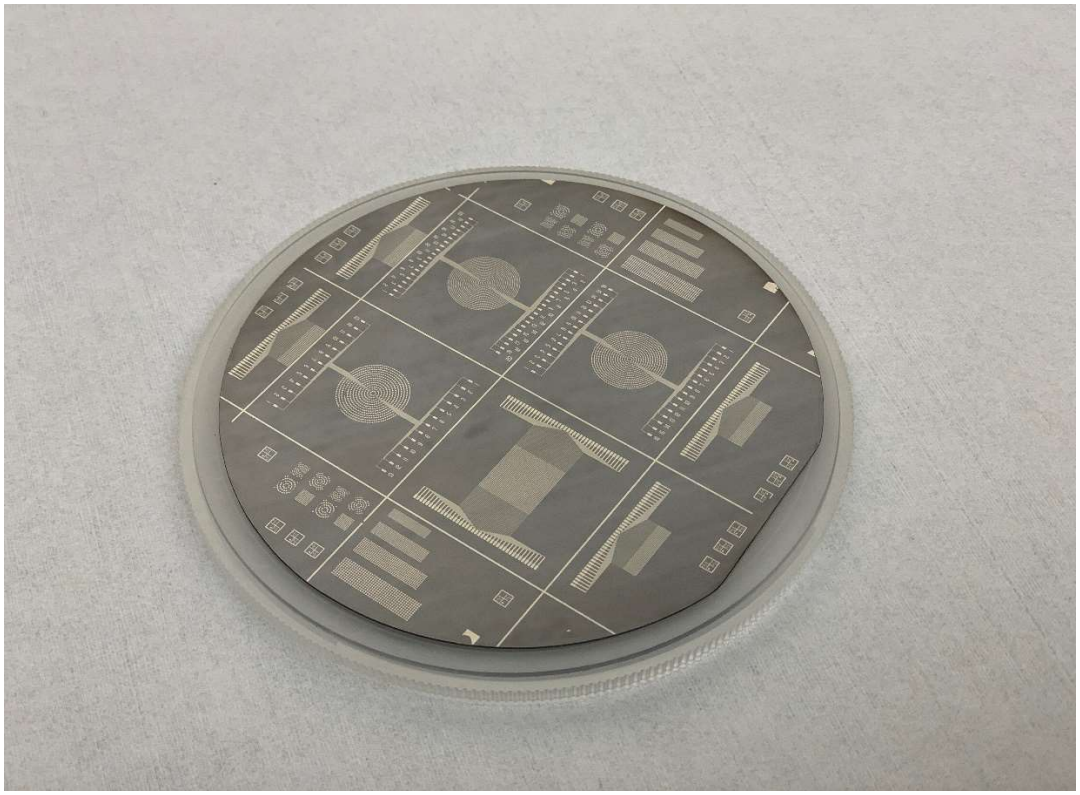


Figure 22. Patterned wafer of cavities and bottom electrodes.

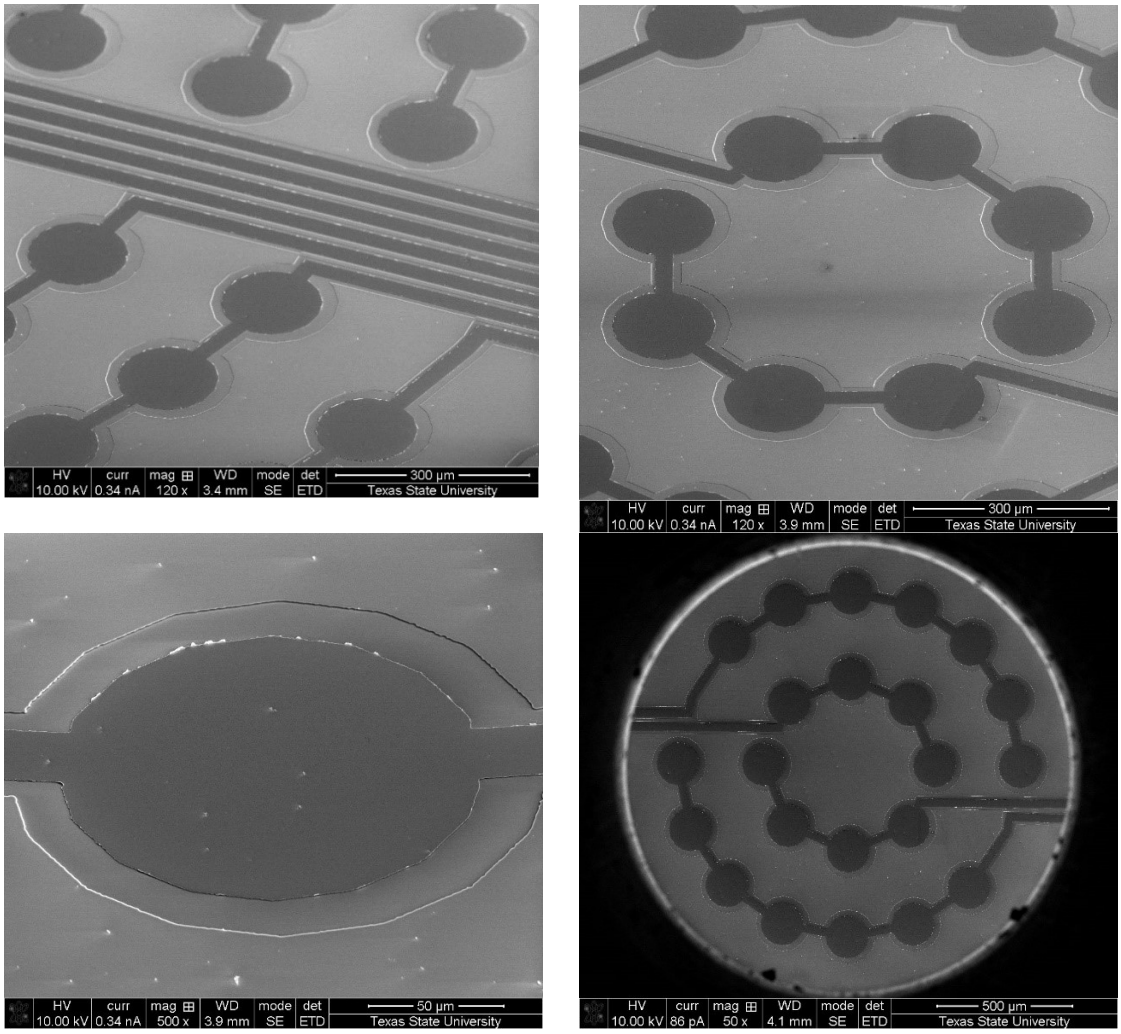


Figure 23. SEM images shows the bottom electrodes deposited in the cavities of one cMUT design.

Membrane Bonding

cMUT devices are mainly produced based on two fabrication methods: surface micromachining and wafer bonding technique [42, 43]. Surface micromachining method is used when the cavity underneath the membrane, called the sacrificial layer, is formed by wet etching. It requires careful design of membrane thickness, released area dimension and material selection during the wet etching. Wafer bonding technique, on the other hand, utilizes silicon device layer of silicon-on-insulator (SOI) wafer as the membrane

[44]. However, conventional wafer bonding technique requires very high temperature in the bonder chamber during the bonding process in order to make a good adhesion between wafers. As a result, it leads to the degradation of device material, the diffusion of metal deposition layer into the silicon substrate, or the destruction of integrated circuitry on the wafer being bonded [45]. In order to overcome these issues, wafer bonding process in low temperature range (< 400ºC) is presented.

The thickness of device layer of SOI wafer defines the membrane thickness. The silicon device layer is well selected from low internal stress single crystal silicon, which is suitable for making the membrane. The silicon substrate with cavities and a SOI wafer are first cleaned. Then, they are exposed with O_2 plasma at 100 W for 2 minutes for surface activation. Surface roughness is an important factor for high quality wafer bonding. Study shows that increasing in activation time would lead to decreasing in surface roughness; however, until a specific surface activation time, the surface roughness increases significantly with the increasing treatment time [46]. Thereafter, in order to minimize the moisture and dust particles built up on the bonded surfaces, both wafers are immediately brought in contact right after the surface treatment (Fig. 24 (a)). The wafer bonding process is carried out in an EVG 501 wafer bonding system at 1.41 x 10^{-1}mbar vacuum with the temperature as low as 300°C. The process is started with initial 20°C temperature applied on top and bottom wafers, and 5000 N of piston down force applied to the top of bonded wafers. An increment of 2500 N/min piston force and 15°C applied temperature is set up until the system reaches 10000 N and 300°C, then the parameters are kept stable for 3 hours. Molecular bonds are generated between the two wafers forming strong bonds, and these bonds can become inseparable if the annealing

process is executed long enough.

After bonding, the silicon handle portion of SOI wafer is etched all the way down to the buried oxide layer (BOX) of using a heated tetramethylammonium hydroxide (TMAH) solution. The BOX layer acts as a stopper during the wet etching process. Finally, the BOX layer is removed using 10:1 buffered oxide etchant (BOE) solution. Figure 24 (b) shows the device silicon layer on the SOI wafer now constitutes the membrane for cMUT after etching the oxide layer, and the thickness of the device layer of SOI wafer becomes the membrane's thickness.

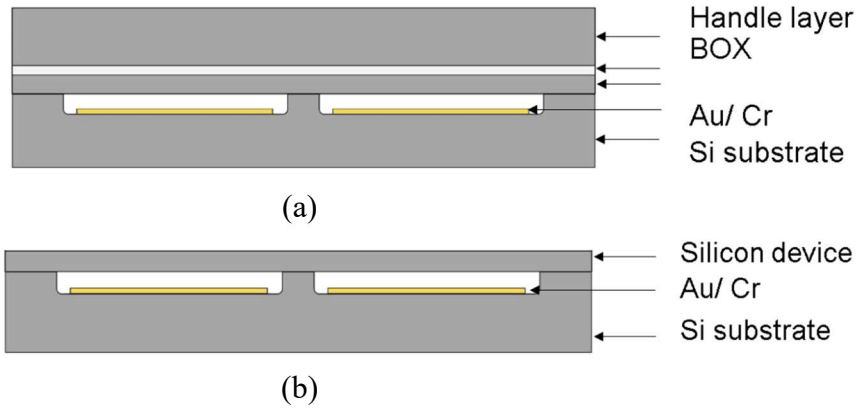


Figure 24. (a) SOI wafer is bonded on top of patterned wafer using wafer bonder, (b) Wet etching the handle layer and BOX layer to define the membrane.

Top Electrode

Photo Mask III is designed to expose the top electrode patterns on the surface of the membrane. The overall fabrication method remains unchanged from the bottom electrode formation. Photoresist S1813 is spun on top of the silicon device layer then patterned using standard contact lithography. UV light exposes the uncovered areas and these areas are then dissolved during the developing step which is used to pattern the area for metal deposition as seen on Fig. 25 (a) and Fig. 25 (b). After the exposure and

developing, the wafer is brought for dehydration at 100°C in oven for 15 minutes in order to make good contact with deposited layer of Cr and Au. E-beam evaporation is again used for deposition of metal layers on the top surface of the membrane. Figure 25 (c) illustrates the Cr/ Au layer deposited over the resist pattern on the membrane. Figure 25 (d) shows the top electrodes patterned in the middle of membrane after the lift-off procedure. Finally, Mask IV is used to define trenches to separate four cMUTs chips on the wafer as well as to open the bottom metal contacting pads using silicon dry etching.

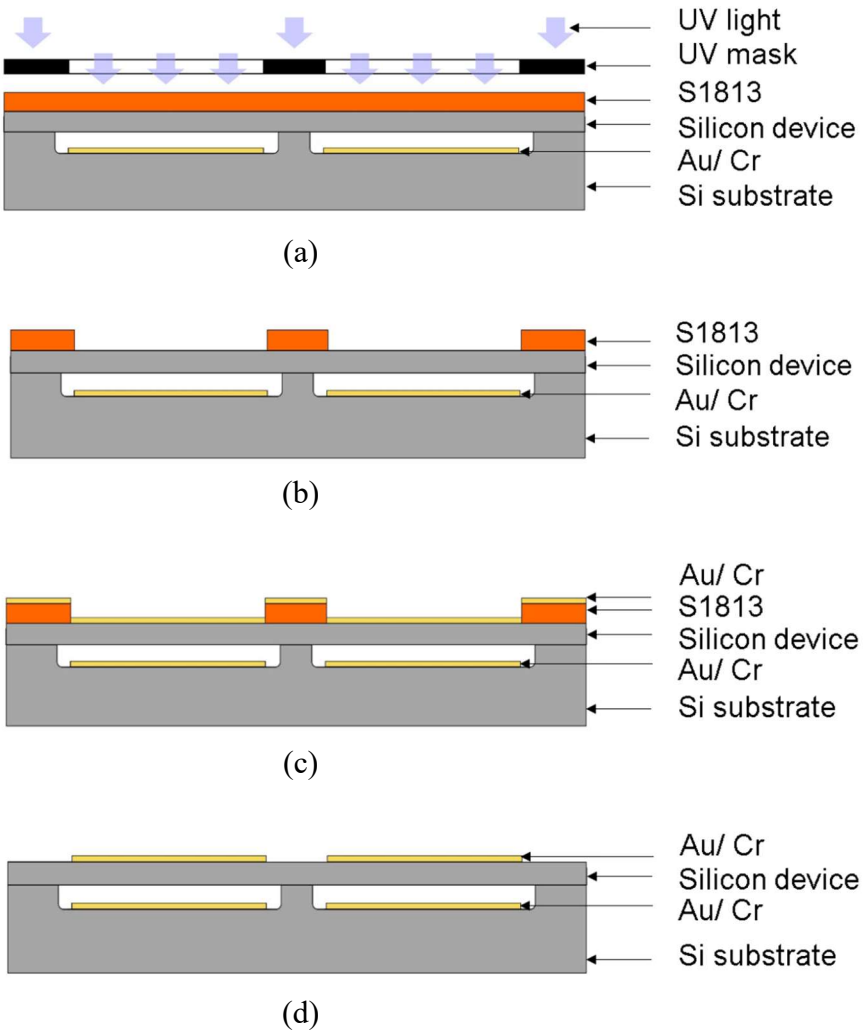


Figure 25. (a) Photoresist applied over the membrane and mask III exposure, (b) Photoresist pattern to define top electrodes, (c) Cr/Au deposition using Ebeam evaporation tool, (d) Metal lift-off to remove metal deposited on top of patterned photoresist.

6. CONCLUSION AND DISCUSSION

The capacitive micromachined ultrasound transducers (cMUTs) have emerged as a favorable ultrasonic transducer technology in MEMS research community due to advantages such as wider bandwidth, higher sensitivity, and ease in fabrication and CMOS compatibility. A cMUT cell consists of an oscillating membrane, which is suspended over a substrate. By applying an AC voltage on a DC bias voltage between the electrodes on the membrane and the substrate, the membrane vibrates and generates ultrasound waves into a medium. Conversely, incoming continuous ultrasound waves actuate the membrane causing a change in the device's capacitance and the result is readout electronically.

An analytical modeling of cMUT was evaluated based on a moveable plate capacitor attached to a mass-spring system. The analytical resonant frequencies were 298 kHz, 669 kHz, 428 kHz and the spring constants were 562 N/m, 1264 N/m, 809 N/m for the 150 μm, 100 μm, 125 μm membrane radius of cMUTs design, respectively. A finite element analysis was also employed to estimate the pull-in voltages, resonant frequencies, and spring stiffnesses of the system. These values were compared to analytical modeling. The FEM analysis was done in COMSOL Multiphysics 4.3b software. The cMUTs resonated at 298 kHz, 671 kHz, 465 kHz and the spring constants were simulated to be 567 N/m, 1273 N/m, 815 N/m, respectively, for 150 μm, 100 μm, 125 μm membrane's radii. Good agreement was shown between analytical and FEM models.

The fabrication process for cMUTs were proposed with silicon and SOI wafer using wafer bonding technique. Photolithography patterns the cavities, electrodes and

contact pads, while wafer bonding defines the membrane. Four distinct structures were fabricated on the same chip by four photo mask layers. Mask I is designed to form cavities, Mask II, III are used to make bottom and top electrodes deposition on the silicon substrate and top of the membrane respectively, and Mask IV is for make trenches and opening the bottom contacting pads.

Unfortunately, the cMUT devices in this work are still in the process of fabrication and the wafer bonding is still investigated to obtain a successful surface bonding. However, the analytical modeling and the finite element method analysis were performed, which benefit us in both assessing preliminary designs and monitoring the progress from a design to an actual working device of cMUTs.

7. FUTURE WORK

The cMUT is still at its early stages and requires further study for improvements. The analytical modeling needs to incorporate a better membrane shape, more accurate membrane thickness and gap distance. The piston like assumption needs to be eliminated during calculation. Moreover, time dependent finite element analysis is of crucial importance to observe the dynamic behavior of cMUT cells. However, in this work, we only perform the finite element analysis of a single cMUT cell. Therefore, in future, analysis in arrays form need to be considered to present a more profound insight in acoustic domain of cMUTs.

The fabrication process of cMUTs in this thesis is still in progress at the wafer bonding step due to improperly working of the bonder system. A complete cMUTs device must be done in future to obtain a successfully working device so that we can be able to perform experimental tests. In order to operate the cMUTs electronically in array form, they require to be coupled with test equipment probes through the opening contacting pads.

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